SOLUTIONS
WITH
SPEED
1993-1994
Comlinear
Corporation

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1993-94 Databook

Solutions with Speed

Comlinear Corporation, located in Fort Collins, Colorado, is a manufacturer and supplier of high-performance analog signal processing components. Comlinear's signal conditioning product line includes high-speed hybrid and monolithic operational amplifiers, buffers, and clamping amplifiers. The data converter product line includes track/hold amplifiers and analog-to-digital converters. The corporate philosophy is to focus development on products that make a significant contribution toward solving customer problems. The result has been the ever-expanding line of high-performance products included in the following pages.

The company is housed in a custom-built facility, which is DESC certified to MIL-STD-1772. Manufacturing, Quality Assurance, Research and Development, Administration and Marketing are centered in this location.

Comlinear's proprietary signal processing components are sold worldwide to a diverse group of commercial, industrial and military customers. Representative application areas include communications (satellite systems, radar, fiber optics), avionics (electronic counter measures, instrumentation), video (high resolution displays, video processing and distribution), and automatic test equipment.

Comlinear believes that a deeply-rooted dedication to quality is a critical path to customer satisfaction. Statistical process control and team quality concepts are approaches used throughout the company to improve quality in activities ranging from new product releases to order processing to shipping. It is only through this comprehensive approach to quality that lasting improvements in all product and service areas can be achieved.

Comlinear's goal is to offer our customers superior products with quality and service second to none.

DISCLAIMER INFORMATION

Warning-Life Support Systems

Comlinear's products are not authorized for use in life support devices or systems without express written authorization from the President of Comlinear Corporation. Life support devices or systems are those which are intended to support or sustain life, and whose failure to perform when properly used in accordance with the instructions provided can be reasonably expected to result in significant personal injury or death to the user.

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Comlinear makes no warranty with respect to its products except as expressly set forth in its standard conditions of sale. All implied warranties, including any implied warranty of merchantability or fitness for a particular purpose, are hereby disclaimed. Any warranty extended on Comlinear products is limited to the replacement of the defective component and does not cover personal injury, property damage, or incidental, consequential or special damages.

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Information on all products and services furnished herein by Comlinear Corporation is believed to be accurate and reliable at the time of this printing. Comlinear reserves the right to make changes to its products and specifications at any time without notice. Comlinear Corporation does not assume responsibility for the use of the products described herein.

The products in this databook are covered under one or more of the following patents: 4,358,739; 4,502,020; 4,628,279; 4,639,685; 4,713,628; 4,757,275; 4,766,367; 4,780,689; 5,049,653 (other patents pending).

January 1993

Product Summary
Contents

Product Summary Guide

Comlinear Corporation

Modular Series

Model[1,3]	-3db Bandwidth (MHz)	Gain[2] (dB)	Gain Flatness (db to MHz)	R^{in} & R^{out} (Ω)	Output at -1dB Gain Compression (+dBm@MHz)	Rise & Fall Time (nsec)	Overload Recovery Time (nsec)	Group Delay (nsec)	Deviation from Linear Phase (°)	Equivalent Input Noise (μV_{rms})	Package
CLC100	500	20	± 0.05 to 300	50	12 @ 500	0.600	<2	1.4	1	20	1.9" X 4.14" Mach. Alum. Case
CLC102	250	15	± 0.4 to 200	50	26 @ 100	1.6	—	2.3	1	46	3.0" X 3.0" Mach. Alum. Case

Model[1,3]	Gain (matched load) (dB)	bandwidth P_{out} (MHz, dBm)	input impedance (Ω)	output impedance (Ω)	V_{out}, I_{out} (matched load) (V, mA)	power supply range (V)	output current (mA)	input voltage (V)
CLC140	20	500, 10	50	50	± 1.25, ± 15	± 5 to ± 16	± 20	± 0.5
CLC142	15 (inv.)	250, 18	50	50	± 10, ± 250	± 12 to ± 16	± 250	±2
CLC143	15 (inv.)	220, 18	50	50	± 10, ± 250	± 12 to ± 16	± 250	± 2
CLC144	14	1100, 12	50	50	± 1.5, ± 35	± 9 to ± 16	± 40	± 0.5
CLC146	0	220, 10	FET	50 or 75	± 5, ± 100	± 10 to ± 16	± 150	$\pm V_{cc}$

Model[1,3]	Gain (open load) (V_o/V_i)	bandwidth P_{out} (MHz, dBm)	input impedance (Ω)	output impedance (Ω)	V_{out}, (open load) I_{out} (V, mA)	power supply range (V)	output current (mA)	input voltage (V)
CLC160	5 to 20	170, 18	50 to 1k	50 to 200	± 10, ± 200	± 10, to ± 16	± 250	$\pm V_{cc}$
CLC162	2 to 5	250, 10	50 to 1k	50 to 1k	± 10, ± 100	± 5 to ± 16	± 150	± 6
CLC163	5 to 40	170, 10	50 to 1k	50 to 1k	± 10, ± 100	± 5 to ± 16	± 150	note 1
CLC166	10 to 40	170, 10	50 to 200	50 to 1k	± 10, ± 50	± 5 to ± 16	± 75	note 1
CLC167	10 to 40	150, 10	50 to 200	50 to 1k	± 10, ± 200	± 10 to ± 16	± 200	note 1

NOTE: THE OUTPUT MUST NOT BE OVERDRIVEN FOR THESE PARTS. THEREFORE THE MAXIMUM $\pm V_{in}$ WILL BE $\pm (|V_{cc}| - 4V)/A_v$

Unity-Gain and Linear Amplifiers (typical specifications, + 25°C, $R_s = 50\Omega$)

Model[1,3]	Key Features	– 3db Bandwidth (MHz)	Gain (V/V)	Full Power BW (MHz @ V_{pp}, R_L)	Harmonic Distortion (dBc @ 20MHz, $2V_{pp}$)	Settling Time (nsec, %)	Output (V, mA)	Slew Rate (V/μsec)	Output Offset Drift(mV,μV/°C)	Test Conditions	Versions[1] J	E	I	K	M	8	L
CLC104	Very Wideband Linear Amp	1100	14dB	1050 @ 2, 50	– 44, – 43	1.2, 0.8	1.5, 40	6000	50, 375	R_L 50Ω V_{cc} = ±15V			√				
CLC110	Closed-Loop Design Low Distortion	730	0.97	90 @ 5, 100	– 65, – 65	5, 0.2	4, 70	800	2, 20	R_L = 100Ω V_{cc} = ±5V	√	√	√			√	√
CLC114	Quad Buffer Low Power	200	0.97	95, @ 2, 100	– 50, – 58	10, 0.1	4, 25	450	.5, 9	R_L = 100Ω V_{cc} = ±5V	√	√	√			√	√
CLC115	Quad Buffer High Speed	700	0.99	270 @ 4, 100	– 62, – 62	12, 0.1	60	2700	2, 25	R_L = 100Ω V_{cc} = ±5V	√	√	√			√	*

Operational Amplifiers (typical specifications, +25°C)

Model 1,3	Key Features	–3dB Bandwidth (MHz)			Gain Range ($A_v = V_o/V_i$)	Full Power BW (MHz @ V_{pp}, R_L)	Settling Time (nsec, %)	Output (V,mA)	Slew Rate (V/µsec)	Input Offset Drift (mV, µV/°C)	Test Conditions	Versions[1]						
		$\|A_v\| = 4$	$\|A_v\| = 20$	$\|A_v\| = 40$								J	E	I	K	M	8	L
CLC103A	High Output Current	170	150	130	± 1 to 40	80 @ 20, 100	10, 0.4	± 11, 200	6000	10, 50	$R_L = 100\Omega$ $V_{cc} = \pm 15V$			√		√		
CLC203A	High Output Current	180	160	130	± 1 to 50	60 @ 20, 100	15, 0.2	± 11, 200	6000	0.5, 5	$R_L = 100\Omega$ $V_{cc} = \pm 15V$			√		√		
CLC200A	General Purpose	100	95	90	± 1 to 50	25 @ 20, 200	18, 0.1 25, 0.02	± 12, 100	4000	10, 35	$R_L = 200\Omega$ $V_{cc} = \pm 15V$			√			√	
CLC201A	Low Offset and Drift	100	95	90	± 1 to 50	50 @ 20, 200	18, 0.1 30, 0.02	± 12, 100	4000	0.5, 5	$R_L = 200\Omega$ $V_{cc} = \pm 15V$			√			√	
CLC220A	General Purpose	200	190	160	± 1 to 50	100 @ 10, 200	8, .01 15, 0.02	± 12, 50	7000	10, 35	$R_L = 200\Omega$ $V_{cc} = \pm 15V$			√			√	
CLC221A	Low Offset and Drift	200	170	120	± 1 to 50	130 @ 10, 200	15, 0.1 18, 0.02	± 12, 50	6500	0.5, 5	$R_L = 200\Omega$ $V_{cc} = \pm 15V$			√			√	
CLC205A	Overdrive Protected Low Power	190	170	120	+ 7 to + 50 – 1 to – 50	100 @ 10, 200	22, 0.1 24, 0.05	± 12, 50	2400	3.5, 11	$R_L = 200\Omega$ $V_{cc} = \pm 15V$			√	√		√	
CLC206A	Overdrive Protected 100mA Output Current	200	180	90	+ 7 to + 50 – 1 to – 50	70 @ 20, 200	19, 0.1 22, 0.05	± 12, 100	3400	3.5, 11	$R_L = 200\Omega$ $V_{cc} = \pm 15V$			√	√		√	
CLC207	Low Distortion	250	170	90	+ 7 to + 50 – 1 to – 50	100 @ 10, 200	24, 0.05	± 12, 150	2400	3.5, 11	$R_L = 200\Omega$ $V_{cc} = \pm 15V$			√	√		√	
CLC300A	Low Cost 100mA Output Current	105	85	70	+ 1 to 40	45 @ 20, 100	20, 0.8	± 10, 100	3000	10, 25	$R_L = 100\Omega$ $V_{cc} = \pm 15V$			√				
CLC231A Buff-Amp™	Low Gain Low Power	$\|A_v\| = 1$ 165	$\|A_v\| = 2$ 165	$\|A_v\| = 5$ 120	± 1 to 5	95 @ 10, 100	12, 0.1 15, 0.05	± 11, 100	3000	1, 10	$R_L = 100\Omega$ $V_{cc} = \pm 15V$			√	√		√	
CLC232	Low Distortion	$\|A_v\| = 1$ 220	$\|A_v\| = 2$ 175	$\|A_v\| = 5$ 110	± 1 to 5	95 @ 10, 100	15, 0.05	± 12, 100	3000	1, 10	$R_L = 100\Omega$ $V_{cc} = \pm 15V$			√	√		√	
CLC400	Low Cost Low Power	$\|A_v\| = 1$ 220	$\|A_v\| = 2$ 200	$\|A_v\| = 8$ 60	± 1 to 8	50 @ 5 100	12, 0.05	± 3.5, 70	700 (NI) 1600 (IN)	2, 20	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√	√			√	√
CLC401	Low Cost Low Power	$\|A_v\| = 7$ 180	$\|A_v\| = 20$ 150	$\|A_v\| = 50$ 75	± 7 to 50	100 @ 5, 100	10. 0.1	± 3.5, 70	1200	3, 20	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√	√			√	√
CLC402	14-Bit Accurate Low Offset and Drift	$\|A_v\| = 1$ 260	$\|A_v\| = 2$ 190	$\|A_v\| = 8$ 85	± 1 to 8	80 @ 5, 100	25, 0.0025	± 3.5, 55	800	0.5, 3.0	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√	√			√	√
CLC404	High Full-Power BW Low Power, High Slew	$\|A_v\| = 2$ 165	$\|A_v\| = 6$ 175	$\|A_v\| = 20$ 60	+ 2 to + 21 – 1 to – 20	165 @ 5, 100	10, 0.2	± 3.3, 70	2600	2.0, 30	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√	√			√	√
CLC406	Low Cost Low Power	$\|A_v\| = 2$ 180	$\|A_v\| = 6$ 160	$\|A_v\| = 10$ 100	± 1 to 10	130 @ 5, 100	12, 0.05	± 2.7, 70	1500	2, 30	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√	√			√	√
CLC409	Very Wideband	$\|A_v\| = 2$ 350	$\|A_v\| = 6$ 150	$\|A_v\| = 10$ 100	± 1 to 10	110 @ 5, 100	8, 0.1	± 3.5, 70	1200	0.5, 25	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√	√			√	√
CLC410	High-Speed Video Op Amp with Disable	$\|A_v\| = 1$ 220	$\|A_v\| = 2$ 200	$\|A_v\| = 8$ 60	± 1 to 8	50 @ 5, 100	12, 0.05	± 3.5, 70	700 (NI) 1600 (IN)	2, 20	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√	√			√	√
CLC411	High-Speed Video Op Amp with Disabler	$\|A_v\| = 1$ 275	$\|A_v\| = 2$ 200	$\|A_v\| = 10$ 37	± 1 to 10	75 @ 15, 100	15, 0.1	± 4.5, 70	2300	2, 30	$R_L = 100\Omega$ $V_{cc} = \pm 15V$	√	√	√			*	*
CLC412	Dual Amp Low Power	$\|A_v\| = 2$ 320			± 1 to 10	105 @ 4, 100	12, 0.05	± 2.2, 70	1300	2, 30	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	*	*			*	*
CLC414	Quad Amp Low Power	$\|A_v\| = 2$ 70	$\|A_v\| = 6$ 90	$\|A_v\| = 10$ 60	± 1 to 10	55 @ 5, 100	16, 0.1	± 2.8, 70	1000	2, 30	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√	√			√	√
CLC415	Quad Amp High Speed	$\|A_v\| = 2$ 180	$\|A_v\| = 6$ 160	$\|A_v\| = 10$ 140	± 1 to 10	120 @ 5, 100	12, 0.1	± 2.6, 70	1500	2, 20	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√	√			√	√

Operational Amplifiers (typical specifications, +25°C)

Model[1,3]	Key Features	– 3dB Bandwidth (MHz)			Gain Range ($A_V = V_o/V_i$)	Full Power BW (MHz@V_{pp}, R_L)	Settling Time (nsec, %)	Output (V, mA)	Slew Rate (V/μsec)	Input Offset Drift (mV,μV/°C)	Test Conditions	Versions[1]						
												J	E	I	K	M	8	L
CLC 420	Voltage Feedback Low Gain	|A_V|=1 300	|A_V|=2 100	|A_V|=5 25	± 1 to 10	40@5, 100	18, 0.01	3.2, 70	1100	0.5, 4/1, 3	R_L ± 100Ω V_{cc} = ±5V	√	√	√			√	√
CLC422	Voltage Feedback High Gain	|A_V|=30 250	|A_V|=40 200	|A_V|=50 120	±30 to ±200	200@5, 100	17, 0.2	±3.8, 70	2300	0.8, 2	R_L ± 100Ω V_{cc} = ±5V	√	√	√			√	√
CLC425	Ultra Low Noise Wideband Op Amp		|A_V|=20 85	|A_V|=40 40	±10 to ±1000	TBD	22, 0.1	3.4, 90	350	0.1, 3	R_L ± 100Ω V_{cc} = ±5V	√	√	*			*	*
CLC430	Low Gain Op Amp with Disable	|A_V|=1 48	|A_V|=2 55	|A_V|=10 19	± 1 to 10	27@10, 100	35, 0.05	±8, 85	2000	2, 25	R_L ± 100Ω V_{cc} = ±15	√	√	√			√	√
CLC501	Clamped Output 1nsec Overload Recovery	|A_V|=8 165	|A_V|=20 120	|A_V|=32 80	+ 7 to + 50 – 1 to – 50	80@5, 100	12, 0.05	±3.5, 70	1200	1.5, 10	R_L ± 100Ω V_{cc} = ±5V	√	√	√			√	
CLC502	Clamped Output, Low Offset, 14-bit Settling	|A_V|=1 190	|A_V|=2 150	|A_V|=8 75	+ 1 to 8	65@5, 100	25, 0.0025	±3.5, 55	800	0.5, 3.0	R_L ± 100Ω V_{cc} = ±5V	√	√	√			√	
CLC505	Very Low Programmable Supply Current/ Power (10mW-100mW)	|A_V|=6 50 I_{cc}1mA	|A_V|=6 100 I_{cc}3.4mA	|A_V|=6 150 I_{cc}9mA	+ 2 to + 21 – 1 to – 20	80@5, 500	14, 0.05	±3.3, 25	1200	3.0, 40	I_{cc} = 3.4mA V_{cc} = ±5V	√	√	√			√	√

High Power Amplifiers (typical specifications, +25°C, R_L = 50Ω)

Model[1,3]	Key Features	– 3dB Bandwidth (MHz)	Large Signal Bandwidth (MHz@V_{pp})	2nd/3rd Harmonic Distortion (dBc)				Rise Time (nsec)	Input Offset Drift (mV,μV/°C)	Gain Range (V/V)	R_{out} Range (Ω)	Output (V, mA)	Versions[1]			
				10dBm (2V_{pp})		24dBm (10V_{pp})							I	K	M	8
				20MHz	100Mhz	20MHz	100MHz									
CLC560	High-power, adjustable output impedence	215	120@10V_{pp}(24dBm)	–60/ –62	–54/ –44	– 46/ –38	–33/ –25 (50MHz)	1.6	2.0, 35	+ 5 to + 80	25Ωto200Ω	± 10V, 200mA	√			√
CLC561		215	150@10V_{pp}(24dBm)	–59/ –62	–35/ –49	–50/ –41	–40/ –30	1.5	2.0, 35	+ 5 to + 80	25Ωto200Ω	± 10V, 200mA	√			√

Variable Gain Amplifiers (typical specifications, + 25° C)

Model[1,3]	Key Features	–3(dB) Bandwidth (MHz)		Gain Adjust Range (dB)	Signal Non-Linearity (%)	Full Power BW (MHz@V_{pp},R_L)	Settling Time (nsec, %)	Output (V,mA)	Slew Rate (V/μsec	Output Offset Drift (mV,μV/°C)	Version[1]						
		Signal Channel	Control Chan.								J	E	I	K	M	8	L
CLC520	Voltage Controlled Gain (AGC)	160	100	– 40	0.04	140 @ 4, 100	12, 0.1	±3.5, 70	2000	40, 100	√	√	•			•	
CLC522	Variable Gain Amplifier (VGA)	165	165	– 40	0.04	150 @ 5, 100	18, 0.1	±4, 70	2000	25, 100	√	√	*			*	*

Analog Multiplexers (typical specifications, +25°C)

Model[1,3]	Channels	Switching Speed (ns)	Input Voltage Range	Crosstalk Rejection (dB)	Settling Time to 0.01%	Settling Time to 0.0025%	2nd Harmonic Distortion (dBc)	3rd Harmonic Distortion (dBc)	Digital Interface	Features	Versions[1]						
											J	E	I	K	M	8	L
*CLC 532	2:1	6	±3.4V	- 80	17ns	35ns	- 80	- 86	TTL/ECL	Buffered input/output	√	√	√			√	
*CLC 533	4:1	7	±3.4V	- 80	17ns		- 80	- 86	TTL/ECL	Buffered input/output	√	√	√			√	

Analog to Digital Converters (typical specifications, + 25°C)

Model[1,3]	Resolution (Bits)	Sampling Rate (MSPS)	Input Voltage Range	Differential Non-Linearity (LSB's)	Spurious Free Signal Range SFSR (dB)	SNR (excl. harmonics) (dB)	Dynamic Test Conditions	Digital Interface	Power Dissipation (W)	Architecture	Features	Versions[1]				
												C	J	I	K	M	8
CLC922B	12	dc to 10	±1V	0.35	66.6	66.6	F_s =10MSPS F_{in} =4.996MHz FS =–1dB	TTL	4.1	±5V Sub-system	Internal T/H and reference has gain and offset adjust			√			√
CLC925B	12	dc to 10	$2V_{pp}$ over a –2V to + 2V range	0.35	66.8	66.6	F_s =10MSPS F_{in} =4.996MHz FS =–1dB	TTL	4.2	Complete sub-system				√			√
CLC935	12	dc to 15	±1V	0.7	75.0	66.3	F_s =15MSPS F_{in} =7.227MHz FS =–1dB	ECL	5.2	Complete Sub-system		√					*
CLC936	12	dc to 20	±1V	0.7	65.0	64.0	F_s =20MSPS F_{in} =9.685MHz FS =–1dB	ECL	5.4	Complete Sub-system		√					*
→ Q3, 93 CLC937		dc to 25.6			65.0	62.0	F_s =25.6MSPS F_{in} =9.685MHz FS = 1dB		6.4		Internal T/H and reference	√					*
→ Q1, 94 CLC950	12	dc to 25.6	±1V	1.0	65.0	64.0	F_s =25.6MSPS F_{in} =9.685MHz FS = 1dB	TTL/ECL	1.9	Complex Monolithic	Internal T/H			√	√		√

Track + Hold Amplifiers (typical specifications, + 25° C, $R_L = R_S = 50\Omega$, $V_{cc} = \pm 15V$)

Model[1,3]	H-to-T Acquistion Time, Tolerance	T-to-H Settling Time to 1mV (nsec)	Effective Aperture Delay (nsec)	Aperture Jitter ($psec_{rms}$)	– 3dB Bandwidth (MHz)	Slew Rate (V/μs)	Pedestal Offset (mV)	Feedthrough Rejection (dB at 20MHz)	Output (± V, mA)	Digital Control	Versions[1]				
											J	I	K	M	L
CLC940 FLash-Track™	10, 1.0 16, 0.1	12	2.5	1	150	470	2	74	2.2, 50	ECL or TTL		√		√	
CLC942	20, 0.1 25, 0.01	5	– 1.5	1.4	70	300	8	78	2.2 50	ECL		√		√	

NOTES:

[1]The version designation indicates the temperature range and screening level:

version	temperature	screening
C:	0°C to + 70°C	commercial
J:	– 40°C to + 85°C	industrial
I:	– 40°C to + 85°C	industrial: hybrid
E:	– 40°C to + 85°C	commercial SOIC
K:	– 55°C to + 125°C	high-reliability industrial hybrid
L:	– 55°C to + 125°C	dice
M:	– 55°C to + 125°C	hybrid: high-reliability military
8:	– 55°C to + 125°C	MIL-STD-883 compliant

[2]CLC100 and CLC104A are non-inverting, CLC102 is inverting gain.

[3]Evaluation boards are available for all hybrid and monolithic integrated circuits. Encased and connectorized versions of the CLC103, CLC203, CLC200, CLC201, CLC220, CLC221, CLC231 and CLC104 are available as well. Contact Comlinear or your local Comlinear representative for details.

*Contact the factory for further information.

→ Indicates new products since 1991 databook.

See the individual product data sheets for details.

Package Type	Dual in Line												Surface mount								TO-8	Die
Package Material	Plastic			Cerdip			Ceramic Side Brazed					Metal	Small Outline IC (SOIC)			LCC		Cerpak			Metal	Waffle Pack
Number of Pins	8	14	16	8	14	16	8	14	16	24	40	14	8	14	16	16	20	10	14		12	
CLC103										√												
CLC104												√										
CLC110	√			√			√						√			•						√
CLC114		√			√			√						√		√						√
CLC115		√						√						√								√
CLC200																					√	
CLC201																					√	
CLC203										√												
CLC205																					√	
CLC206																					√	
CLC207																					√	
CLC220																					√	
CLC221																					√	
CLC231																					√	
CLC232																					√	
CLC300										√												
CLC400	√			√			√						√			√						√
CLC401	√			√			√						√			•						√
CLC402	√			•			√						√			•						√
CLC404	√			•			√						√			•						√
CLC406	√			√			√						√			•						√
CLC409	√			•			√						√			√						√
CLC410	√			√			√						√			•						√
CLC411	√			•									√			•						•
CLC412	√			•									•			•						•

√ Existing Package
• Future Package

Package Type	Dual in Line												Surface mount								TO-8	Die
Package Material	Plastic			Cerdip			Ceramic Side Brazed					Metal	Small Outline IC (SOIC)			LCC		Cerpak			Metal	Waffle Pack
Number of Pins	8	14	16	8	14	16	8	14	16	24	40	14	8	14	16	16	20	10	14		12	
CLC414		√			•			√						√			√					√
CLC415		√			•			√						√			•					√
CLC420	√			•			√						√				•					√
CLC422	√			√			√						√				•					√
CLC425	√			•									√				•					√
CLC430	√			√			√						√				•					√
CLC501	√			•			√						√			√	•	√				
CLC502	√			•			√						√				•					
CLC505	√			•			√						√				•	√				√
CLC520		√			•			√						√			•		√			√
CLC522		√						√						√								√
CLC532		√			•			√						√			•					
CLC533			√			•									•		•					
CLC560										√												
CLC561										√												
CLC922											√											
CLC925											√											
CLC935											√											
CLC936											√											
CLC937											√											
CLC940										√												
CLC942										√												

√ Existing Package
• Future Package

Quality and Reliability
Contents

Quality excellence is an approach to business based on understanding the customer's needs, and then striving consistently and efficiently to meet those needs with desired products and services.

Comlinear recognizes that pursuing quality excellence will result in both increased customer and employee satisfaction by achieving higher productivity, improved reliability and increased value.

At Comlinear, quality excellence is implemented through a continuous and committed team approach to quality improvement, from senior management through all employees for all activities of the company.

We elevate quality beyond its typical stature as a military mandated program, and foster an environment where it becomes a pervasive operating attitude. Comlinear's ability to deal with the required elements of a quality program is shown by the continual maintenance of our MIL-STD-1772 facility certification, and our MIL-STD-883 compliant, DESC SMD approved, monolithic and hybrid products.

What makes Comlinear a preferred supplier are our efforts to address the competitive challenge in today's market by focusing on the quality of all of our products and services.

Our commitment to product assurance means that we start with the required systems and then enhance them with the most up-to-date quality assurance techniques available. Tools such as SPC, quality improvement teams, and experimental design are all used in an environment of Total Quality.

Application of these techniques is the responsibility of all managers and employees. These techniques, and the desire for continuous quality improvement, are found in areas ranging from accounting, research and development, and computer services to manufacturing processes and shipment.

The Quality Assurance group supports these efforts by providing technical resources in quality engineering for failure analysis, reliability monitoring, and process improvement. Furthermore, quality levels in manufacturing are continually measured and the information is supplied to the responsible managers.

Comlinear will be pursuing assessment and certification to the International Organization for Standardization (ISO), specifications 9000 and 9001. This effort will solidify Comlinear's commitment to fulfilling customer needs and achieving product and service excellence.

PRODUCTS AND TECHNOLOGIES

Comlinear's hybrid circuit manufacturing is located in our MIL-STD-1772 certified production line in Fort Collins, Colorado. Our capabilities include high density thin film substrate fabrication incorporating high precision, high stability tantalum nitride resistors, gold metalization, and alumina substrates. Monolithic microcircuits are fabricated in the U.S.A. using a high speed complementary bipolar integrated circuit process. This combination has demonstrated an actual failure rate for ICs of less than 1.0 FIT in lifetesting.

Both monolithic and hybrid products are available as MIL-STD-883, industrial or commercial levels. DESC SMDs are available for most of our catalog hybrid and monolithic products. Our monolithic products are also available as MIL-STD-883, S (space) level compliant. Though our hybrid products can be processed to selected K (space) level criteria, the final product would not be compliant or certified to MIL-STD-883 or MIL-M-38534, K level.

ENVIRONMENTAL IMPACT/SAFETY AWARENESS

Comlinear is actively pursuing the elimination of ozone depleting substances (ODS) in its manufacturing processes and is persuading its suppliers to comply with the Montreal Protocol and all U.S Federal regulations.

The flammability rating of commercial, plastic DIP, monolithic products is 94V-0 of the UL-94 Flame Class; this rating is subject to change without notification.

The following section outlines the various flows for both the hybrid and the monolithic product lines and provides additional reliability data.

SPACE LEVEL PRODUCTS

Comlinear has the expertise, product lines and demonstrated reliability to support your space-based systems. In addition, we have the experience and program management necessary to meet the unique demands of processing components to space level MIL-STD-883 or custom flows.

The monolithic product lines have been designed for the robust, reliable assembly and high radiation tolerance necessary for success in the space system environment. Also, a mono-metallic gold wire bonding system is used for superior dependability.

Recognizing the special nature of space programs and the impact of component performance on system capability, we are fully prepared to provide either our standard S Level screening or full custom processing flows to suit your application requirements. Hybrid products can be processed to selected K (space) level criteria, but the final product would not be compliant or certified to MIL-STD-883 or MIL-M-38534, K level. Contact Comlinear for specific information.

Radiation testing has been completed on several Comlinear products at different levels. Our complementary bipolar IC process, for instance, has shown radiation tolerance up to one megarad total dose.

Radiation Test Data Summary*

Part Number	Package Type	Quantity	Date Code	Neutron Irrad. (neutron/cm^2)	Total Dose (krads)	Dose Rate	Result Summary
CLC205	TO-8	5+1Control	8931	None	50, 100 300, 1000	126 rad (Si)/sec	Devices withstood radiation to 1Mrad (Si) with little degradation.
CLC220	TO-8	4+1Control	8508	3.36 x 10^{12}	100, 300 500, 1000	Unknown	No change in ac characteristics. Slight change in dc bias characteristics.
CLC231	TO-8	4		1.2 x 10^{12} 3.2 x 10^{12} 9.9 x 10^{12} 25 x 10^{12} 36 x 10^{12}	None	None	Slight change in dc operating characteristics and distortion. No change in gain and bandwidth.
CLC400 (.054"x.054" TYP die size)	Ceramic side-brazed DIP	Controls	8817	None	10, 30, 100 300, 1000	140 rad (Si)/sec	Negligible degradation to 1000 krad specification. Should meet specifications to 3000krad.
CLC401 (.054"x.054" TYP die size)	Ceramic side-brazed DIP			1.85 x 10^{12}	None	None	Very little change in the small signal frequency response over a wide gain range.
CLC401 (.039"x.039" TYP die size)	Ceramic side-brazed DIP	4	9136	None	10, 30, 50 100	570 rad (Si)/min	No degradation of test limits up to 100 krads.
CLC501	Plastic DIP	2		None	5, 10, 15 20, 25	50 rad/hr	No degradation of gain at all; slight degradation of bandwidth at initial radiation exposure only.
CLC925	Ceramic side-brazed DIP	2		None	0.5, 1, 1.5 2, 5, 10, 20 38, 40, 50 56	Unknown	Performance is virtually constant from 0 to 56 krad total dose. Any trend versus total dose is obscured by test repeatability.

*Detail Reports Available

Date: 1/93

Standardized Military Drawings (SMD)

Comlinear is involved in and supports a drawing (detail specification) standardization program administered by the Defense Electronics Supply Center (DESC). This program covers all Comlinear products compliant to MIL-STD-883 paragraph 1.2.1, MIL-M-38510 and MIL-H-38534 for monolithic and hybrid devices.

The following listing identifies those models which have DESC (SMD) approval or are in process. Comlinear will, upon device qualification, apply for and seek SMD approval of all products to be compliant to military standards.

Contact Comlinear for new releases or any models currently in-process which are not listed herein.

SMD Number	CLC Part Number
5962-89594	CLC231
5962-89858	CLC206
5962-89910	CLC200
5962-89911	CLC220
5962-89970	CLC400
5962-89973	CLC401
5962-89974	CLC501
5962-89975	CLC110
5962-90600	CLC410
5962-90756*	CLC560
5962-90833	CLC201
5962-90835	CLC205
5962-90836	CLC221
5962-90925	CLC500
5962-90977	CLC207
5962-90993	CLC505
5962-90994	CLC404
5962-90995	CLC925
5962-91665	CLC232
5962-91666*	CLC422
5962-91693	CLC414
5962-91694	CLC520
5962-91743	CLC502
5962-91758	CLC420
5962-92004	CLC406
5962-92030	CLC430
5962-92033	CLC402
5962-92034	CLC409
5962-92035*	CLC532
5962-92039*	CLC935
5962-92339	CLC114
5962-93055*	CLC415

CLC Part Number	SMD Number
CLC110	5962-89975
CLC114	5962-92339
CLC200	5962-89910
CLC201	5962-90833
CLC205	5962-90835
CLC206	5962-89858
CLC207	5962-90977
CLC220	5962-89911
CLC221	5962-90836
CLC231	5962-89594
CLC232	5962-91665
CLC400	5962-89970
CLC401	5962-89973
CLC402	5962-92033
CLC404	5962-90994
CLC406	5962-92004
CLC409	5962-92034
CLC410	5962-90600
CLC414	5962-91693
CLC415	5962-93055*
CLC420	5962-91758
CLC422	5962-91666*
CLC430	5962-92030
CLC500	5962-90925
CLC501	5962-89974
CLC502	5962-91743
CLC505	5962-90993
CLC520	5962-91694
CLC532	5962-92035*
CLC560	5962-90756*
CLC925	5962-90995
CLC935	5962-92039*

* Release Pending

RELIABILITY PREDICTIONS

This listing provides mean time between failure (MTBF) rate prediction analysis, calculated in accordance with MIL-HDBK-217E. The stated values are for MIL-STD-883, B level, H level, or Comlinear M level processed versions. For monolithic products, the number range of transistors has been shown; these products are achieving a continuous tested FIT (Failures in Time) rate of <1.0 fails per billion device hours.

Part[1] Number	MTBF[1] (million hours)	Number of Transistors[2]	Product Process[3]
CLC103	1.76		H
CLC110	59.5	< 100	M
CLC114	44.8	< 100	M
CLC115	13.4	< 100	M
CLC200	1.47		H
CLC201	1.30		H
CLC203	1.68		H
CLC205	1.77		H
CLC206	2.06		H
CLC207	1.77		H
CLC220	1.42		H
CLC221	1.30		H
CLC231	1.65		H
CLC232	1.65		H
CLC400	42.1	< 100	M
CLC401	51.4	< 100	M
CLC402	56.3	< 100	M
CLC404	75.3	< 100	M
CLC406	88.8	< 100	M
CLC409	70.0	< 100	M
CLC410	50.3	< 100	M
CLC411	15.7	< 100	M
CLC412	51.7	< 100	M
CLC414	30.9	101 - 300	M
CLC415	23.2	101 - 300	M
CLC420	90.9	< 100	M
CLC422	56.3	< 100	M
CLC425	59.0	< 100	M
CLC430	20.0	< 100	M
CLC501	40.6	< 100	M
CLC505[4]	68.4	< 100	M
CLC520	24.7	< 100	M
CLC522	12.2	< 100	M
CLC532	27.8	< 100	M
CLC533	10.8	101 - 300	M
CLC560	1.64		H
CLC561	1.64		H
CLC922	see datasheet plot		H
CLC925	see datasheet plot		H
CLC935	see datasheet plot		H
CLC936	see datasheet plot		H
CLC940	1.15		H
CLC942	2.22		H

[1]Based on MIL-STD-883, B Level, H level or our M level versions; per MIL-HDBK-217E; Ground Fixed (GF) at 70° C case still air (hybrid), GF at 25° C ambient still air (monolithic). [2]For CLC hybrid products, the number of transistors is not listed due to further transistor attributes beyond the scope of this listing; these attributes should be discussed with Comlinear personnel directly. [3]H = hybrid; M = monolithic. [4]Rp=33kΩ

Thermal Resistances[1]

Package / CLC Pkg Code / CLC Part Number	Plastic DIP P θ_{JA}	Plastic SOIC E θ_{JA}	Ceramic side-brazed DIP D θ_{JA}, θ_{JC}	CERDIP B θ_{JA}, θ_{JC}
CLC110	100	125	100, 28	120, 50
CLC114	75	75	75, 28	TBD
CLC115	75	75	75, 28	
CLC400	100	125	100, 28	120, 50
CLC401	100	125	100, 28	120, 50
CLC402	100	125	100, 28	100, 50
CLC404	100	125	100, 28	100, 50
CLC406	100	125	100, 28	120, 50
CLC409	100	125	100, 28	100, 50
CLC410	100	125	100, 28	100, 50
CLC411	100	125		TBD
CLC412	100	125		100, 50
CLC414	75	75	75, 28	TBD
CLC415	75	75	75, 28	TBD
CLC420	100	125	100, 28	100, 50
CLC422	100	125	100, 28	100, 50
CLC425	100	125		120, 50
CLC430	100	125	100, 28	100, 50
CLC501	100	125	100, 28	100, 50
CLC502	100	125	100, 28	100, 50
CLC505[2]	100	125	100, 28	100, 50
CLC520	75	75	75, 28	TBD
CLC522	75	75	TBD	
CLC532	75	75	75, 28	TBD
CLC533	75	75		TBD

[1]Typical, °C/W, ambient temperature 25°C, still air
[2]R_p=33kΩ

ESD Sensitivity

Comlinear's products are Electro Static Discharge (ESD) sensitive and are designed, processed, handled and packaged with consideration to both optimal ESD protection and product high performance.

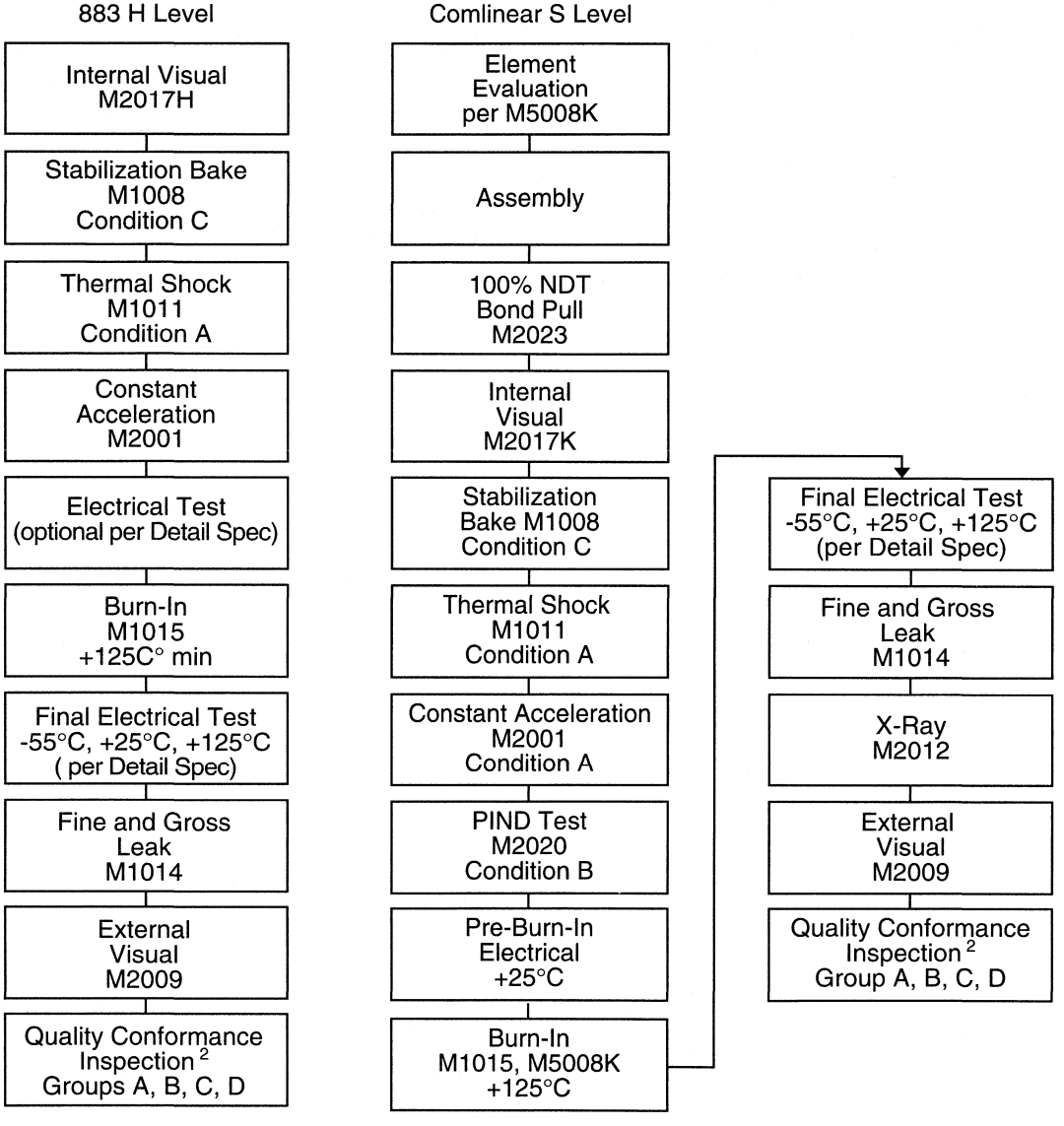
Ratings listed below are based on criteria set forth per MIL-STD-883, Method 3015. Device ESD classifications are:

Class 1:	0 to 1999 volts
Class 2:	2000 to 3999 volts
Class 3:	4000 volts and above

Part Number	Class	Part Number	Class
CLC103	1	CLC411	1
CLC104	1	CLC412	1
CLC110	1*	CLC414	1*
CLC114	1*	CLC415	1*
CLC115	3*	CLC420	2*
CLC200	1	CLC422	1*
CLC201	1	CLC425	1
CLC203	1	CLC430	3*
CLC205	1	CLC501	1*
CLC206	1	CLC502	1*
CLC207	1	CLC505	1*
CLC220	1	CLC520	1*
CLC221	1	CLC522	1
CLC231	1*	CLC532	1*
CLC232	1	CLC533	1
CLC300	1	CLC560	1
CLC400	1*	CLC561	1
CLC401	1*	CLC922	1
CLC402	2*	CLC925	1
CLC404	1*	CLC935	1
CLC406	1*	CLC936	1
CLC409	1	CLC940	1
CLC410	1*	CLC942	1

*These parts have been tested and classified; others are considered Class 1 by design similarity. All products are marked with one ESD triangle symbol.

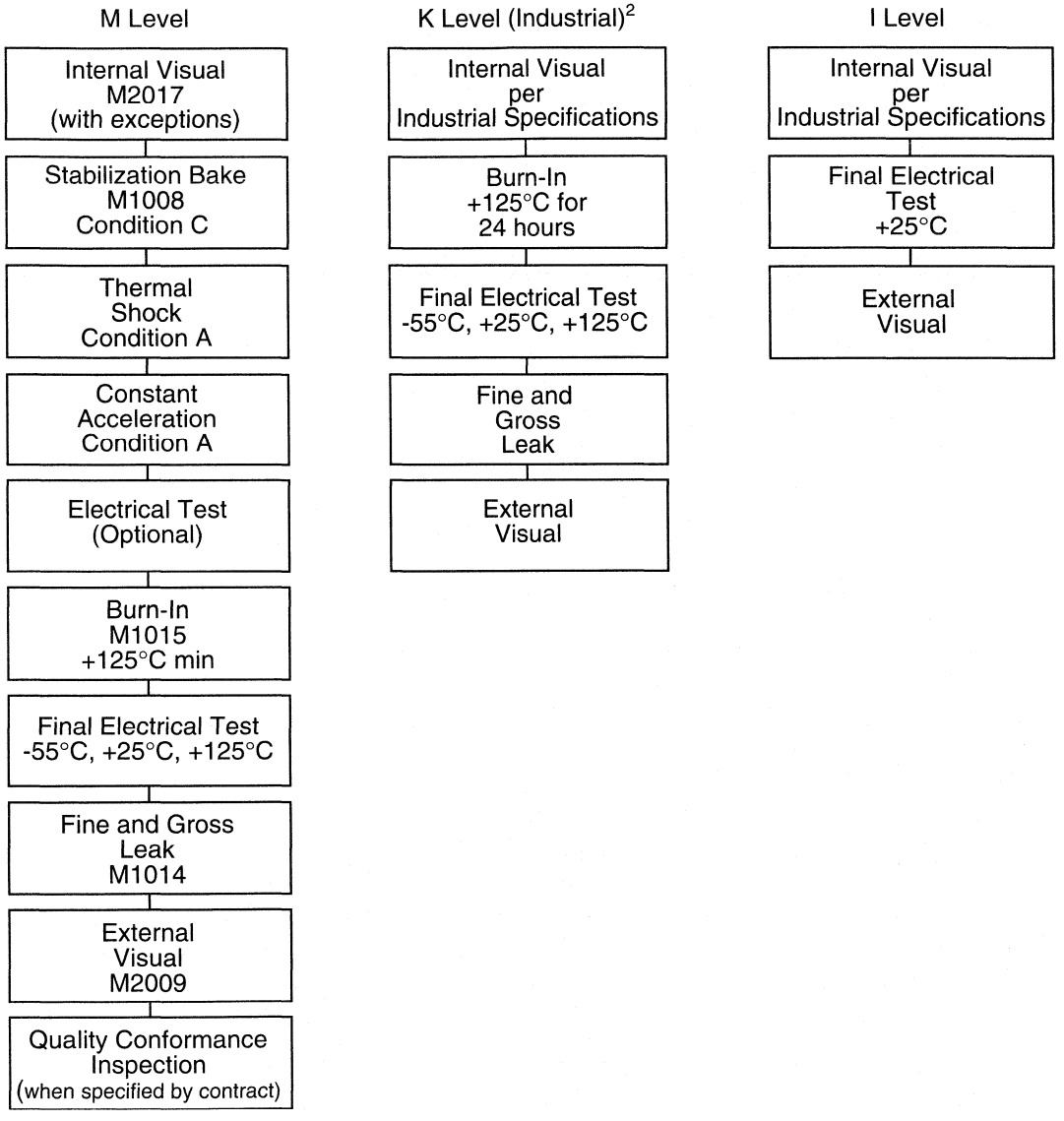
HYBRID



[1]All processing flows are based on MIL-STD-883, MIL-H-38534 and are subject to change to correspond to current revisions. MXXXX references are to test methods in MIL-STD-883.

[2]Quality Conformance Inspection is per MIL-H-38534, option 1 (in-line).

HYBRID

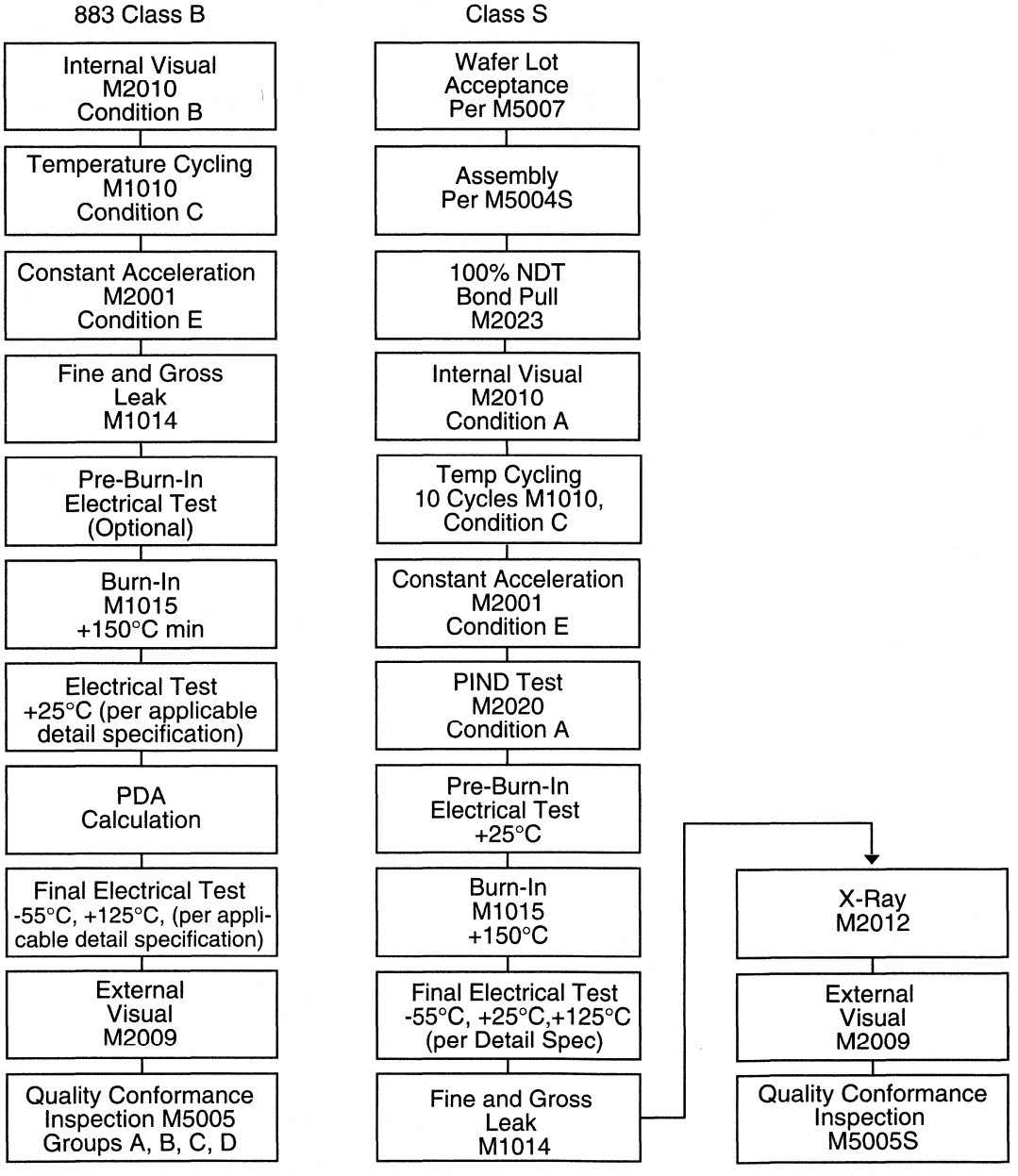


[1]All processing flows are based on MIL-STD-883, MIL-H-38534 and are subject to change to correspond to current revisions. MXXXX references are to test methods in MIL-STD-883.

[2]Comlinear identification of an industrial grade flow. Not a 1772 "S Level" equivalent.

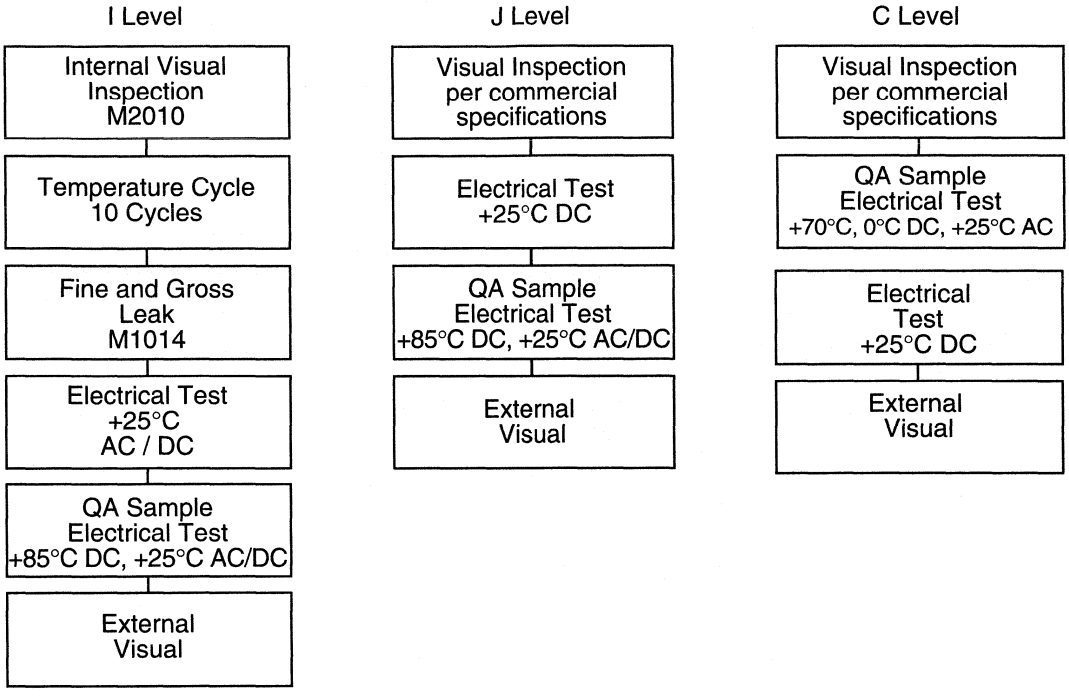
PROCESS FLOWS[1]

MONOLITHIC



[1]All processing flows are based on MIL-STD-883 or MIL-M-38510 and are subject to change to correspond to current revisions. MXXXX references are to test methods in MIL-STD-883.

MONOLITHIC



[1]All processing flows are based on MIL-STD-883 or MIL-M-38510 and are subject to change to correspond to current revisions. MXXXX references are to test methods in MIL-STD-883.

Quality Conformance Inspection
HYBRID

In-line Group A will be performed on inspection lots less than 500 pieces. Should end of line sampling techniques be utilized, the table below will be followed. Refer to detail specification for electrical tests within each subgroup.

Group A, H Level

Subgroup	Parameters	Sample (Acc)
1	Static Test +25°C	116 (0)
2	Static Test at maximum operating temperature	76 (0)
3	Static Test at minimum operating temperature	45 (0)
4	Dynamic Test +25°C	116 (0)
5	Dynamic Test at maximum operating temperature	76 (0)
6	Dynamic Test at minimum operating temperature	45 (0)
7	Functional Test +25°C	116 (0)
8	Functional Tests at maximum and minimum operating temperatures	76 (0)
9	Switching Test +25°C	116 (0)
10	Switching Test at maximum operating temperature	76 (0)
11	Switching Test at minimum operating temperature	45 (0)

HYBRID

Group B, In-Line

Test	Method	Condition	Sample (Acc)
Subgroup1 Physical Dimensions	2016	Monthly	2 (0)
Subgroup 3 Resistance to Solvents	2015	Each Ink Lot	4 (0)
Subgroup 4 Internal Visual/Mechanical	2014	Monthly	1 (0)
Subgroup 5 Bond Strength 1. Thermocompression 2. Ultrasonic or Wedge	2011	 C or D, Weekly C or D, Weekly	2 (0)
Subgroup 6 Die Shear	2019	First lot and major change. Performed as part of Group C.	2 (0)
Subgroup 7 Solderability	2003	Solder Temperature 245 ± 5°C each package lot. Performed as part of Receiving Inspection.	1 (0)
Subgroup 8 Seal Test	1014	Performed 100%	100%

Group C, In-Line

Test	Method	Condition	Sample (Acc)
Subgroup1 External Visual Temperature Cycle or Thermal Shock Mechanical Shock or Constant Acceleration Seal Test Visual Exam End Point Electricals	 2009 1010 1011 2002 2001 1014 1010/1011	 C minimum A minimum B,Y_1 direction A,Y_1 direction +25°C DC	15 (0)
Subgroup 2 Life Test End Point Electricals	1005	1000 hours at 125°C(minimum) +25°C DC	22 (0)
Subgroup 3 Internal Water Vapor	1018	5000 ppm H_20 Maximum	3 (0) or 5 (1)
Subgroup 4 Wirebond Strength	2011	D	22 (0) wires[1]
Subgroup 5 Die Shear	2019		22 (0) die

[1] Class H, 45 (0) wires, Condition S.

HYBRID

Group D, H Level, In-Line[1] (Option1)

Test	Method	Condition	Quantity Accept No.
Thermal Shock	1011	C	3 (0)
High Temperature Bake	1008	Per Time/Temp in MIL-H-38534	3 (0)
Lead Integrity	2004	B2	3 (0)
Seal	1014	A_4, unlidded cases	3 (0)

[1]Each package lot as part of incoming inspection.

Quality Conformance Inspection
MONOLITHIC

Group A, Classes B and S[1]

Subgroup	Parameters	Sample (Acc)
1	Static Test +25°C	116 (0)
2	Static Tests at maximum rated operating temperature	116 (0)
3	Static Tests at minimum rated operating temperature	116 (0)
4	Dynamic Test +25°C	116 (0)
5	Dynamic Tests at maximum rated operating temperature	116 (0)
6	Dynamic Tests at minimum rated operating temperature	116 (0)
7	Functional Test +25°C	116 (0)
8A	Functional Tests at maximum rated operating temperature	116 (0)
8B	Functional Tests at minimum rated operating temperature	116 (0)
9	Switching Test +25°C	116 (0)
10	Switching Tests at maximum rated operating temperature	116 (0)
11	Switching Tests at minimum rated operating temperature	116 (0)

[1] Refer to detail specification for electrical tests within each subgroup.

MONOLITHIC

Group B, Class B

Test	Method	Condition	LTPD or Sample (Acc)
Subgroup 2 A. Resistance to Solvents	2015		4 (0)
Subgroup 3 A. Solderability	2003	Soldering Temperature of 245 ± 5°C	10 leads
Subgroup 5 A. Bond Strength	2011	D	10 bonds

Group B, Class S

Test	Method	Condition	LTPD or Acceptance Quantity
Subgroup 1 A. Physical Dimensions B. Internal Water Vapor	 2016 1018	 5000 ppm at 100°C	 2 (0) 3 (0) or 5 (1)
Subgroup 2 A. Resistance to Solvents B. Internal Visual and Mechanical C. Bond Strength D. Die Shear	 2015 2013, 2014 2011 2019	 D	 4 (0) 2 (0) 22 (0) wires 3 (0)
Subgroup 3 A. Solderability	 2003		 22 (0) leads
Subgroup 4 A. Lead Integrity B1. Fine Leak B2. Gross Leak C. Lid Torque	 2004 2004 1014 1014 2024	 B2 D (Leadless chip carriers) A2 C1 As applicable	 45 (0)leads 15 (0)pads 5 5 -
Subgroup 5 A. Pre-life test (electrical) B1. Board Check B2. Device Functional Test B3. Steady State Life B4. Device Functional Test C. Post-Life Test (electrical)	Group A, Subgroups 1,2,3 1005 1005 1005 1005 Group A, Subgroups 1,2,3	-55°C, +25°C, +125°C DC B, 500 hours at 150°C -55°C, + 25°C, +125°C DC	5 100% 100% 5 100% 5

(continued on next page)

Group B, Class S

Test	Method	Condition	LTPD or Acceptance Quantity
Subgroup 6			
A. End Point Electrical Test	Per SCD	+25°C AC/DC	15
B. Temperature Cycling	1010	C, 100 cycles per minute	15
C. Constant Acceleration	2001	E, Y1	15
D1. Fine Leak	1014	A2	15
D2. Gross Leak	1014	C1	15
E. End Point Electrical Test	Per SCD	+25°C AC/DC	15

Group C, Class B

Test	Method	Condition	LTPD
Subgroup 1			
A. Steady State Life Test	1005	184 hours at 150°C min or equivalent	5
B. End Point Electricals		+25°C DC	5

MONOLITHIC

Group D, Classes B and S

Test	Methods	Conditions	LTPD or Sample (Acc)
Subgroup 1 A. Physical Dimensions	2016		15
Subgroup 2 A. Lead Integrity B1. Fine Leak[1] B2. Gross Leak[1]	 2004 2004 1014 1014	 B2 D (leadless chip carrier) A2 C1	 15 5 5 5
Subgroup 3 A. Thermal Shock B. Temperature Cycling C. Moisture Resistance D. End Point Electricals E. Visual Exam F1. Fine Leak F2. Gross Leak	 1011 1010 1004 1004, 1010 1014 1014	 B (min), 15 cycles (min) C, 100 cycles (min) +25°C DC A2 C1	 15
Subgroup 4 A. Mechanical Shock B. Vibration, Variable Frequency C. Constant Acceleration[3] D1. Fine Leak D2. Gross Leak E. Visual Exam F. End Point Electricals	 2002 2007 2001 1014 1014 1010,1011	 B (min) A (min) E (min), Y_1 orientation A2 C1 +25°C DC	 15
Subgroup 5 A. Salt Atmosphere B. Visual Exam C1. Fine Leak C2. Gross Leak	 1009 1009 1014 1014	 A (min) A2 C1	 15
Subgroup 6 A. Internal Water Vapor Content	1018	5000 ppm H_2O maximum 100°C	3 (0) or 5 (1)

(continued on next page)

MONOLITHIC

Group D, Classes B and S (continued)

Test	Method	Conditions	LTPD or Sample (Acc)
Subgroup 7 A. Adhesion to Lead Finish[4]	2025		15 leads
Subgroup 8 A. Lid Torque[2]	2024		5 (0)

[1] Seal test (Subgroup 2B) need be performed only on packages that have leads exiting through a glass seal.

[2] Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame lead or package body (i.e., wherever the frit seal establishes hermeticity or package integrity).

[3] Microcircuits which are contained in packages which have an inner seal or cavity perimeter of two inches or more or have a package mass of 5 grams or more, may be tested to condition D (unless otherwise specified).

[4] Adhesion of lead finish not applicabe to leadless chip carriers.

A reliability qualification and monitoring program exists for all Hi-Rel as well as commercial/industrial products. Details of this program and current data for the different product lines are available upon request.

Operational Amplifiers
Contents

General Purpose

Category	Description	Model	−3dB Bandwidth @ Gain (MHz @ V/V)	Settling Time to % Accuracy (nsec to %)	Slew Rate (V/μsec)	Input Offset Voltage		Output		Recommended Gain Range (V_o/V_i)	Package[1]
						At 25°C (mV)	Drift (μV/°C)	Voltage (±V)	Current (±mA)		
±5V Current Feedback	Low Gain	CLC400	200 @ 2	12 to 0.05	700 (NI) 1600 (IN)	2	20	3.5	70	±1 to 8	DIP
	High Gain	CLC401	150 @ 20	10 to 0.1	1200	3	20	3.5	70	±7 to 50	DIP
	High Slew Rate	CLC404	175 @ 6	10 to 0.2	2600	2	30	3.3	70	+2 to +21 −1 to −20	DIP
	Low Power	CLC406	160 @ 6	12 to 0.05	1500	2	30	+3.1, −2.7	70	±1 to ±10	DIP
	Dual Wideband	CLC412	320 @ 2	12 to 0.05	1300	2	30	3.3	70	±1 to 10	DIP
±15V Current Feedback	General Purpose	CLC200	95 @ 20	25 to 0.02	4000	10	35	12	100	±1 to 50	TO-8
	Low Offset	CLC201	95 @ 20	30 to 0.02	4000	0.5	5	12	100	±1 to 50	TO-8
	Low Power	CLC205	170 @ 20	24 to 0.05	2400	3.5	11	12	50	+7 to 50 −1 to −50	TO-8
	General Purpose	CLC206	180 @ 20	22 to 0.05	3400	3.5	11	12	100	+7 to 50 −1 to −50	TO-8
	Low Gain	CLC231	165 @ 2	15 to 0.05	3000	1	10	11	100	±1 to 5	TO-8
	General Purpose	CLC300	85 @ 20	20 to 0.8	3000	10	25	10	100	±1 to 40	DIP
	High-Speed	CLC411	200 @ 2	15 to 0.1	2300	2	30	6.0	70	±1 to 10	DIP
	Low Cost Monolithic	CLC430	45 @ 2	40 to 0.1	2000	2	TBD	13	85	±1 to 10	DIP
±5V Voltage Feedback	Low Gain	CLC420	500 @ 1	18 to 0.01	1100	0.5	4	3.6	70	±1 to 10	DIP
	High Gain	CLC422	200 @ 40	17 to 0.2	2300	0.8	2	3.8	70	±30 to 200	DIP
	Ultra Low Noise	CLC425	90 @ 20	22 to 0.1	350	0.1	2	3.8	90	±10 to 1000	DIP
Quad Amplifiers	Low Power	CLC414	90 @ 6	24 to 0.1	1000	2	30	2.8	70	±1 to 10	DIP
	High Speed	CLC415	160@6	12 to 0.1	1500	2	20	2.6	70	±1 to 10	DIP

[1]Primary package is listed. Other packages exist for many products. See data sheets for details.

Very High Speed

Description	Model	−3dB Bandwidth @ Gain (MHz @ V/V)	Slew Rate (V/μsec)	Rise/Fall Time (nsec)	Settling Time to % Accuracy (nsec to %)	Recommended Gain Range (V_o/V_i)	Supplies		Output		Package[1]
							Voltage (V)	Current (mA)	Voltage (±V)	Current (±mA)	
High Slew Rate	CLC220	190 @ 20	7000	1.9	15 to 0.02	±1 to 50	±5 to 15	30	12	50	TO-8
Low Offset	CLC221	170 @ 20	6500	2.1	18 to 0.02	±1 to 50	±5 to 15	30	12	50	TO-8
High Slew Rate Monolithic	CLC404	175 @ 6	2600	2.0	10 to 0.2	+2 to 21 −1 to −20	±5	11	3.3	70	DIP
Wideband Monolithic	CLC409	350 @ 2	1200	1.3	8 to 0.1	±1 to 10	±5	13.5	3.5	70	DIP
High-Speed	CLC411	200 @ 2	2300	2.3	15 to 0.1	±1 to 10	±10 to 15	70	6.0	70	DIP
High-Gain	CLC422	200 @ 40	2300	2.0	17 to 0.2	±30 to 200	±5	70	3.8	70	DIP

[1]Primary package is listed. Other packages exist for many products. See data sheets for details.

Accurate Settling (≥12-bit accuracy)

Description	Model	Settling Time (nsec)	Settling Accuracy (%)	Settling Step Size (V)	−3dB Bandwidth @ Gain (MHz @ V/V)	Slew Rate (V/μsec)	Rise/Fall Time (nsec)	Output Voltage (±V)	Output Current (±mA)	Recommended Gain Range (V_o/V_i)	Package[1]
14-bit (to ½LSB)	CLC402	25	0.0025	2	175@2	800	2.7	3.5	55	±1 to 8	DIP
14-bit with Output Clamp	CLC502	25	0.0025	2	150@2	800	2.7	3.5	55	±1 to 8	DIP

[1]Primary package is listed. Other packages exist for many products. See data sheets for details.

[2]The CLC502 is recommended for new designs in place of the CLC500.

Low Power

Category (Supply Voltages)	Description	Model	Supply Current (mA)	Power Consumption (mW)	−3dB Bandwidth @ Gain (MHz @ V/V)	Slew Rate (V/μsec)	Output Voltage (±V)	Output Current (±mA)	Settling Time to % Accuracy (nsec to %)	Recommended Gain Range (V_o/V_i)	Package[1]
±5V Single Op Amps	Variable Supply Current	CLC505[3]	1 to 9	10 to 90	100@6	1200	3.3	25	14 to 0.05	+2 to 21 −1 to −20	DIP
	Voltage Feedback	CLC420	4	40	270@1	1100	3.2	70	18 to 0.01	±1 to 10	DIP
	Current Feedback	CLC406	5	50	160@6	1500	+3.1, −2.7	70	12 to 0.05	±1 to 10	DIP
	Dual Wideband	CLC412	10.2	102	320@2	1300	3.3	70	12 to 0.05	±1 to 10	DIP
	High Slew Rate	CLC404	11	110	175@6	2600	3.3	70	10 to 0.2	+2 to 21 −1 to −20	DIP
±5V Quad Op Amps	Low Power	CLC414	8	80	90@6	1100	2.8	70	24 to 0.1	±1 to 10	DIP
	High Speed	CLC415	20	200	160@6	1500	2.6	70	12 to 0.1	±1 to 10	DIP
±15V Single Op Amps	Low Cost	CLC430	11	330	45@2	2000	13	85	40 to 0.1	±1 to 10	DIP
	Low Gain	CLC231	18	540	165@2	3000	11	100	15 to 0.05	±1 to 5	TO-8
	High Gain	CLC205	19	570	170@20	2400	12	50	24 to 0.05	+7 to 50 −1 to −50	TO-8

[1]Primary package is listed. Other packages exist for many products. See data sheets for details.

[3]Specifications shown are for I_{cc} = 3.4mA. See the CLC505 datasheet for performance at other supply current conditions.

Low Offset Voltage/Drift

Description	Model	Input Offset Voltage At 25°C (mV)	Input Offset Voltage Drift (μV/°C)	Input Bias Current At 25°C (μA)	Input Bias Current Drift (nA/°C)	−3dB Bandwidth @ Gain (MHz @ V/V)	Slew Rate (V/μsec)	Settling Time to % Accuracy (nsec to %)	Recommended Gain Range (V_o/V_i)	Output Voltage (V)	Output Current (mA)	Package[1]
Accurate Settling	CLC402	0.5	3	10	100	175@2	800	25 to 0.0025	±1 to 8	3.5	55	DIP
Clamping Amplifier	CLC502	0.5	3	10	100	150@2	800	25 to 0.0025	±1 to 8	3.5	55	DIP
Low Gain Voltage Feedback	CLC420	0.5	5	0.2[4]	4[4]	270@1	1100	18 to 0.01	±1 to 10	3.2	70	DIP
High Gain	CLC422	0.8	2	15	75	200@40	2300	17 to 0.2	±3 to 200	3.8	70	DIP
Ultra Low Noise	CLC425	0.1	2	12	−100	90@20	350	22 to 0.1	±10 to 1000	3.8	90	DIP
General Purpose	CLC201	0.5	5	5	50	95@20	4000	30 to 0.02	±1 to 50	12	100	TO-8
High Drive	CLC203	0.5	5	5	50	160@20	6000	15 to 0.2	±1 to 50	11	200	DIP
High Speed	CLC221	0.5	5	5	50	170@20	6500	18 to 0.02	±1 to 50	12	50	TO-8
Low Gain	CLC231	1.0	10	10	125	165@2	3000	15 to 0.05	±1 to 5	11	100	TO-8

[1]Primary package is listed. Other packages exist for many products. See data sheets for details.

[4]For the CLC420 and CLC424, voltage feedback op amps, these numbers are for offset current, not bias current.

Low Distortion

Description	Model	Harmonic Distortion ($2V_{pp}$) 2nd (dBc)	3rd (dBc)	Frequency (MHz)	Load (Ω)	−3dB Bandwidth @ Gain (MHz @ V/V)	Settling Time to % Accuracy (nsec to %)	Supply Voltages (V)	Output Voltage (±V)	Output Current (±mA)	Package[1]
High Gain	CLC207	−69 −80	−69 −85	20 20	100 200	170@20	24 to 0.05	±5 to 15	12	100	TO-8
Low Gain	CLC232	−69	−69	20	100	270@2	15 to 0.05	±5 to 15	12	75	TO-8
Low Gain, Monolithic	CLC409	−86 −65 −49	−84 −72 −59	5 20 60	100 100 100	350@2	8 to 0.1	±5	3.5	70	DIP
Driver-amp	CLC560	−60 −54	−62 −44	20 100	50 50	215@10	10 to 0.1	±10 to 15	10.5	200	DIP
Driver-amp	CLC561	−59 −52	−62 −60	20 50	50 50	215@10	7 to 0.1	±10 to 15	10.5	200	DIP

[1]Primary package is listed. Other packages exist for many products. See data sheets for details.

High Output Current

Description	Model	Output Current (±mA)	Output Voltage (±V)	−3dB Bandwidth @ Gain (MHz @ V/V)	Large Signal BW Frequency (MHz)	Large Signal BW Output (V_{pp})	Slew Rate (V/μsec)	Settling Time to % Accuracy (nsec to %)	Supplies Voltage (V)	Supplies Current (mA)	Package[1]
High Slew Rate	CLC103	200	11	150@20	80	20	6000	10 to 0.4	±10 to 15	30	DIP
Low Offset	CLC203	200	11	160@20	60	20	6000	15 to 0.2	±10 to 15	30	DIP
Driver-amp	CLC560	200	10.5	215@10	120	10	2600[5]	10 to 0.1	±10 to 15	50	DIP
Driver-amp	CLC561	200	10.5	215@10	150	10	3300[5]	7 to 0.1	±10 to 15	50	DIP
General Purpose	CLC200	100	12	95@20			4000	25 to 0.02	±5 to 15	29	TO-8
Low Offset	CLC201	100	12	95@20	50	20	4000	30 to 0.02	±5 to 15	29	TO-8
General Purpose	CLC206	100	12	180@20	70	20	3400	22 to 0.05	±5 to 15	29	TO-8
Low Distortion	CLC207	100	12	170@20	100	10	2400	24 to 0.05	±5 to 15	25	TO-8
Low Gain	CLC231	100	12	165@20	95	10	3000	15 to 0.05	±5 to 15	18	TO-8
General Purpose	CLC300	100	10	85@20	45	20	3000	20 to 0.8	±5 to 15	24	DIP
Ultra Low Noise	CLC425	90	3.8	90@20	TBD	TBD	350	22 to 0.1	±5	15	DIP
Low Cost, Monolithic	CLC430	85	13	45@2	30	10	2000	40 to 0.1	±5 to 15	11	DIP

[1]Primary package is listed. Other packages exist for many products. See data sheets for details.

[5]The effective slew rate is twice the number shown. See the CLC560 or CLC561 datasheet for details.

Special Functions

Function	Model	Features	−3dB Bandwidth @ Gain (MHz @ V/V)	Settling Time to % Accuracy (nsec to %)	Slew Rate (V/μsec)	Supply Voltage (V)	Recommended Gain Range (V_o/V_i)	Output Voltage (±V)	Output Current (±mA)
Fast Enable/Disable Video Op Amps	CLC410	100nsec enable, 200nsec disable; differential gain/phase 0.01%/0.01°.	200@2	12 to 0.05	700	±5	±1 to 8	3.5	70
	CLC430	100nsec enable, 200nsec disable; differential gain/phase 0.05%/0.01°.	45@2	40 to 0.1	2000	±5 to 15	±1 to 10	13	85
Output Clamping Op Amps	CLC501	User-defined output voltage clamp levels.	75@32	12 to 0.05	1200	±5	+7 to 50 −1 to −50	3.5	70
	CLC502		150@2	25 to 0.0025	800	±5	±1 to 8	3.5	55
Programmable – Supply-Current Op Amp	CLC505[3]	User-variable supply current from 1mA to 9mA[3].	100@6	14 to 0.05	1200	±5	+2 to 21 −1 to 20	3.3	25

[3]Specifications shown are for I_{cc} = 3.4mA. See the CLC505 datasheet for performance at other supply current conditions.

Comlinear Corporation

Fast Settling, High Current Wideband Op Amps

CLC103

APPLICATIONS:

- coaxial line driving
- DAC current to voltage amplifier
- flash A to D driving
- baseband and video communications
- radar and IF processors

FEATURES:

- 80MHz full-power bandwidth ($20V_{pp}$, 100Ω)
- 200mA output current
- 0.4% settling in 10ns
- $6000V/\mu s$ slew rate
- 4ns rise and fall times (20V)

DESCRIPTION:

The CLC103 is a high-power, wideband op amp designed for the most demanding high-speed applications. The wide bandwidth, fast settling, linear phase, and very low harmonic distortion provide the designer with the signal fidelity needed in applications such as driving flash A to Ds. **The 80MHz full-power bandwidth and 200mA output current of the CLC103 eliminate the need for power buffers in most applications;** the CLC103 is an excellent choice for driving large high-speed signals into coaxial lines.

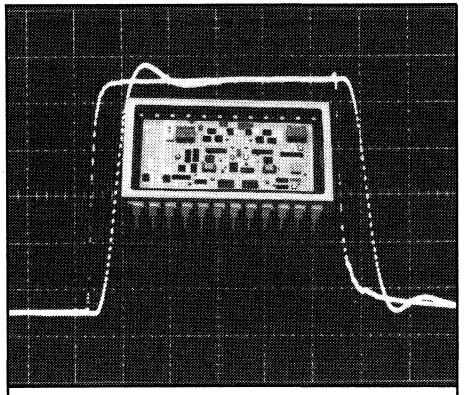
In the design of the CLC103 special care was taken in order to guarantee that the output settle quickly to within 0.4% of the final value for use with ultra fast flash A to D converters. This is one of the most demanding of all op amp requirements since settling time is affected by the op amp's bandwidth, passband gain flatness, and harmonic distortion. This high degree of performance ensures excellent performance in many other demanding applications as well.

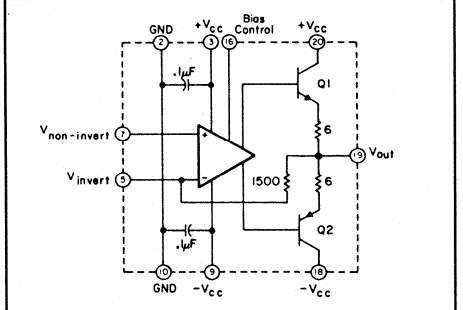
The dynamic performance of the CLC103 is based on Comlinear's proprietary op amp topology. This new design provides performance far beyond that available from conventional op amp designs; unlike conventional op amps where optimum gain-bandwidth product occurs at a high gain, minimum settling time at a gain of −1, and maximum slew rate at a gain of +1, the Comlinear design provides consistent, predictable performance across its entire gain range. For example, the table below shows how **the −3dB bandwidth remains nearly constant over a wide range of gains.** And since the amplifier is inherently stable, no external compensation is required. The result is shorter design time and the ability to accommodate design changes (in gain, for example) without loss of performance or redesign of compensation circuits.

The CLC103 is constructed using thin film resistor/bipolar transistor technology. The CLC103AI is specified over a temperature range of – 25°C to +85°C, while the CLC103AM is specified over a range of – 55°C to +125°C and is screened to Comlinear's M Standard for high reliability applications. Both devices are packaged in 24-pin ceramic DIPs.

Typical Performance

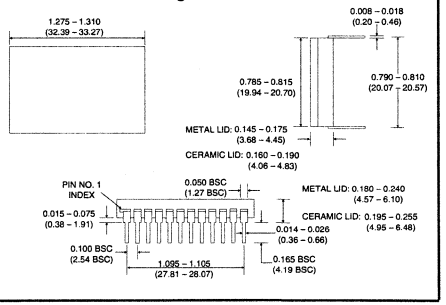
parameter	gain setting +4	+20	+40	−4	−20	−40	units
−3dB bandwidth	230	150	130	155	145	125	MHz
rise time (20V)	4	4	4	4	4	4	ns
slew rate	6	6	6	6	6	6	V/ns
settling time (0.4%)	10	10	12	10	10	12	ns





CLC103 Equivalent Circuit Diagram
(all undesignated pins are internally unconnected)

Package Dimensions



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DS103.05

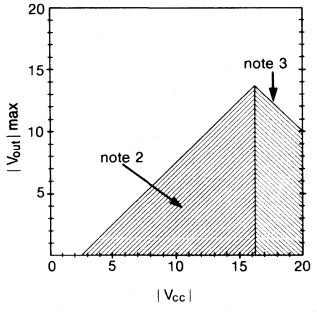
January 1993

Electrical Characteristics ($A_V = +20$, $V_{CC} = \pm 15V$, $R_L = 100\Omega$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature [1]	CLC103AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature [1]	CLC103AI	+25°C	−25°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
* −3dB bandwidth	$V_{out} < 4V_{pp}$	150	>125	>135	>120	MHz	SSBW
gain flatness	$V_{out} < 4V_{pp}$						
* peaking	0.1 to 50MHz	0.1	<0.6	<0.3	<0.3	dB	GFPL
* peaking	>50MHz	0.2	<1.5	<0.6	<0.6	dB	GFPH
* rolloff	at 100MHz	—	<0.4	<0.6	<0.8	dB	GFR
group delay	to 75MHz	3.0	—	—	—	ns	GD
linear phase deviation	to 75MHz	1	<3	<2	<4	°	LPD
reverse isolation - non-inverting	to 150MHz	55	>45	>45	>45	dB	RINI
TIME DOMAIN RESPONSE							
rise and fall time	5V step	2.3	<2.8	<2.6	<2.9	ns	TRS
	20V step	4	<5	<5	<5	ns	TRL
settling time to 0.4%	10V step	10	<25	<20	<25	ns	TSP
overshoot	5V step	5	<15	<10	<10	%	OS
slew rate (overdriven input)		6	>5	>5	>5	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		30	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
* 2nd harmonic distortion	$2V_{pp}$, 20MHz	−48	<−40	<−40	<−40	dBc	HD2
* 3rd harmonic distortion	$2V_{pp}$, 20MHz	−48	<−40	<−40	<−40	dBc	HD3
equivalent input noise							
noise floor	>100kHz	−158	<−152	<−152	<−152	dBm(1Hz)	SNF
integrated noise	1kHz to 100MHz	28	<56	<56	<56	μV	INV
noise floor	>5MHz	−158	<−152	<−152	<−152	dBm(1Hz)	SNF
integrated noise	5MHz to 100MHz	28	<56	<56	<56	μV	INV
STATIC, DC PERFORMANCE							
* input offset voltage		10	<30	<25	<30	mV	VIO
average temperature coefficient		35	<120	<120	<120	μV/°C	DVIO
* input bias current	non-inverting	10	<40	<30	<40	μA	IBN
average temperature coefficient		20	<125	<125	<125	nA/°C	DIBN
* input bias current	inverting	20	<110	<60	<110	μA	IBI
average temperature coefficient		250	<500	<500	<500	nA/°C	DIBI
* power supply rejection ratio		54	>45	>45	>45	dB	PSRR
common mode rejection ratio		38	>30	>30	>30	dB	CMRR
* supply current	no load	30	<36	<34	<36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	>100	>100	>100	kΩ	RIN
	capacitance	2.4	<3	<3	<3	pF	CIN
output impedance	at DC	—	<0.1	<0.1	<0.1	Ω	RO
	at 100MHz	2, 45	—	—	—	Ω, nH	ZO
output voltage range	no load	—	>±11	>±11	>±11	V	VO

Absolute Maximum Ratings

Output Voltage Limit



supply voltage (V_{CC})	±20V
output current	±200mA
thermal resistance (θ_{CA})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
	AM: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

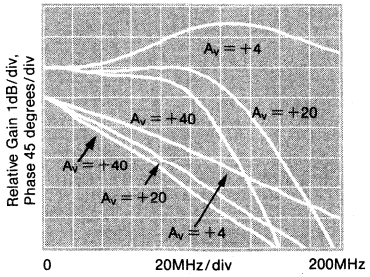
***note 1:** Parameters preceded by an * are the final electrical test parameters and are 100% tested. AM units are tested at – 55°C, +25°C, and +125°C. AI units are tested only at +25°C although their performance is guaranteed at – 25°C and +85°C as indicated above.

note 2: This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10%, maximum input voltage may be as large as twice the maximum. V_{cm} should never exceed ±5V. (V_{cm} is the voltage at the non-inverting input, pin 7.)

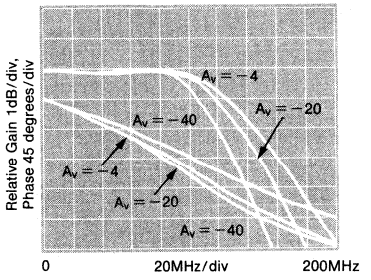
note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{CC} is ±15V.

Typical Performance Characteristics ($A_v = +20$, $V_{cc} = \pm 15V$, $R_L = 100\Omega$)

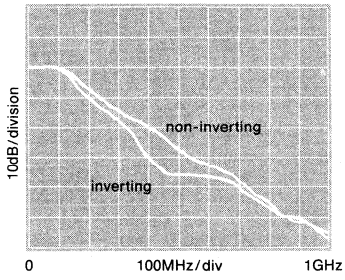
Non-Inverting Gain and Phase



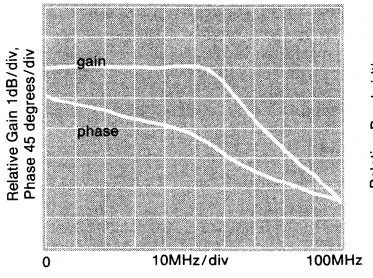
Inverting Gain and Phase



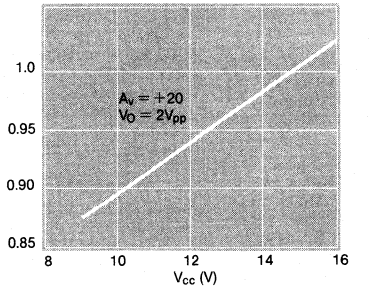
Broadband Inverting and Non-Inverting Gain



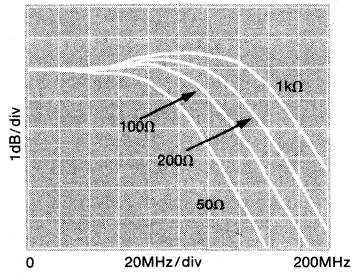
Large Signal Gain and Phase



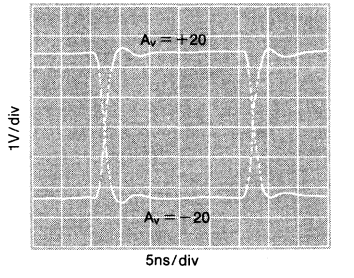
Relative Bandwidth vs. V_{cc}



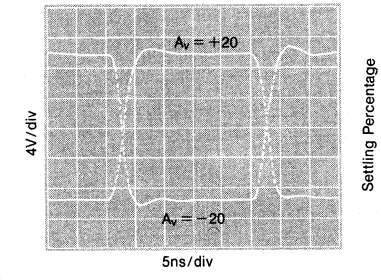
Gain vs. Frequency for Various Loads



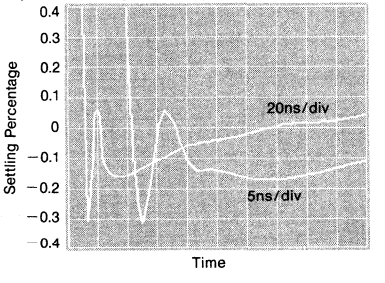
Small Signal Pulse Response (Inv, Non-Inv)



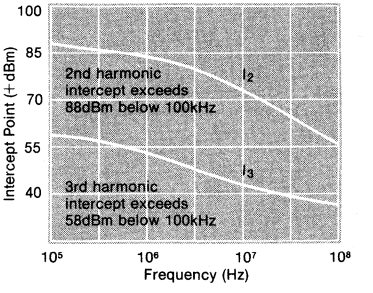
Large Signal Pulse Response (Inv, Non-Inv)



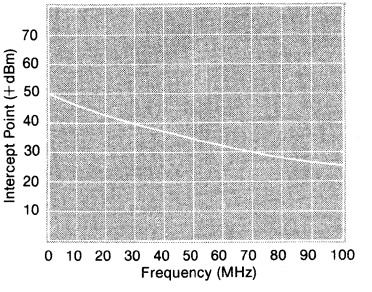
Settling Time



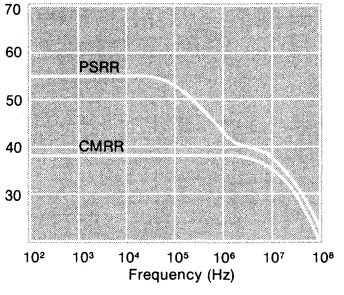
2nd and 3rd Harmonic Distortion Intercept



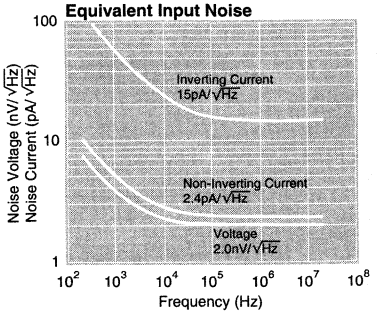
2-Tone 3rd Order Intermod. Intercept

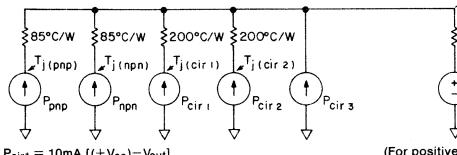


CMRR and PSRR



Equivalent Input Noise





$P_{cir1} = 10mA\,[(+V_{cc}) - V_{out}]$
$P_{cir2} = 10mA\,[V_{out} - (-V_{cc})]$
$P_{cir3} = I_C\,[(+V_{cc}) - (-V_{cc})]$ where $I_C = 10mA$ at $\pm 15V$
$P_{XXX} = I_{col}\,[(\pm V_{cc}) - V_{out} - I_{col}\,(R_{col} + 6)]$ where $I_{col} = V_{out}/R_{load}$ or 9mA, whichever is greater. (Include R_f in R_{load}.)

(For positive V_{out} and V_{cc}, P_{XXX} is the power in the npn device. For negative V_{out} and V_{cc}, this power is in the pnp device.)
R_{col} is an external resistor (22 ohms recommended) between the xxx collector and $\pm V_{cc}$.
$T_{j\,(pnp)} = (P_{pnp})\ 85°C/W + (P_{total})\ \theta_{ca} + T_{ambient}$, similar for $T_{j\,(npn)}$.
$T_{j\,(cir1)} = (P_{cir1})\ 200°C/W + (P_{total})\ \theta_{ca} + T_{ambient}$, similar for $T_{j\,(cir2)}$.

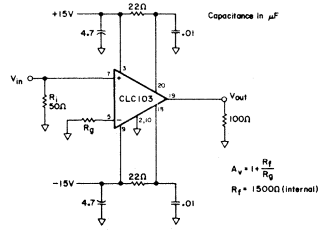


Figure 1: recommended non-inverting gain circuit

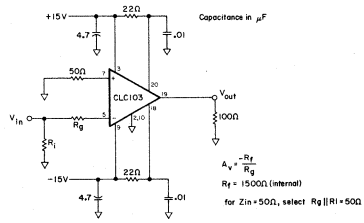


Figure 2: recommended inverting gain circuit

Test fixture layout artwork is available upon request.

CLC103 Operation

The CLC103 is based on Comlinear's proprietary op amp topology, a unique design which uses current feedback instead of the usual voltage feedback. This design provides dynamic performance far beyond that previously available, yet it is used basically the same as the familiar voltage-feedback op amp (see the gain equations above). A complete discussion of current feedback is given in application note AN300-1.

Layout Considerations

To obtain optimum performance from any circuit operating at high frequencies, good PC layout is essential. Fortunately, the stable, well-behaved response of the CLC103 makes operation at high frequencies less sensitive to layout than is the case with other wideband op amps, even though the CLC103 has a much wider bandwidth.

In general, a good layout is one which minimizes the unwanted coupling of a signal between nodes in a circuit. A continuous ground plane from the signal input to output on the circuit side of the board is helpful. Traces should be kept short to minimize inductance. If long traces are needed, use microstrip transmission lines which are terminated in their characteristic impedance. At some high-impedance nodes, or in sensitive areas such as near pin 5 of the CLC103, stray capacitance should be kept small by keeping nodes small and removing ground plane directly around the node.

The $\pm V_{cc}$ connections to the CLC103 are internally bypassed to ground with 0.1μF capacitors to provide good high-frequency decoupling. It is recommended that 1μF or larger tantalum capacitors be provided for low-frequency decoupling. The 0.01μF capacitors shown at pins 18 and 20 in figures 1 and 2 should be kept within 0.1" of those pins. A wide strip of ground plane should be provided for a signal return path between the load-resistor ground and these capacitors.

Since the layout of the PC board forms such an important part of the circuit, much time can be saved if prototype amplifier boards are tested early in the design stage. Encased/connectorized amplifiers are available from Comlinear.

Settling Time, Offset, and Drift

After an output transition has occurred, the output settles very rapidly to the final value and no change occurs for several microseconds. Thereafter, thermal gradients inside the CLC103 will cause the output to begin to drift. When this cannot be tolerated, or when the initial offset voltage and drift is unacceptable, the use of a composite amplifier is advised.

A composite amplifier can also be referred to as a feed-forward amplifier. Most feed-forward techniques such as those used in the vast majority of wideband op amps, involve the use of a wideband AC-coupled channel in parallel with a low-bandwidth, high-gain DC-coupled amplifier. For the composite amplifier suggested for use with the CLC103, the CLC103 replaces the wideband AC-coupled amplifier and a low-cost monolithic op amp is used to supply high open-loop gain at low frequencies. Since the CLC103 is strictly DC coupled throughout, crossover distortion of less than 0.01dB and 1° results.

For composite operation in the non-inverting mode, the circuit in figure 1 should be modified by the addition of the circuit shown in figure 3. For inverting operation, modify the circuit in figure 2 by the addition of the circuit in figure 4. Keep all resistors which connect to the CLC103 within 0.2" of the CLC103 pins. The other side of these resistors should likewise be as close to U1 as possible. For good overall results, U1 should be similar to the LF356; this gives 5μV/°C input offset drift and the crossover frequency occurs at about 2MHz. Since U1 has a feedback network composed of $R_a + R_b$ and a 15kΩ resistor, which is in parallel with R_g and the internal 1.5kΩ feedback resistor of the CLC103, R_b must be adjusted to match the feedback ratios of the two networks. This is done by driving the composite amplifier with a 70kHz square wave large enough to produce a transition from +5V to −5V at the CLC103 output and adjusting R_b until the output of U1 is at a minimum. R_a should be about $9.5R_g$ for best results; thus, R_b should be adjusted around the value of $0.5R_g$.

Bias Control

In normal operation, the bias control pin (pin 16) is left unconnected. However, if control over the bias of the amplifier is desired, the bias control pin may be driven with a TTL signal; a TTL high level will turn the amplifier off.

Distortion and Noise

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the CLC103. First, convert the output voltage V_O to $V_{rms} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{rms}^2))$ to get the output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below the level of P, as will the two-tone third order intermodulation products. These approximations are useful for P<−1dB compression levels.

Approximate noise figure can be determined for the CLC103 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high-frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly-qualified applications engineers to provide technical and design assistance.

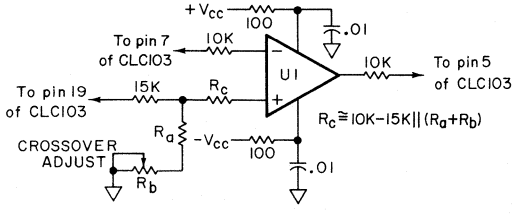


Figure 3: non-inverting gain composite amp to be used with figure 1 circuit

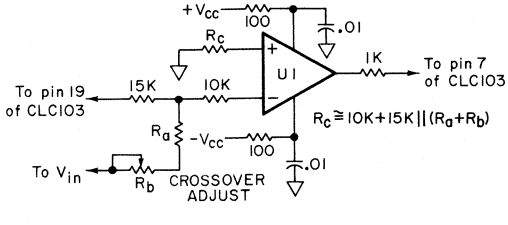


Figure 4: inverting gain composite amplifier to be used with figure 2 circuit

Comlinear Corporation

Fast Settling, Wideband Operational Amplifiers

CLC200

APPLICATIONS:
- fast, precision A to D, D to A conversion
- baseband and video communications
- radar, sonar, IF processors
- laser drivers, photodiode preamps
- graphic CRT composite video drive amp

FEATURES:
- −3dB bandwidth of 95MHz
- 0.1% settling in 18ns
- 4000V/μs slew rate
- low distortion, linear phase
- 3.6ns rise and fall times

DESCRIPTION:

The CLC200 operational amplifier achieves performance far superior to that of other high performance op amps. A proprietary Comlinear design provides a **bandwidth of DC-95MHz and an unprecedented settling time of 18nsec to 0.1%.** And since thermal tail has been eliminated, the CLC200 can be depended upon to settle fast and solidly maintain its level. Drive capability is also impressive at $24V_{pp}$ and 100mA.

Using the CLC200 is as easy as adding power supplies and a gain-setting resistor. The result is reliable, consistent performance because such characteristics as bandwidth and settling time are virtually independent of gain setting. Unlike conventional op amp designs where the optimum gain-bandwidth product occurs at a high gain, minimum settling time at a gain of −1, maximum slew rate at a gain of +1, et cetera, the CLC200 offers predictable response at gain settings from ±1 to ±50. This, coupled with consistent performance from unit to unit with **no external compensation**, makes the CLC200 a real time and cost-saver in design and production situations alike.

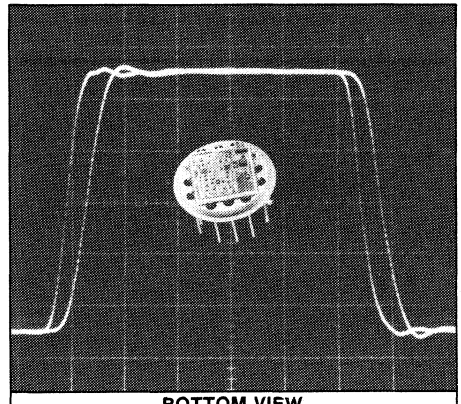
Minimizing settling time was a design goal of the CLC200. Settling time is one of the most demanding of all op amp requirements since it is affected by the op amp's bandwidth, gain flatness, and harmonic distortion. The result of this effort is an amplifier fast enough for the most demanding high speed D to A converters and "flash" A to D converters.

The superior slew rate and rise and fall times of the CLC200 make it an ideal amplifier for a broad range of pulse, analog, and digital applications. Flat gain and phase response from DC to beyond 50MHz ensure distortion levels well below those of other op amps. A **full power bandwidth of 20MHz** eliminates the need for power buffers in many applications.

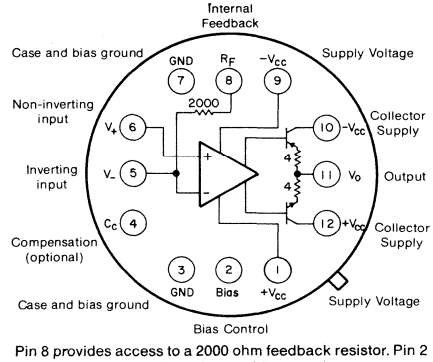
The CLC200 is constructed using thin film resistor/bipolar transistor technology. The CLC200AI is specified over a temperature range of −25°C to +85°C, while the CLC200A8C is specified over a range of −55°C to +125°C and is fully compliant with MIL-STD-883, Level B. Both devices are packaged in 12-pin metal TO-8 cans. The DESC SMD number is 5962-89910.

Typical Performance

	gain setting						
parameter	+2	+20	+50	−2	−20	−50	units
−3dB bandwidth	150	95	75	100	95	90	MHz
rise time (20V)	—	4	5	4	4	4	ns
slew rate	4	4	4	4	4	4	V/ns
settling time (0.1%)	—	18	23	18	18	23	ns

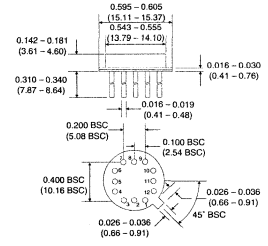


BOTTOM VIEW



Pin 8 provides access to a 2000 ohm feedback resistor. Pin 2 allows the user to reduce the amplifier supply current or to turn the amplifier off completely.

Package Dimensions



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DS200.06

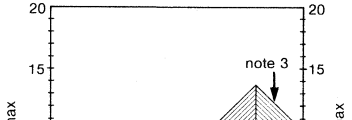
January 1993

Electrical Characteristics (A_V=+20; V_{cc}=±15V; R_L = 200Ω; R_f = 2000Ω)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	CLC200AI[1]	+25°C	–25°C	+25°C	+85°C		
Ambient Temperature	CLC200A8[1]	+25°C	–55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
* –3dB bandwidth	V_{out}<2V_{pp}	95	> 85	> 85	> 80	MHz	SSBW
gain flatness at	V_{out}<2V_{pp}						
* peaking	0.1 to 25MHz	0	< 0.4	< 0.3	< 0.4	dB	GFPL
* peaking	>25MHz	0.2	< 0.8	< 0.6	< 1.0	dB	GFPH
* rolloff	at 50MHz	—	< 0.6	< 0.4	< 0.6	dB	GFR
group delay	to 50MHz	4.2 ± 0.5	—	—	—	ns	GD
linear phase deviation	to 50MHz	1	< 2	< 2	< 2	°	LPD
reverse isolation	to 50MHz						
non-inverting		60	> 50	> 50	> 50	dB	RINI
inverting		45	> 35	> 35	> 35	dB	RIIN
TIME DOMAIN RESPONSE							
rise and fall time	2V step	3.6	< 4.1	< 4.1	< 4.4	ns	TRS
	20V step	4	< 5	< 5	< 6	ns	TRL
settling time to .02%	10V step[4]	25	—	—	—	ns	TSP
to .1%	10V step[4]	18	< 25	< 25	< 25	ns	TS
overshoot	10V step	5	< 12	< 10	< 10	%	OS
slew rate (overdriven input)		4	> 3	> 3	> 3	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		25	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
*2nd harmonic distortion	2V_{pp}, 20MHz	–52	< –45	< –45	< –45	dBc	HD2
*3rd harmonic distortion	2V_{pp}, 20MHz	–58	< –50	< –50	< –50	dBc	HD3
equivalent noise input							
noise floor	>100kHz	–156	< –150	< –150	< –150	dBm(1Hz)	SNF
integrated noise	1kHz to 100MHz	35	< 70	< 70	< 70	µV	INV
noise floor	>5MHz	–156	< –150	< –150	< –150	dBm(1Hz)	SNF
integrated noise	5MHz to 100MHz	35	< 70	< 70	< 70	µV	INV
STATIC DC PERFORMANCE							
*input offset voltage		10	< 25	< 25	< 25	mV	VIO
average temperature coefficient[1]		35	< 120	< 120	< 120	µV/°C	DVIO
*input bias current	non-inverting	10	< 40	< 30	< 40	µA	IBN
average temperature coefficient[1]		20	< 125	< 125	< 125	nA/°C	DIBN
*input bias current	inverting	20	< 70	< 50	< 70	µA	IBI
average temperature coefficient[1]		70	< 250	< 250	< 250	nA°/C	DIBI
*power supply rejection ratio		55	> 45	> 45	> 45	dB	PSRR
common mode rejection ratio		46	> 40	> 40	> 40	dB	CMRR
*supply current	no load	29	< 36	< 34	< 36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	> 100	> 100	> 100	kΩ	RIN
	capacitance	2.4	< 3	< 3	< 3	pF	CIN
ouput impedance	at DC	—	< 0.1	< 0.1	< 0.1	Ω	RO
	at 50MHz	1, 35	—	—	—	Ω, nH	ZO
output voltage range	no load	±12	> ±11	> ±11	> ±11	V	VO
internal feedback resistor	absolute tolerance	< 0.4	—	—	—	%	RFA

Absolute Maximum Ratings

Common Mode and Output Voltage Limits



supply voltage (V_{cc})	±20V
output current	±100mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C A8: −55°C to + 125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

note 1: Parameters preceded by an * are the final electrical test parameters and are 100% tested. A8 units are tested at –55°C, +25°C, and +125°C. AI units are tested only at +25°C although performance at –25°C and +85°C is guaranteed to be better than or equal to the performance specified for A8 devices in the –55°C and +125°C ranges. Maximum temperature coefficient parameters apply only to A8 devices.

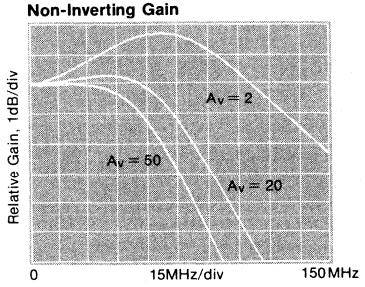
note 2: This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1µs (duty cycle not exceeding 10%), maximum input voltage may be as large as twice the maximum. V_{cm} should never exceed V_{cc}. (V_{cm} is the voltage at the non-inverting input, pin 6.)

note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{cc} is ± 15V.

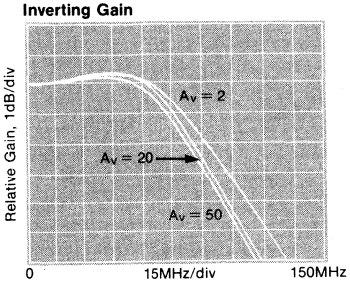
note 4: Settling time specifications require the use of an external feedback resistor (2000Ω).

Typical Performance Characteristics ($T_A = 25°C$, $A_v = 20$, $V_{cc} = \pm 15V$, $R_L = 200\Omega$)

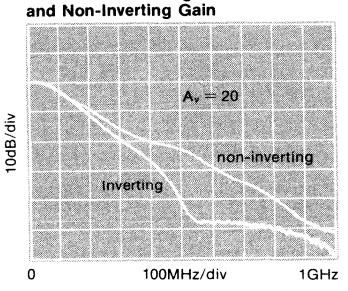
Non-Inverting Gain



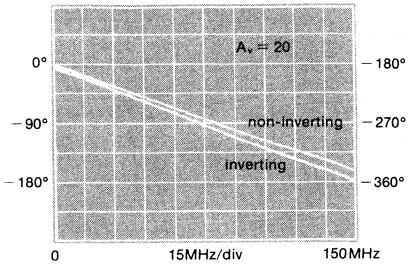
Inverting Gain



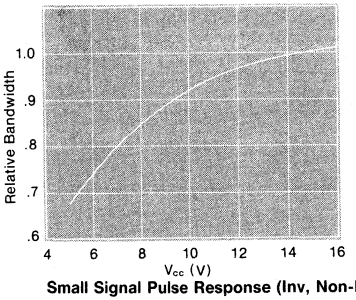
Broadband Inverting and Non-Inverting Gain



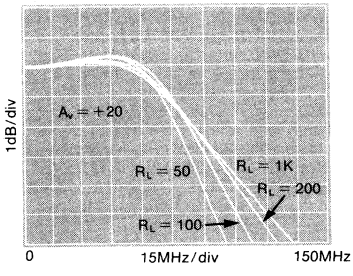
Inverting and Non-Inverting Phase



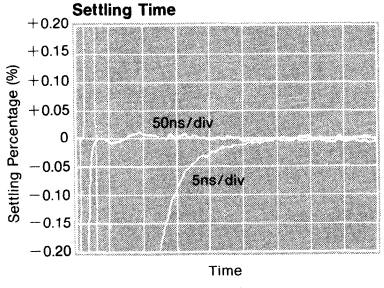
Relative Bandwidth vs. V_{cc}



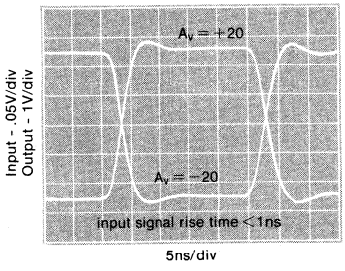
Gain vs. Frequency for Various R_Ls



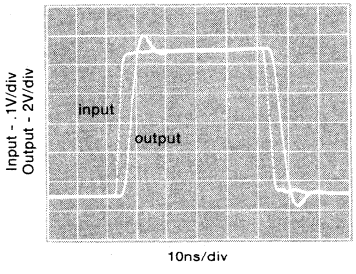
Settling Time



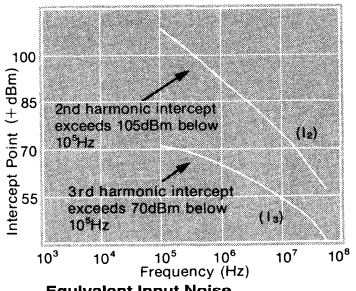
Small Signal Pulse Response (Inv, Non-Inv)



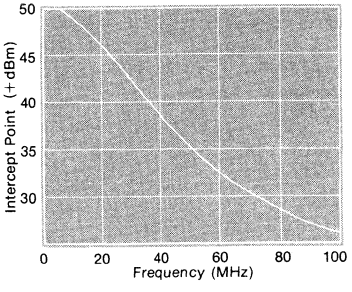
Large Signal Pulse Response



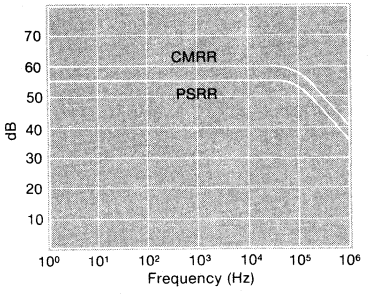
2nd and 3rd Harmonic Distortion Intercept



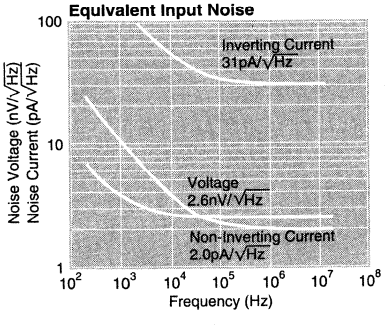
2-Tone 3rd Order Intermod. Intercept

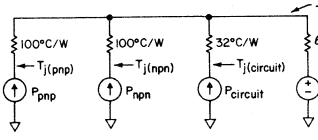


CMRR and PSRR



Equivalent Input Noise





θ_{ca} = 65°C/W in still air without a heatsink
38°C/W in still air with a Thermalloy 2268
15°C/W in 300ft/min air with a Thermalloy 2268

$P_{circuit} = I_{cc}[(+V_{cc}) - (-V_{cc})]$ where $I_{cc} = 23mA$ at $\pm 15V$

$P_{XXX} = [(\pm V_{cc}) - V_{out} - (I_{col})(R_{col} + 4)](I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 4mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\,(pnp)} = P_{pnp}(100 + \theta_{ca}) + (P_{cir} + P_{npn})\theta_{ca} + T_a$.
similar for $T_{j\,(npn)}$.

$T_{j\,(cir)} = P_{cir}(32 + \theta_{ca}) + (P_{pnp} + P_{npn})\theta_{ca} + T_a$.

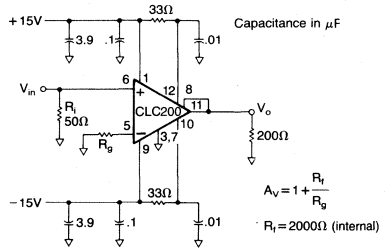


Figure 1: suggested non-inverting gain circuit

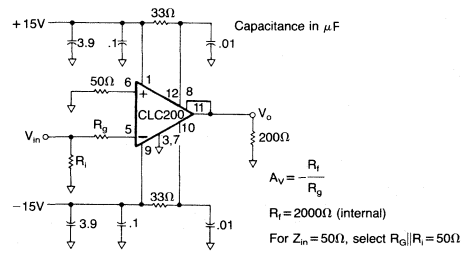


Figure 2: suggested inverting gain circuit

Test fixture schematics are available upon request.

Controlling Bandwidth and Passband Response

As with any op amp, the ratio of the two feedback resistors R_f and R_g determines the gain of the CLC200. Unlike conventional op amps, however, the closed loop pole-zero response of the CLC200 is affected very little by the value of R_g. R_g scales the magnitude of the gain, but does not change the value of the feedback. This is possible due to a proprietary circuit topology. R_f does influence the feedback and so the CLC200 has been internally compensated for optimum performance with R_f=2000Ω, but any value of R_f>1kΩ may be used with a single capacitor placed between pins 4 and 5 for compensation. See Table 1. As R_f decreases, C_c must increase to maintain flat gain. Slew rate will decrease slightly with increasing C_c, but other parameters such as bandwidth, settling time, and phase linearity will improve. Large values of R_f and C_c can be used together or separately to reduce the bandwidth. This may be desirable for reducing the bandwidth in applications not requiring the full frequency response available although this may cause the output noise to increase at low gains.

Table 1: Bandwidth versus R_f and C_c

R_f (kΩ)	C_c (pF)	$f \pm 0.3$dB (MHz)	$f - 3.0$dB (MHz)
10.0	0	5	15
5.0	0	10	30
3.0	0	20	60
2.0	0	50	100
1.5	0.25	70	130
1.0	0.50	120	170

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{cc} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in Figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip of coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available from Comlinear at minimal cost.

Distortion and Amplification Fidelity

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the CLC200. First, convert the output voltage (V_O) to $V_{RMS} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{RMS}^2))$ to get output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below P, as will the two-tone third order intermodulation products. These approximations are useful for P<−1dB compression levels.

Approximate noise figure can be determined for the CLC200 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{\frac{i_n^2 R_F^2}{A_v^2} + v_n^2}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current at the inverting node. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

For linear operation of the CLC200 at large output voltage swings (DC component not included) and at high frequencies, observe the (AC output voltage) × (frequency) product specification of 400V · MHz. Exceeding this rating will cause the signal to be greatly distorted as the amplifier bias control circuit reduces the current available for slewing to prevent damage. At frequencies and voltages within this range the excess slew rate and bandwidth available will ensure the highest possible degree of amplified signal fidelity.

Operation with Reduced Bias Current

Placing a resistor between pins 1 and 2 will cause the CLC200 bias current to be reduced. A value of 20K will cause only a slight reduction, 3K will almost halve the current, while less than 1K will reduce bias to about 5mA and the amplifier will be off. In this condition, the input signal will be greatly attenuated. In the reduced bias, on condition, bandwidth will be roughly proportional to the reduction in bias current. A mechanical or semiconductor switch can be used to turn the amplifier off. Any connection which would cause current to flow out of pin 2 will result in increased bias current and may lead to device destruction from overheating and excessive current.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly qualified applications engineers to provide technical and design assistance.

Comlinear Corporation

Fast Settling, Wideband Operational Amplifiers

CLC201

APPLICATIONS:

- fast, precision A to D, D to A conversion
- baseband and video communications
- radar, sonar, IF processors
- laser drivers, photodiode preamps
- graphic CRT composite video drive amp
- high resolution imaging systems

FEATURES (typical):

- −3dB bandwidth of 95MHz
- 0.5mV input offset voltage, 5μV/°C drift
- 0.1% settling in 18ns
- 4000V/μs slew rate
- 3.6ns rise and fall times

DESCRIPTION:

The CLC201 is a wideband operational amplifier that combines state of the art dynamic performance with excellent DC performance. This combination allows designers to maximize system performance without making the speed versus DC accuracy compromises that are necessary with most high-speed amplifiers. For example, the CLC201 provides a **−3dB bandwidth of 95MHz** (at a gain of +20) and a **settling time of only 18ns** (to 0.1%) yet exhibits an input offset voltage that is typically only 0.5mV and guaranteed to be less than 1.0mV at +25°C. **The input offset voltage drift is typically only 5μV/°C.**

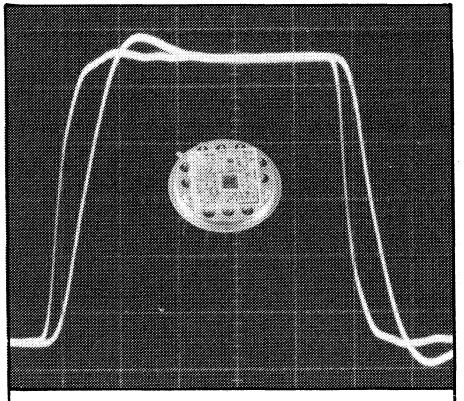
The superior slew rate and rise and fall times of the CLC201 make it an ideal amplifier for a broad range of pulse, analog, and digital applications. The **full-power bandwidth of 50MHz and 100mA output current** eliminate the need for power buffers in most applications. Flat gain and phase response from DC to beyond 50MHz ensure distortion levels well below those of other op amps; in high-resolution applications such as 12-bit A to D converters, this low distortion combined with the excellent DC performance allows maximum accuracy and dynamic range—without the need for complicated error correction circuitry. Engineers desiring to increase the DC performance or full-power bandwidth of systems using the original CLC200 may replace it with a CLC201—in most cases with no design changes (they are pin compatible, however the CLC201 has neither a bias control pin nor a compensation pin).

The excellent dynamic performance is due to Comlinear's proprietary op amp topology, a unique design which is not subject to the limitations of the conventional op amp design. Dynamic parameters such as **settling time and bandwidth are virtually independent of gain**; for example, at a gain of −4, the bandwidth is 105MHz, yet it is still 95MHz at a gain of −20 (see the table below). In addition, the CLC201 is **inherently stable across its entire (±1 to ±50) gain range.** Besides the performance, the benefit of these features is reduced design time and the ability to make design changes with little or no change in dynamic performance.

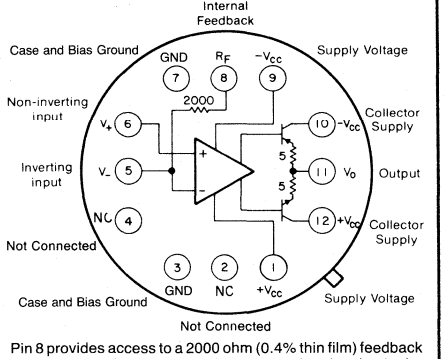
The CLC201 is constructed using thin film resistor/bipolar transistor technology. The CLC201AI is specified over a temperature range of −25°C to +85°C, while the CLC201A8C is specified over a range of −55°C to +125°C and is fully compliant with MIL-STD-883 Level B. Both devices are packaged in 12-pin metal TO-8 cans. The DESC SMD number is 5962-90833.

Typical Performance

parameter	gain setting +4	+20	+50	−4	−20	−50	units
−3dB bandwidth	150	95	80	105	95	80	MHz
rise time (20V)	—	4	5	4	4	4	ns
slew rate	4	4	4	4	4	4	V/ns
settling time (0.1%)	—	18	20	18	18	20	ns

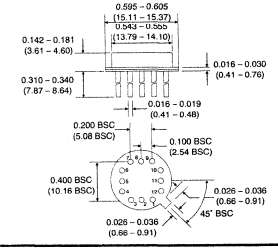


BOTTOM VIEW



Pin 8 provides access to a 2000 ohm (0.4% thin film) feedback resistor. Though not electrically connected to the circuit, the case provides EMI shielding and should be connected to a low impedance signal return.

Package Dimensions



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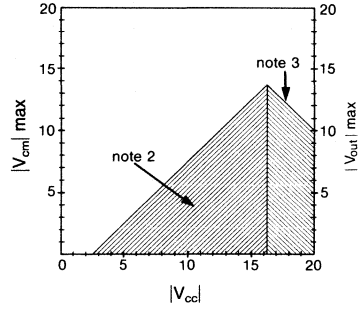
Electrical Characteristics ($A_V = +20$, $V_{CC} = \pm 15V$, $R_L = 200\Omega$, $R_f = 2000\Omega$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	CLC201A8[1]	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC201AI[1]	+25°C	−25°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
*−3dB bandwidth	$V_{out}<2V_{pp}$	95	>85	>85	>75	MHz	SSBW
gain flatness at	$V_{out}<2V_{pp}$						
* peaking	0.1 to <25MHz	0	<0.4	<0.3	<0.5	dB	GFPL
* peaking	>25MHz	0.2	<1	<0.6	<0.6	dB	GFPH
* rolloff	at 50MHz	—	<0.6	<0.4	<0.6	dB	GFR
group delay,	to 50MHz	4.2±0.5	—	—	—	ns	GD
linear phase deviation	to 50MHz	1	<2.5	<2	<3	°	LPD
reverse isolation	to 50MHz						
non-inverting		60	>50	>50	>50	dB	RINI
inverting		45	>35	>35	>35	dB	RIIN
TIME DOMAIN RESPONSE							
rise and fall time	2V step	3.6	<4.1	<4.1	<4.4	ns	TRS
	20V step	4	<5	<5	<6	ns	TRL
settling time to .02%	10V step[4]	30	—	—	—	ns	TSP
to .1%	10V step[4]	18	<25	<25	<30	ns	TS
overshoot	2V step	7	<15	<12	<15	%	OS
slew rate (overdriven input)		4	>3	>3	>3	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		25	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
*2nd harmonic distortion	$2V_{pp}$, 20MHz	−52	<−45	<−45	<−45	dBc	HD2
*3rd harmonic distortion	$2V_{pp}$, 20MHz	−58	<−50	<−50	<−50	dBc	HD3
equivalent noise input							
noise floor	>100kHz	−156	<−150	<−150	<−150	dBm(1Hz)	SNF
integrated noise	1kHz to 100MHz	35	<70	<70	<70	μV	INV
noise floor	>5MHz	−156	<−150	<−150	<−150	dBm(1Hz)	SNF
integrated noise	5MHz to 100MHz	35	<70	<70	<70	μV	INV
STATIC DC PERFORMANCE							
*input offset voltage		0.5	<2.2	<1.0	<2.5	mV	VIO
average temperature coefficient		5	<15	<15	<15	μV/°C	DVIO
*input bias current	non-inverting	5	<36	<20	<20	μA	IBN
average temperature coefficient		50	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	5	<26	<10	<30	μA	IBI
average temperature coefficient		50	<200	<200	<200	nA/°C	DIBI
*power supply rejection ratio		55	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
*supply current	no load	29	<36	<34	<36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	>100	>100	>100	kΩ	RIN
	capacitance	2.4	<3	<3	<3	pF	CIN
output impedance	at DC	—	<0.1	<0.1	<0.1	Ω	RO
	at 50MHz	1, 35	—	—	—	Ω, nH	ZO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO
internal feedback resistor	absolute tolerance	<0.4	—	—	—	%	RFA

Absolute Maximum Ratings

Common Mode and Output Voltage Limits



supply voltage (V_{cc})	±20V
output current	±100mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
	A8: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

***note 1:** Parameters preceded by an * are the final electrical test parameters and are 100% tested. A8 units are tested at –55°C, +25°C, and +125°C. AI units are tested only at +25°C although performance at –25°C and +85°C is guaranteed at –25°C and +85°C as indicated above.

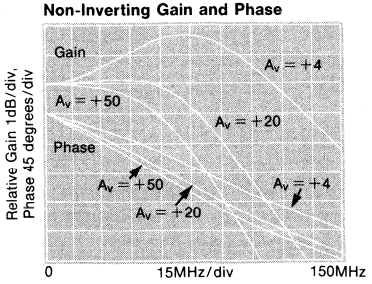
note 2: This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10%), maximum input voltage may be as large as twice the maximum. V_{cm} should never exceed V_{cc}. (V_{cm} is the voltage at the non-inverting input, pin 6.)

note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{cc} is ± 15V.

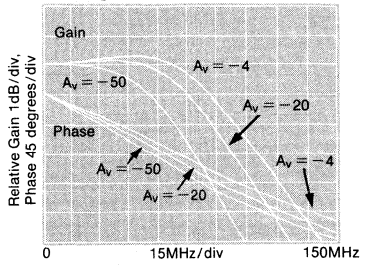
note 4: Settling time specifications require the use of an external feedback resistor (2000Ω).

Typical Performance Characteristics ($T_A = 25°C$, $A_V = +20$, $V_{CC} = \pm 15V$, $R_L = 200\Omega$)

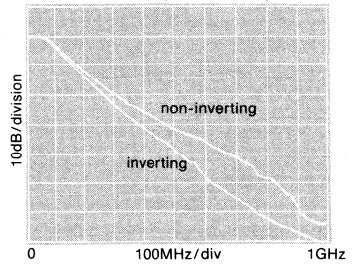
Non-Inverting Gain and Phase



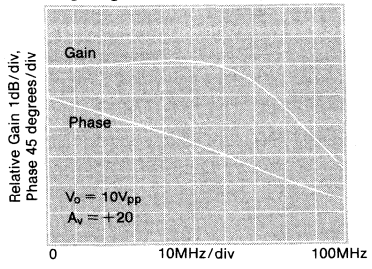
Inverting Gain and Phase



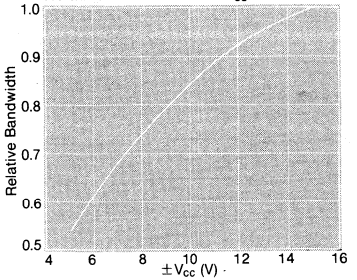
Broadband Gain (Inv, Non-Inv)



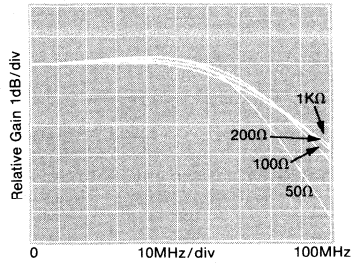
Large Signal Gain and Phase



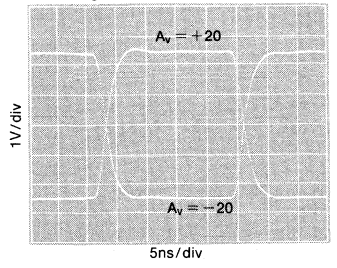
Relative Bandwidth vs. V_{cc}



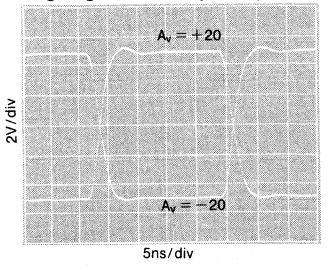
Gain vs. Frequency for Various R_Ls



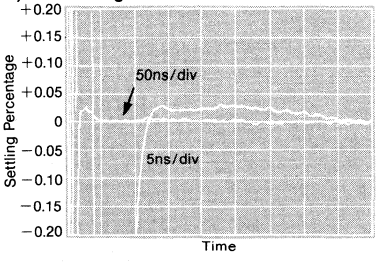
Small Signal Pulse Response (Inv, Non-Inv)



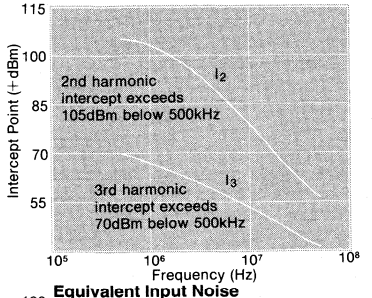
Large Signal Pulse Response (Inv, Non-Inv)



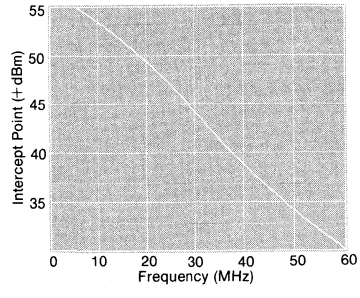
Settling Time



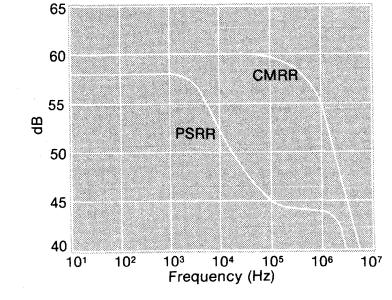
2nd and 3rd Harmonic Distortion Intercept



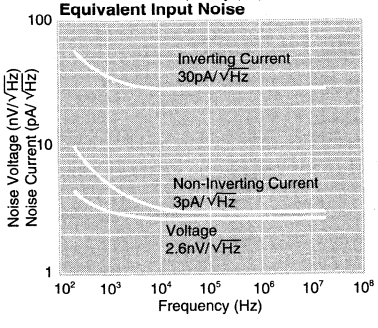
2-Tone 3rd Order Intermod. Intercept

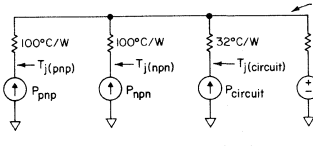


CMRR and PSRR



Equivalent Input Noise





θ_{ca} = 65°C/W in still air without a heatsink
30°C/W in still air with a Thermalloy 2268
15°C/W in 300ft/min air with a Thermalloy 2268

$P_{circuit} = I_{cc}[(+V_{cc}) - (-V_{cc})]$ where $I_{cc} = 25mA$ at $\pm 15V$

$P_{XXX} = [(\pm V_{cc}) - V_{out} - (I_{col})(R_{col} + 5)](I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 4mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\,(pnp)} = P_{pnp}(100 + \theta_{ca}) + (P_{cir} + P_{npn})\theta_{ca} + T_a$, similar for $T_{j\,(npn)}$.

$T_{j\,(cir)} = P_{cir}(32 + \theta_{ca}) + (P_{pnp} + P_{npn})\theta_{ca} + T_a$.

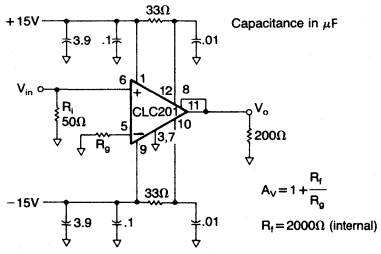


Figure 1: suggested non-inverting gain circuit

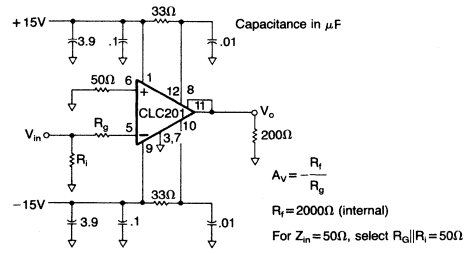


Figure 2: suggested inverting gain circuit

Test fixture layout artwork is available upon request.

CLC201 Operation

The CLC201 is based on Comlinear's proprietary op amp topology, a unique design that uses current feedback instead of the usual voltage feedback. This design provides dynamic performance far beyond that previously available, yet it is used basically the same as the familiar voltage-feedback op amp (see the gain equations above). A complete discussion of current feedback is given in application note AN300-1.

Controlling Bandwidth and Passband Response

In most applications, use of the internal 2000Ω feedback resistor will provide optimum dynamic performance; nonetheless, some designs may require an external feedback resistor of some value other than 2000Ω. The table below shows how bandwidth depends on the value of R_f. Values of feedback resistance greater than 2000Ω will decrease the bandwidth of the amplifier; values of R_f less than 2000Ω will increase the bandwidth. At most gain settings, however, low values of R_f may cause instability unless a small amount of compensation capacitance (typically <0.5pF) is connected in parallel with R_f. At $|A_v|$ <, R_f must be greater than 1kΩ.

Bandwidth versus R_f

R_f (external)	−3dB Bandwidth (A_v = 20)
2kΩ	90MHz
5kΩ	30MHz
10kΩ	15MHz

At large closed-loop gains ($|A_v| \geq 50$) the bandwidth may be increased by using a low value of R_f as the table below indicates. External compensation is not required under these high-gain conditions.

Increasing Bandwidth at High Gains

$|A_v|$	R_f	−3dB Bandwidth
50	1kΩ	90MHz
100	500Ω	70MHz

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{cc} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in Figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available from Comlinear.

Distortion, Noise, and Amplification Fidelity

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the CLC201. First, convert the output voltage (V_O) to $V_{RMS} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{RMS}^2))$ to get output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below P, as will the two-tone third order intermodulation products. These approximations are useful for P<—1dB compression levels.

Approximate noise figure can be determined for the CLC201 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current at the inverting node. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

For linear operation of the CLC201 at large output voltage swings (DC component not included) and at high frequencies, limit the (AC output voltage) × (frequency) product to 1000V·MHz. Exceeding this rating will cause the signal to be greatly distorted as the amplifier bias control circuit reduces the current available for slewing to prevent damage. At frequencies and voltages within this range the excess slew rate and bandwidth available will ensure the highest possible degree of amplified signal fidelity.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly qualified applications engineers to provide technical and design assistance.

Comlinear Corporation

Fast Settling, High Current Wideband Op Amps

CLC203

APPLICATIONS:

- coaxial line driving
- DAC current to voltage amplifier
- flash A to D driving
- baseband and video communications
- radar and IF processors

FEATURES:

- 60MHz full-power bandwidth ($20V_{pp}$, 100Ω)
- 200mA output current
- 0.2% settling in 15ns
- 0.5mV input offset voltage, $5\mu V/°C$ drift
- 4ns rise and fall times (20V)

DESCRIPTION:

The CLC203 is a wideband, high-current operational amplifier which features a unique combination of high power and high precision. The amplifier's **output current of 200mA and a full-power bandwidth of 60MHz ($20V_{pp}$, 100Ω)** ensure a quick design solution for the most demanding loads and signals. The **solid 15ns settling time (to 0.2%)** is reinforced by the CLC203's excellent DC performance; typically, the input offset voltage is only 0.5mV and is guaranteed to be less than 1mV at +25°C. **The input offset voltage drift is typically only $5\mu V/°C$.**

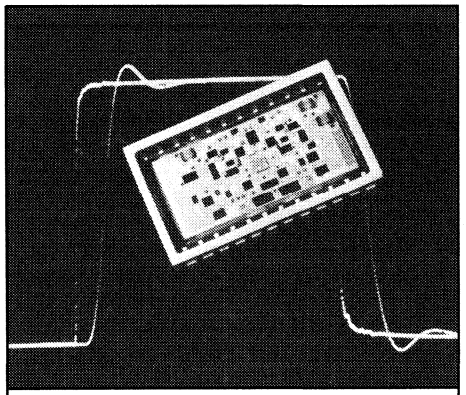
The CLC203 is well suited to a wide range of applications. Specifically, the wide bandwidth, fast settling, linear phase, and very low harmonic distortion provide the designer with the signal fidelity needed in applications such as driving flash A to Ds or coaxial lines. The 60MHz full-power bandwidth and 200mA output current of the CLC203 eliminate the need for power buffers in most applications. Engineers desiring to improve the DC performance or settling precision of systems using the original CLC103 may replace it with a CLC203—in most cases with no design changes (they are pin compatible, however the CLC203 does not have a bias control pin).

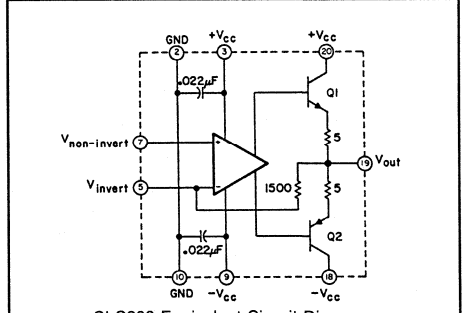
The dynamic performance of the CLC203 is based on Comlinear's proprietary op amp topology. This new design provides performance far beyond that available from conventional op amp designs; for example, **the −3dB bandwidth remains nearly constant over a wide range of gains.** (See the table below.) And since the amplifier is inherently stable, the user is saved the trouble and expense of designing external compensation networks. The result is shorter design time and the ability to accommodate design changes (in gain, for example) without loss of performance or a redesign of compensation circuits.

The CLC203 is constructed using thin film resistor/bipolar transistor technology. The CLC203AI is specified over a temperature range of –25°C to +85°C, while the CLC203AM is specified over a range of –55°C to +125°C and is screened to Comlinear's M Standard for high reliability applications. Both devices are packaged in 24-pin ceramic DIPs.

Typical Performance

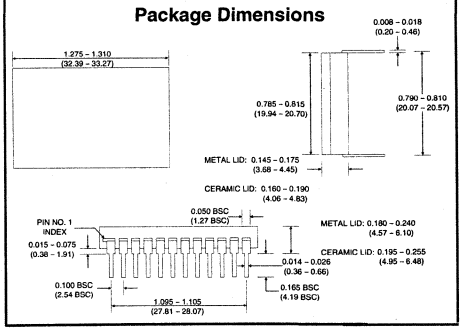
parameter	gain setting +4	+20	+50	−4	−20	−50	units
−3dB bandwidth	250	170	120	195	165	120	MHz
rise time (20V)	4	4	4	4	4	4	ns
slew rate	6	6	6	6	6	6	V/ns
settling time (0.2%)	15	15	18	15	15	18	ns





CLC203 Equivalent Circuit Diagram
(all undesignated pins are internally unconnected)

Package Dimensions



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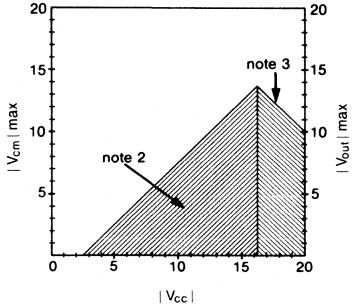
Electrical Characteristics ($A_V = +20$, $V_{CC} = \pm 15V$, $R_L = 100\Omega$, $R_f = 1500\Omega$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	CLC203AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC203AI	+25°C	−25°C	+25°C	+ 85°C		
FREQUENCY DOMAIN RESPONSE							
*−3dB bandwidth	$V_{out}<4V_{pp}$	160	>140	>140	>110	MHz	SSBW
	$V_{out}=20V_{pp}$	60	>50	>50	>40	MHz	FPBW
gain flatness at	$V_{out}<4V_{pp}$						
* peaking	0.1 to 40MHz	0.1	<0.7	<0.4	<0.3	dB	GFPL
* peaking	>40MHz	0.2	<1.5	<0.6	<0.6	dB	GFPH
* rolloff	at 75MHz	—	<0.4	<0.6	<1.0	dB	GFR
group delay	to 75MHz	3.3±0.3	—	—	—	ns	GD
linear phase deviation	to 75MHz	1	<3.5	<2.5	<2.5	°	LPD
reverse isolation	to 150MHz						
non-inverting		55	>45	>45	>45	dB	RINI
inverting		48	>40	>40	>40	dB	RII
TIME DOMAIN RESPONSE							
rise and fall time	5V step	2.5	<2.9	<2.9	<3.3	ns	TRS
	20V step	4.0	<5.0	<5.0	<5.0	ns	TRL
settling time to 0.2%	10V step	15	<25	<20	<25	ns	TSP
overshoot	5V step	7	<20	<15	<15	%	OS
slew rate (overdriven input)		6	>5	>5	>5	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		30	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
*2nd harmonic distortion	$2V_{pp}$, 20MHz	−55	<−45	<−45	<−45	dBc	HD2
*3rd harmonic distortion	$2V_{pp}$, 20MHz	−55	<−45	<−45	<−45	dBc	HD3
equivalent noise input							
noise floor	>100kHz	−158	<−152	<−152	<−152	dBm(1Hz)	SNF
integrated noise	1kHz to 100MHz	28	<56	<56	<56	μV	INV
noise floor	>5MHz	−158	<−152	<−152	<−152	dBm(1Hz)	SNF
integrated noise	5MHz to 100MHz	28	<56	<56	<56	μV	INV
STATIC DC PERFORMANCE							
*input offset voltage		0.5	<2.2	<1.5	<2.5	mV	VIO
average temperature coefficient		5	<15	<15	<15	μV/°C	DVIO
*input bias current	non-inverting	5	<36	<20	<20	μA	IBN
average temperature coefficient		50	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	5	<26	<15	<30	μA	IBI
average temperature coefficient		50	<200	<200	<200	nA/°C	DIBI
*power supply rejection ratio		60	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
*supply current	no load	30	<36	<34	<36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	>100	>100	>100	kΩ	RIN
	capacitance	2.4	<3	<3	<3	pF	CIN
output impedance	at DC	—	<0.1	<0.1	<0.1	Ω	RO
	at 75MHz	2, 45	—	—	—	Ω, nH	ZO
output voltage range	no load	—	>±11	>±11	>±11	V	VO

Absolute Maximum Ratings

Common Mode and Output Voltage Limits



supply voltage (V_{cc})	±20V
output current	±200mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
	AM: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

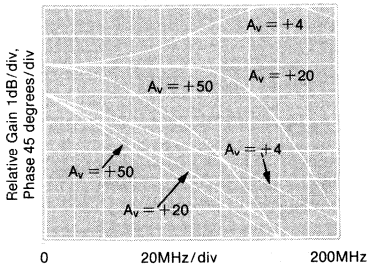
***note 1:** Parameters preceded by an * are the final electrical test parameters and are 100% tested. AM units are tested at –55°C, +25°C, and +125°C. AI units are tested only at +25°C although their performance is guaranteed at –25°C and +85°C as indicated above.

note 2: This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10%), maximum input voltage may be as large as twice the maximum. V_{cm} should never exceed V_{cc}. (V_{cm} is the voltage at the non-inverting input, pin 7.)

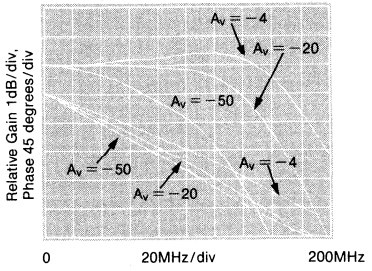
note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{cc} is ± 15V.

Typical Performance Characteristics ($A_v = +20$, $V_{cc} = \pm 15V$, $R_L = 100\Omega$, $R_f = 1500\Omega$)

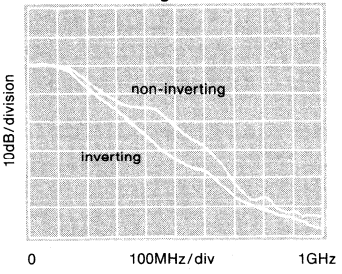
Non-Inverting Gain and Phase



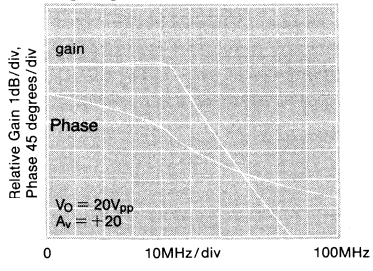
Inverting Gain and Phase



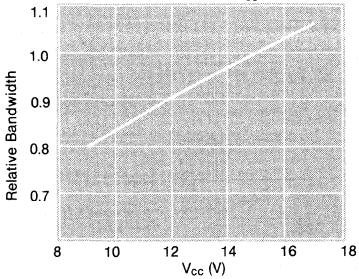
Broadband Inverting and Non-Inverting Gain



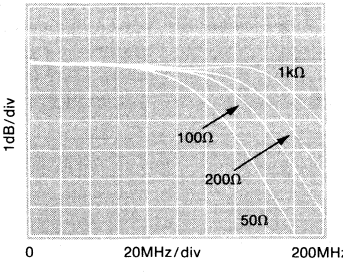
Large Signal Gain and Phase



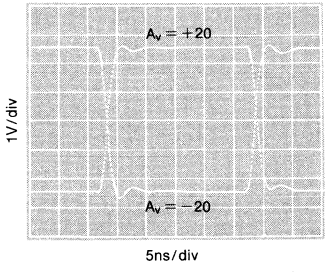
Relative Bandwidth vs. V_{cc}



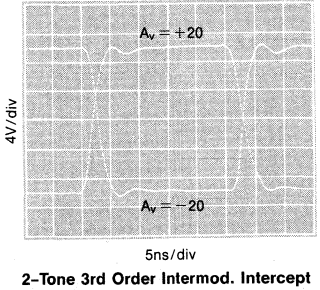
Gain vs. Frequency for Various Loads



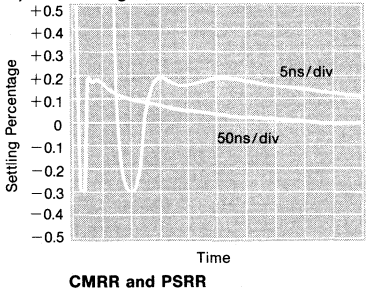
Small Signal Pulse Response (Inv, Non-Inv)



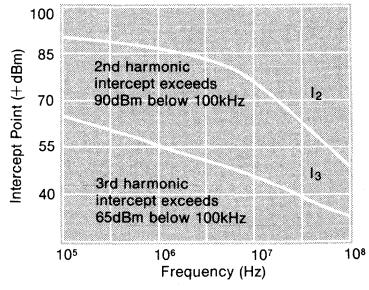
Large Signal Pulse Response (Inv, Non-Inv)



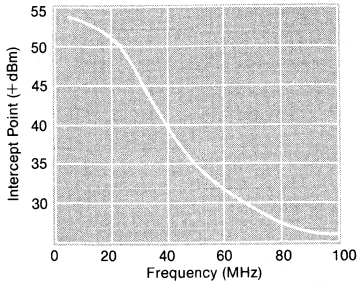
Settling Time



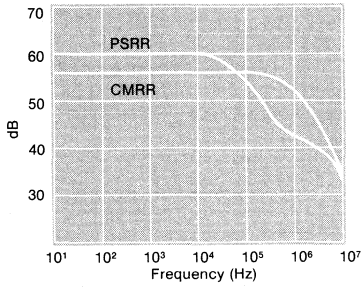
2nd and 3rd Harmonic Distortion Intercept



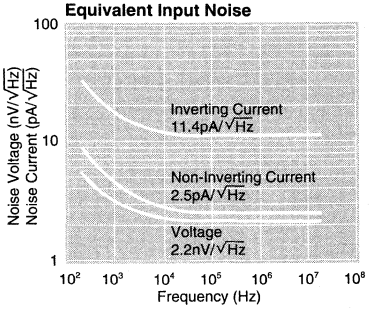
2-Tone 3rd Order Intermod. Intercept

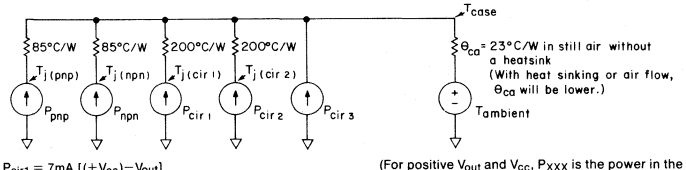


CMRR and PSRR



Equivalent Input Noise





$P_{cir1} = 7mA\,[(+V_{cc}) - V_{out}]$
$P_{cir2} = 7mA\,[V_{out} - (-V_{cc})]$
$P_{cir3} = I_c\,[(+V_{cc}) - (-V_{cc})]$ where $I_c = 15mA$ at $\pm 15V$
$P_{xxx} = I_{col}\,[(\pm V_{cc}) - V_{out} - I_{col}\,(R_{col} + 5)]$ where $I_{col} = V_{out}/R_{load}$ or 8mA, whichever is greater. (Include R_f in R_{load}.)

(For positive V_{out} and V_{cc}, P_{XXX} is the power in the npn device. For negative V_{out} and V_{cc}, this power is in the pnp device.)
R_{col} is an external resistor (22 ohms recommended) between the xxx collector and $\pm V_{cc}$.
$T_{j\,(pnp)} = (P_{pnp})\ 85°C/W + (P_{total})\ \theta_{ca} + T_{ambient}$, similar for $T_{j\,(npn)}$.
$T_{j\,(cir1)} = (P_{cir1})\ 200°C/W + (P_{total})\ \theta_{ca} + T_{ambient}$, similar for $T_{j\,(cir2)}$.

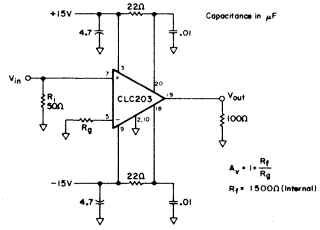


Figure 1: recommended non-inverting gain circuit

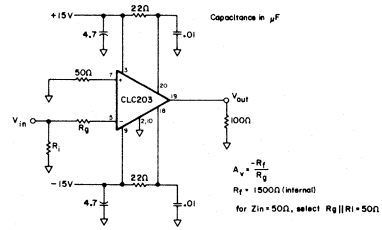


Figure 2: recommended inverting circuit

Test fixture layout artwork is available upon request.

CLC203 Operation

The CLC203 is based on Comlinear's proprietary op amp topology, a unique design which uses current feedback instead of the usual voltage feedback. This design provides dynamic performance far beyond that previously available, yet it is used basically the same as the familiar voltage-feedback op amp (see the gain equations above). A complete discussion of current feedback is given in application note AN300-1.

Increasing Bandwidth at High Gains

At high gains ($|A_v| \geq 50$) the bandwidth of the CLC203 may be increased by lowering the value of feedback resistance. This is done by connecting an external resistor in parallel with the internal 1500Ω feedback resistor. The table below shows the recommended external resistor values for different gain settings.

Increasing Bandwidth at High Gains

$\|A_v\|$	external resistor	−3dB bandwidth
50	3kΩ	140MHz
100	750Ω	110MHz

Layout Considerations

To obtain optimum performance from any circuit operating at high frequencies, good PC layout is essential. Fortunately, the stable, well-behaved response of the CLC203 makes operation at high frequencies less sensitive to layout than is the case with other wideband op amps, even though the CLC203 has a much wider bandwidth.

In general, a good layout is one which minimizes the unwanted coupling of a signal between nodes in a circuit. A continuous ground plane from the signal input to output on the circuit side of the board is helpful. Traces should be kept short to minimize inductance. If long traces are needed, use microstrip transmission lines which are terminated in their characteristic impedance. At some high-impedance nodes, or in sensitive areas such as near pin 5 of the CLC203, stray capacitance should be kept small by keeping nodes small and removing ground plane directly around the node.

The $\pm V_{cc}$ connections to the CLC203 are internally bypassed to ground with 0.022μF capacitors to provide good high-frequency decoupling. It is recommended that 1μF or larger tantalum capacitors be provided for low-frequency decoupling. The 0.01μF capacitors shown at pins 18 and 20 in figures 1 and 2 should be kept within 0.1" of those pins. A wide strip of ground plane should be provided for a signal return path between the load-resistor ground and these capacitors.

Since the layout of the PC board forms such an important part of the circuit, much time can be saved if prototype amplifier boards are tested early in the design stage. Encased/connectorized amplifiers are available from Comlinear.

Distortion and Noise

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the CLC203. First, convert the output voltage (V_O) to $V_{rms} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{rms}^2))$ to get the output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$ dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$ dB below the level of P, as will the two-tone third order intermodulation products. These approximations are useful for $P < -1$dB compression levels.

Approximate noise figure can be determined for the CLC203 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current at the inverting node. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high-frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly-qualified applications engineers to provide technical and design assistance.

Comlinear Corporation

Overdrive-Protected Wideband Op Amp

CLC205

APPLICATIONS:

- fast, precision A/D conversion
- automatic test equipment
- input/output amplifiers
- photodiode, CCD preamps
- IF processors
- high-speed modems, radios
- line drivers

FEATURES:

- −3dB bandwidth of 170MHz
- 0.1% settling in 22ns
- complete overdrive protection
- low power: 570mW (57mW at ± 5V)
- 3MΩ input resistance
- output may be current limited

DESCRIPTION:

The CLC205 is a wideband overdrive-protected operational amplifier designed for applications needing both speed and low power operation. Utilizing Comlinear's well-established current feedback architecture, the CLC205 exhibits performance far beyond that of conventional voltage feedback op amps. For example, the CLC205 has a bandwidth of 170MHz at a gain of +20 and settles to 0.1% in 22ns. Plus, the CLC205 has a combination of important features not found in other high-speed op amps.

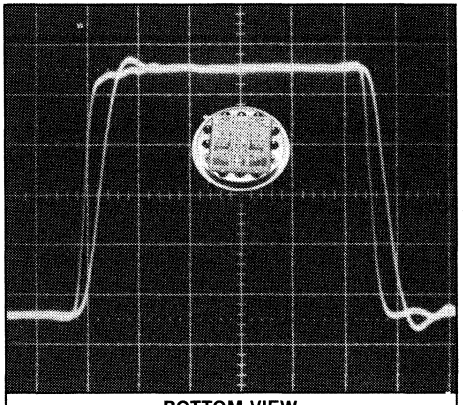
For example, the CLC205 has been designed to consume little power—570mW at ±15V supplies. The result is lower power supply requirements and less system-level heat dissipation. In addition, the device can be operated on supply voltages as low as ±5V for even lower power dissipation.

Complete overdrive protection has been designed into the part. This is critical for applications, such as ATE and instrumentation, which require protection from signal levels high enough to cause saturation of the amplifier. This feature allows the output of the op amp to be protected against short circuits using techniques developed for low-speed op amps. With this capability, even the fastest signal sources can feature effective short circuit protection.

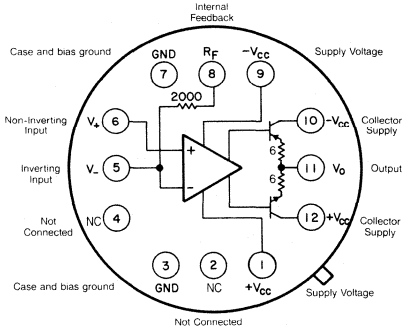
The CLC205 is constructed using thin-film resistor/bipolar transistor technology and is available in three versions. The CLC205AI is specified over a temperature range of –25°C to+85°C. The CLC205AK, which features burn in and tested hermeticity, is specified and tested over a temperature range of –55°C to +125°C. The CLC205A8C is specified and tested over a temperature range of –55°C to +125°C and is fully compliant with MIL-STD-883, Level B. All three versions are packaged in 12-pin TO-8 cans. The DESC SMD number is 5962-90835.

Typical Performance

parameter	gain setting +7	+20	+50	−1	−20	−50	units
−3dB bandwidth	220	170	80	220	130	80	MHz
rise time	1.7	2.2	4.7	1.7	2.9	4.7	ns
slew rate	2.4	2.4	2.4	2.4	2.4	2.4	V/ns
settling time (to 0.1%)	22	22	20	21	20	19	ns

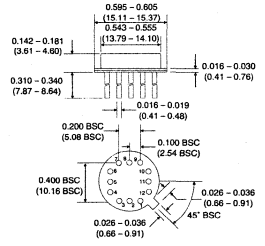


BOTTOM VIEW



Pin 8 provides access to a 2000Ω feedback resistor which can be connected to the output or left open if an external feedback resistor is desired.

Package Dimensions



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Electrical Characteristics ($A_V = +20$, $V_{cc} = \pm 15V$, $R_L = 200\Omega$, $R_f = 2k\Omega$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC205AI	+25°C	−25°C	+25°C	+85°C		
Ambient Temperature	CLC205A8/AK	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
*−3dB bandwidth	$V_{out} < 2V_{pp}$	170	>140	>140	>125	MHz	SSBW
large signal bandwidth	$V_{out} < 10V_{pp}$	100	>72	>80	>80	MHz	FPBW
gain flatness	$V_{out} < 2V_{pp}$						
* peaking	0.1 to 35MHz	0	<0.3	<0.3	<0.5	dB	GFPL
* peaking	>35MHz	0	<0.5	<0.5	<0.8	dB	GFPH
* rolloff	at 70MHz	—	<0.8	<0.8	<0.8	dB	GFR
group delay	to 70MHz	3.0 ± .2	—	—	—	ns	GD
linear phase deviation	to 70MHz	0.8	<3.0	<2.0	<3.0	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.2	<2.6	<2.6	<3.0	ns	TRS
	10V step	4.8	<5.5	<5.5	<5.5	ns	TRL
settling time to 0.1%	10V step, note 2	22	<27	<27	<27	ns	TS
to 0.05%	10V step, note 2	24	<30	<30	<30	ns	TSP
overshoot	5V step	7	<14	<14	<14	%	OS
slew rate	$20V_{pp}$ @ 50MHz	2.4	>1.8	>2.0	>2.0	V/ns	SR
DISTORTION AND NOISE RESPONSE, note 3							
*2nd harmonic distortion	$2V_{pp}$, 20MHz	−57	<−50	<−50	<−50	dBc	HD2
*3rd harmonic distortion	$2V_{pp}$, 20MHz	−68	<−55	<−55	<−55	dBc	HD3
equivalent input noise							
voltage	>100kHz	2.1	<3.0	<3.0	<3.5	nV/$\sqrt{Hz}$	VN
inverting current	>100kHz	22	<30	<30	<35	pA/$\sqrt{Hz}$	ICN
non-inverting current	>100kHz	4.8	<6.5	<6.5	<7.5	pA/$\sqrt{Hz}$	NCN
noise floor	>100kHz	−157	<−154	<−154	<−153	dBm(1Hz)	SNF
integrated noise	1kHz to 150MHz	39	<55	<55	<61	μV	INV
noise floor	>5MHz	−157	<−154	<−154	<−153	dBm(1Hz)	SNF
integrated noise	5MHz to 150MHz	39	<55	<55	<61	μV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		3.5	<8.0	<8.0	<11.0	mV	VIO
average temperature coefficient		11	<25	<25	<25	μV/°C	DVIO
*input bias current	non-inverting	3.0	<25	<15	<15	μA	IBN
average temperature coefficient		15	<100	<100	<100	nA/°C	DIBN
*input bias current	inverting	2.0	<22	<10	<25	μA	IBI
average temperature coefficient		20	<150	<150	<150	nA/°C	DIBI
*power supply rejection ratio		69	>55	>55	>55	dB	PSRR
common mode rejection ratio		60	>50	>50	>50	dB	CMRR
*supply current	no load	19	<20	<20	<22	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance	DC	3.0	>1.0	>1.0	>1.0	MΩ	RIN
non-inverting input capacitance	70MHz	5.0	<7.0	<7.0	<7.0	pF	CIN
output impedance	DC	—	<0.1	<0.1	<0.1	Ω	RO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO
internal feedback resistor							
absolute tolerance		—	—	<0.2	—	%	RFA
temperature coefficient		—	—	−100±40	—	ppm/°C	RFTC
inverting input current self limit		2.2	<3.0	<3.0	<3.2	mA	ICL

Absolute Maximum Ratings

V_{cc}	±20V
I_{out}	±75mA
common mode input voltage	±(|V_{cc}| − 1)V
differential input voltage	±3V
thermal resistance: See thermal model.	
junction temperature	+175°C
operating temperature AI:	−25°C to +85°C
A8/AK:	−55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

Recommended Operating Conditions

V_{cc}	±5V to ±15V
I_{out}	±50mA
common mode input voltage	±(|V_{cc}| − 5)V
gain range:	+7 to +50, −1 to −50

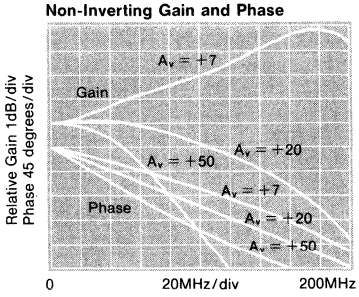
***note: 1:** Parameters preceded by an * are 100% tested. A8 and AK units are tested at −55°C, +25°C, and +125°C. AI units tested at +25°C, although performance at −25°C and +85°C is guaranteed as shown above.

note: 2: Settling time specifications require the use of an external feedback resistor (2Ω).

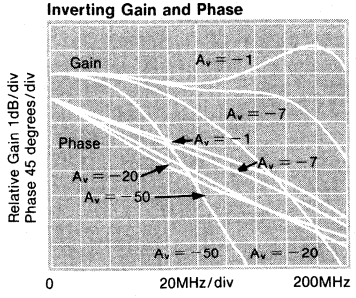
note: 3: In AI units, the noise and distortion specifications are guaranteed (but not tested) as shown above.

Typical Performance Characteristics ($T_A = 25°C$, $A_v = +20$, $V_{CC} = \pm 15V$, $R_L = 200\Omega$)

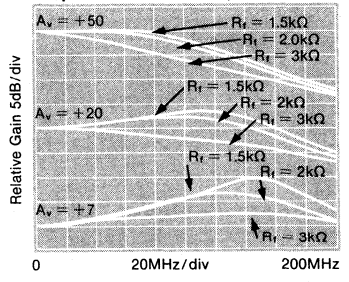
Non-Inverting Gain and Phase



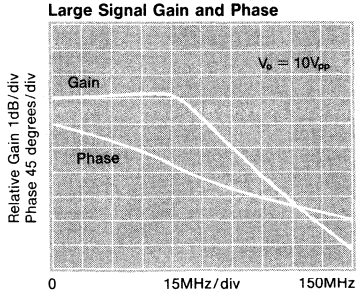
Inverting Gain and Phase



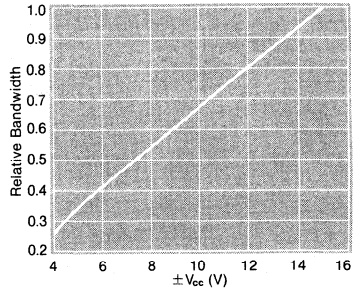
Response vs. External R_f



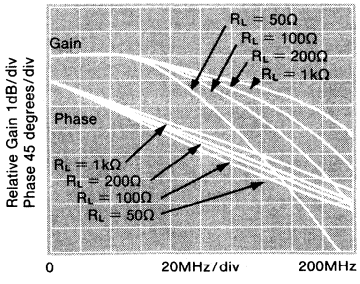
Large Signal Gain and Phase



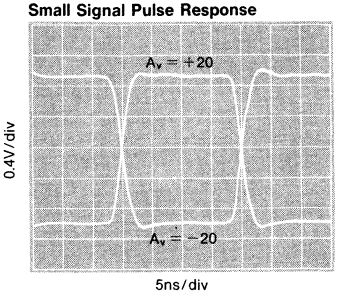
Relative Bandwidth vs. V_{CC}



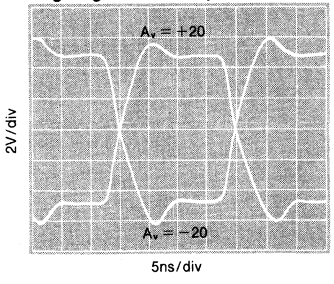
Gain and Phase for Various Loads



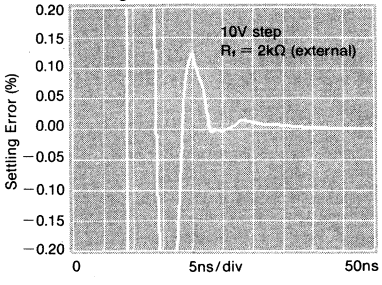
Small Signal Pulse Response



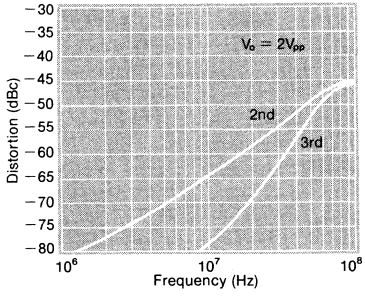
Large Signal Pulse Response



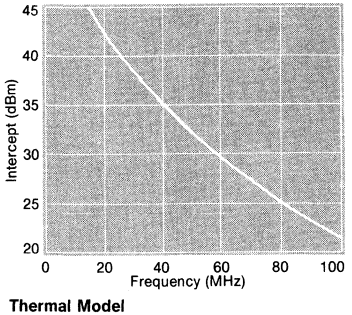
Settling Time



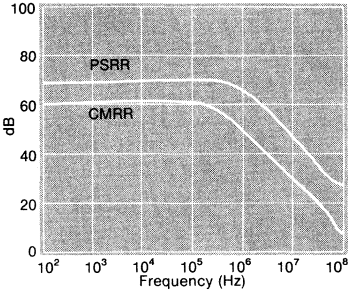
2nd and 3rd Harmonic Distortion



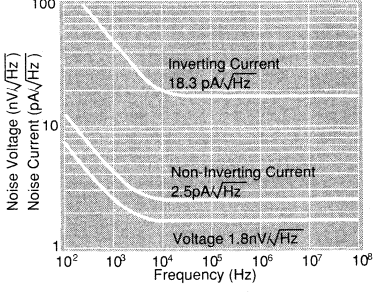
2-Tone 3rd Order Intermodulation Intercept



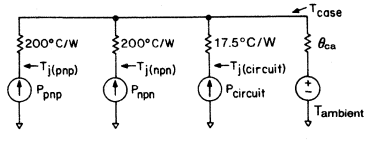
CMRR and PSRR



Equivalent Input Noise



Thermal Model



θ_{ca} = 65°C/W in still air without a heatsink
35°C/W in still air with a Thermalloy 2268
15°C/W in 300ft/min air with a Thermalloy 2268
(Thermalloy 2240 works equally well.)

$P_{circuit} = [(+V_{cc}) - (-V_{cc})]^2 / 1.77k\Omega$

$P_{xxx} = [(\pm V_{cc}) - V_{out} - (I_{col})(R_{col} + 6)]$ (I_{col})
(% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)
(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 3mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\ (pnp)} = P_{pnp}(200 + \theta_{ca}) + (P_{cir} + P_{npn})\,\theta_{ca} + T_a$, similar for $T_{j\ (npn)}$.

$T_{j\ (cir)} = P_{cir}(17.5 + \theta_{ca}) + (P_{pnp} + P_{npn})\,\theta_{ca} + T_a$.

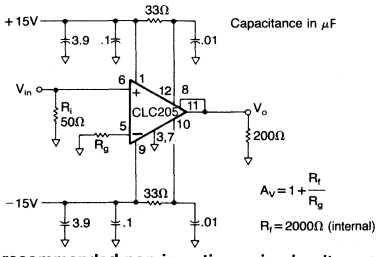


Figure 1: recommended non-inverting gain circuit

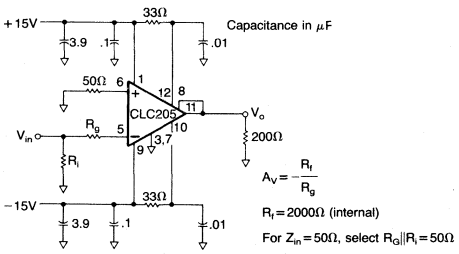


Figure 2: recommended inverting gain circuit

Test fixture schematics are available upon request.

Overdrive Protection

Unlike most other high-speed op amps, the CLC205 is not damaged by saturation caused by overdriving input signals (where $V_{in} \times \text{gain} > \text{max. } V_{out}$). The CLC205 self limits the current at the inverting input when the output is saturated (see the inverting input current self limit specification); this ensures that the amplifier will not be damaged due to excessive internal currents during overdrive. For protection against input signals which would exceed either the maximum differential or common mode input voltage, the diode clamp circuits below may be used.

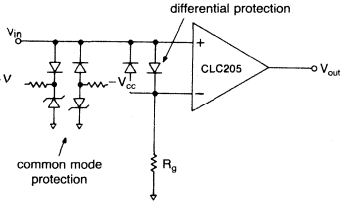


Figure 3: Diode clamp circuits for common mode and differential mode protection.

Short Circuit Protection

Damage caused by short circuits at the output may be prevented by limiting the output current to safe levels. The most simple current limit circuit calls for placing resistors between the output stage collector supplies and the output stage collectors (pins 12 and 10). The value of this resistor is determined by:

$$R_c = \frac{V_c}{I_l} - R_l$$

Where I_l is the desired limit current and R_l is the minimum expected load resistance (0Ω for a short to ground). Bypass capacitors of 0.01μF on should be used on the collectors as in Figures 1 and 2.

A more sophisticated current limit circuit which provides a limit current independent of R_l is shown below.

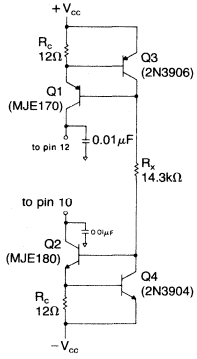


Figure 4: Active current limit circuit (50mA)

With the component values indicated, current limiting occurs at 50mA. For other values of current limit (I_l), select R_c to equal V_{be}/I_l. Where V_{be} is the base to emitter voltage drop of Q3 (or Q4) at a current of $[2V_{cc} - 1.4] / R_x$, where $R_x \leq [(2V_{cc} - 1.4) / I_l]$ B_{min}. Also, B_{min} is the minimum beta of Q1 (or Q2) at a current of I_l. Since the limit current depends on V_{be}, which is temperature dependent, the limit current is likewise temperature dependent. If a temperature-independent current limit circuit is needed, contact Comlinear.

Controlling Bandwidth and Passband Response

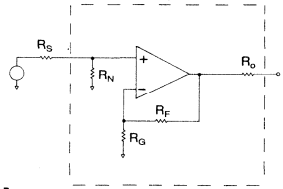
In most applications, a feedback resistor value of 2kΩ will provide optimum performance; nonetheless, some applications may require a resistor of some other value. The response versus R_f plot on the previous page shows how decreasing R_f will increase bandwidth (and frequency response peaking, which may lead to instability). Conversely, large values of feedback resistance tend to roll off the response.

The best settling time performance requires the use of an external feedback resistor (use of the internal resistor results in a 0.1% to 0.2% settling tail). The settling performance may be improved slightly by adding a capacitance of 0.4pF in parallel with the feedback resistor (settling time specifications reflect performance with an external feedback resistor but with no external capacitance).

Noise Analysis

Approximate noise figure can be determined for the CLC205 using the equivalent input noise graph on the preceding page and the equations shown below.

Noise figure is for the network inside this box.



$$F = 10\log\left[1 + \frac{R_S}{R_N} + \frac{R_S}{4kT}\cdot\left(i_n^2 + \frac{V_n^2}{R_p^2} + \frac{R_F^2\, i_i^2}{R_p^2\, A_v^2}\right)\right]$$

where $R_p = \dfrac{R_S\, R_N}{R_S + R_N}$; $A_v = \dfrac{R_F}{R_G} + 1$

$kT = 4.00 \times 10^{-21}$ Joules at 290°K
V_n is spot noise voltage ($V / \sqrt{Hz}$)
i_n is non-inverting spot noise current ($A / \sqrt{Hz}$)
i_i is inverting spot noise current ($A / \sqrt{Hz}$)

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance the performance of the CLC205. Good ground plane construction and power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal stray capacitance to the ground plane or other nodes. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Evaluation PC boards (part number 730008 for inverting, 730009 for non-inverting) for the CLC205 are available.

Comlinear Corporation

Overdrive-Protected Wideband Op Amp

CLC206

APPLICATIONS:

- fast, precision A/D conversion
- automatic test equipment
- input/output amplifiers
- photodiode, CCD preamps
- IF processors
- high-speed modems, radios
- line drivers

FEATURES:

- −3dB bandwidth of 180MHz
- 70MHz large signal bandwidth ($20V_{pp}$)
- 0.1% settling in 19ns
- overdrive protected
- output may be current limited
- stable w/o compensation
- 3MΩ input impedance

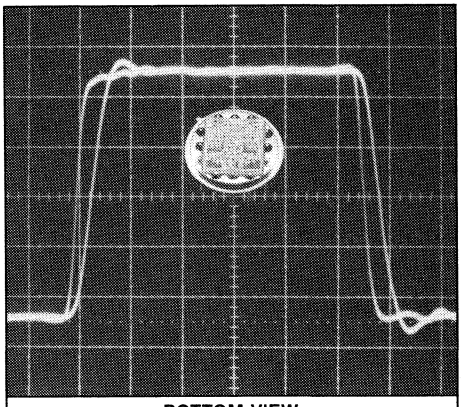
DESCRIPTION:

The CLC206 is a wideband, overdrive-protected operational amplifier designed for applications needing both speed and high drive capability (100mA). Utilizing Comlinear's well-established current feedback architecture, the CLC206 exhibits performance far beyond that of conventional voltage feedback op amps. For example, the CLC206 has a bandwidth of 180MHz at a gain of +20 and settles to 0.1% in 19ns. Plus, the CLC206 has a combination of important features not found in other high-speed op amps.

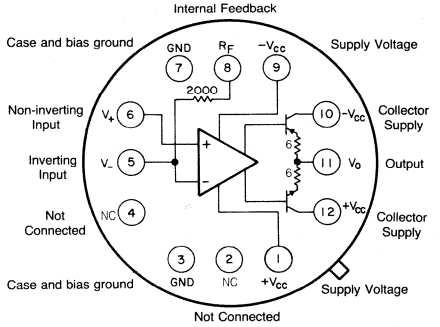
The 100mA output current and the large signal bandwidth of 70MHz ($20V_{pp}$) make the CLC206 ideal for applications which involve both high signal amplitudes and heavy loads as in coaxial line driving applications.

Complete overdrive protection has been designed into the CLC206. This is critical for applications, such as ATE and instrumentation, which require protection from signal levels high enough to cause saturation of the amplifier. This feature allows the output of the op amp to be protected against short circuits using techniques developed for low-speed op amps. With this capability, even the fastest signal sources can feature effective short circuit protection.

The CLC206 is constructed using thin-film resistor/bipolar transistor technology and is available in three versions. The CLC206AI is specified over a temperature range of –25°C to +85°C. The CLC206AK, which features burn in and tested hermeticity, is specified and tested over a temperature range of –55°C to +125°C. The CLC206A8C is specified and tested over a temperature range of –55°C to +125°C and is fully compliant with MIL-STD-883, Level B. All three versions are packaged in 12-pin TO-8 cans. The DESC SMD number is 5962-89858.



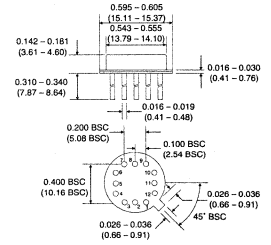
BOTTOM VIEW



Not Connected

Pin 8 provides access to a 2000Ω feedback resistor which can be connected to the output or left open if an external feedback resistor is desired.

Package Dimensions



Typical Performance

parameter	gain setting						units
	+7	+20	+50	−1	−20	−50	
−3dB bandwidth	220	180	90	220	145	90	MHz
rise time	1.6	2	4	1.6	2.5	4	ns
slew rate	3.4	3.4	3.4	3.4	3.4	3.4	V/ns
settling time (to 0.1%)	22	19	17	20	19	18	ns

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics ($A_V = +20$, $V_{cc} = \pm 15V$, $R_L = 200\Omega$, $R_f = 2k\Omega$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC206AI	+25°C	−25°C	+25°C	+85°C		
Ambient Temperature	CLC206A8/AK	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
*−3dB bandwidth	$V_{out} < 2V_{pp}$	180	>150	>150	>135	MHz	SSBW
large signal bandwidth	$V_{out} < 20V_{pp}$	70	>54	>60	>60	MHz	FPBW
gain flatness	$V_{out} < 2V_{pp}$						
* peaking	0.1 to 40MHz	0	<0.3	<0.3	<0.5	dB	GFPL
* peaking	>40MHz	0	<0.5	<0.5	<0.8	dB	GFPH
* rolloff	at 75MHz	—	<0.7	<0.7	<0.7	dB	GFR
group delay	to 75MHz	3.0±.2	—	—	—	ns	GD
linear phase deviation	to 75MHz	0.6	<2.0	<1.5	<2.0	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.0	<2.5	<2.5	<2.7	ns	TRS
	20V step	7.0	<8.5	<8.5	<8.5	ns	TRL
settling time to 0.1%	10V step, note 2	22	<25	<25	<25	ns	TS
to 0.05%	10V step, note 2	24	<27	<27	<27	ns	TSP
overshoot	10V step	11	<15	<15	<15	%	OS
slew rate	$20V_{pp}$, 100MHz	3.4	>2.7	>3.0	>3.0	V/ns	SR
DISTORTION AND NOISE RESPONSE, note 3							
*2nd harmonic distortion	$2V_{pp}$, 20MHz	−59	<−50	<−50	<−50	dBc	HD2
*3rd harmonic distortion	$2V_{pp}$, 20MHz	−67	<−55	<−55	<−55	dBc	HD3
equivalent input noise							
voltage	>100kHz	2.1	<3.0	<3.0	<3.5	nV/$\sqrt{Hz}$	VN
inverting current	>100kHz	22	<30	<30	<35	pA/$\sqrt{Hz}$	ICN
non-inverting current	>100kHz	5.0	<7.0	<7.0	<8.0	pA/$\sqrt{Hz}$	NCN
noise floor	>100kHz	−157	<−154	<−154	<−153	dBm(1Hz)	SNF
integrated noise	1kHz to 150MHz	39	<55	<55	<61	uV	INV
noise floor	>5MHz	−157	<−154	<−154	<−153	dBm(1Hz)	SNF
integrated noise	5MHz to 150MHz	39	<55	<55	<61	uV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		3.5	<8.0	<8.0	<11.0	mV	VIO
average temperature coefficient		11	<25	<25	<25	uV/°C	DVIO
*input bias current	non-inverting	4.0	<30	<20	<20	uA	IBN
average temperature coefficient		20	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	2.0	<26	<10	<30	uA	IBI
average temperature coefficient		40	<200	<200	<200	nA/°C	DIBI
*power supply rejection ratio		65	>55	>55	>55	dB	PSRR
common mode rejection ratio		60	>50	>50	>50	dB	CMRR
*supply current	no load	29	<31	<31	<33	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance	DC	3.0	>1.0	>1.0	>1.0	MΩ	RIN
non-inverting input capacitance	75MHz	5.2	<7.0	<7.0	<7.0	pF	CIN
output impedance	DC	—	<0.1	<0.1	<0.1	Ω	RO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO
internal feedback resistor							
absolute tolerance		—	—	<0.2	—	%	RFA
temperature coefficient		—	—	−100±40	—	ppm/°C	RFTC
inverting input current self limit		3.3	<4.5	<4.5	<4.7	mA	ICL

Absolute Maximum Ratings

V_{cc}	±20V
I_{out}	±150mA
common mode input voltage	±(|V_{cc}|−1)V
differential input voltage	±3V
thermal resistance: See thermal model.	
junction temperature	+175°C
operating temperature AI:	−25°C to +85°C
A8/AK:	−55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

Recommended Operating Conditions

V_{cc}	±5V to ±15V
I_{out}	±100mA
common mode input voltage	±(|V_{cc}|−5)V
gain range:	+7 to +50, −1 to −50

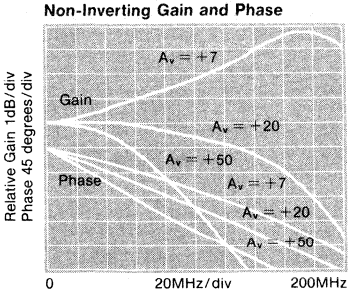
***note: 1:** Parameters preceded by an * are 100% tested. A8 and AK units are tested at –55°C, +25°C, and +125°C. AI units tested at +25°C, although performance at –25°C and +85°C is guaranteed as shown above.

note 2: Settling time specifications require the use of an external feedback resistor (2Ω).

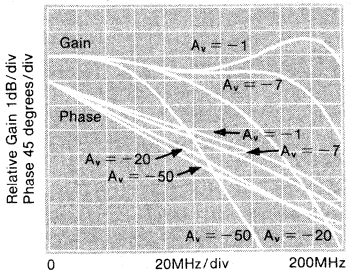
note 3: In AI units, the noise and distortion specifications are guaranteed (but not tested) as shown above.

Typical Performance Characteristics ($T_A = 25°C$, $A_v = +20$, $V_{cc} = \pm 15V$, $R_L = 200\Omega$)

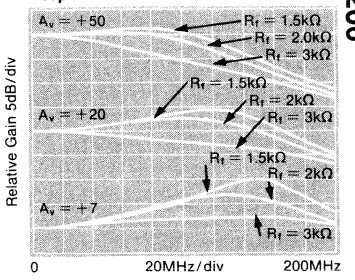
Non-Inverting Gain and Phase



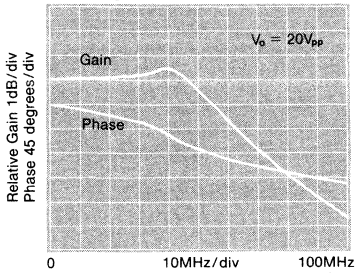
Inverting Gain and Phase



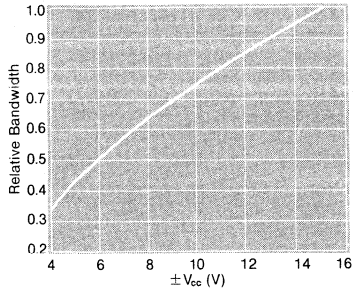
Response vs. External R_f



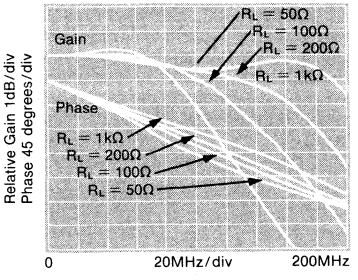
Large Signal Gain and Phase



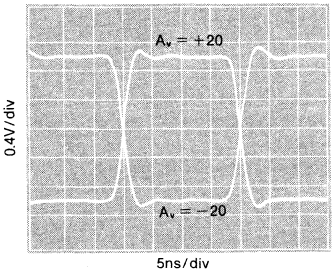
Relative Bandwidth vs. V_{cc}



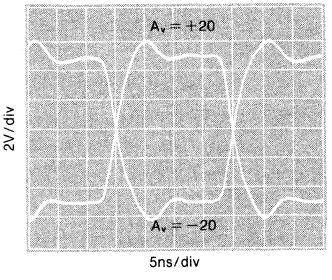
Gain and Phase for Various Loads



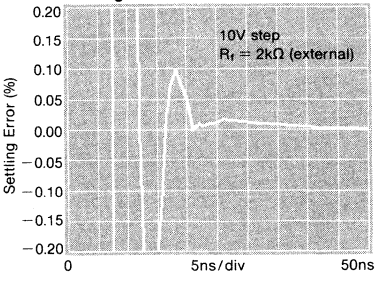
Small Signal Pulse Response



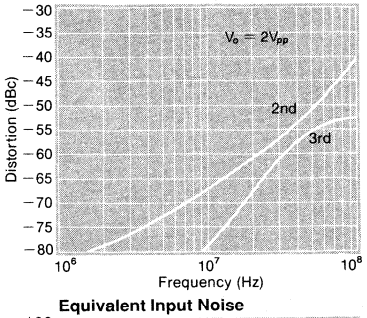
Large Signal Pulse Response



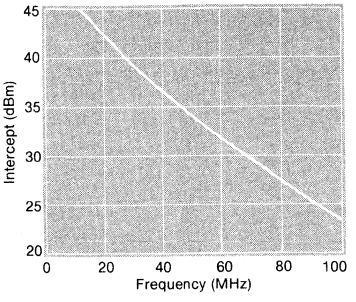
Settling Time



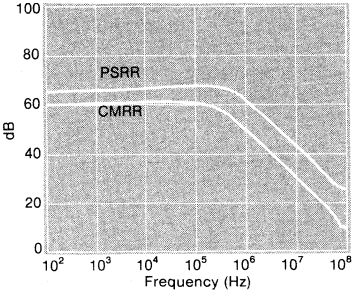
2nd and 3rd Harmonic Distortion



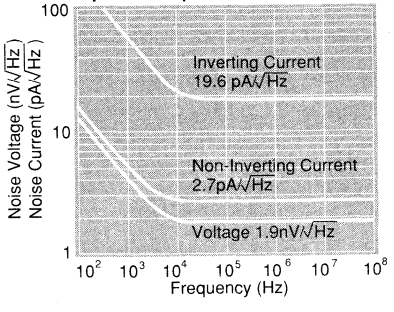
2-Tone 3rd Order Intermodulation Intercept



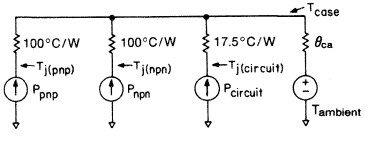
CMRR and PSRR



Equivalent Input Noise



Thermal Model



θ_{ca} = 65°C/W in still air without a heatsink
35°C/W in still air with a Thermalloy 2268
15°C/W in 300ft/min air with a Thermalloy 2268
(Thermalloy 2240 works equally well.)

$P_{circuit} = [(+V_{cc}) - (-V_{cc})]^2 \ / \ 1.15k\Omega$

$P_{xxx} = [(\pm V_{cc}) - V_{out} - (I_{col})(R_{col} + 6)] \quad (I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 4mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\ (pnp)} = P_{pnp}\ (100 + \theta_{ca}) + (P_{cir} + P_{npn})\ \theta_{ca} + T_a$, similar for $T_{j\ (npn)}$.

$T_{j\ (cir)} = P_{cir}\ (17.5 + \theta_{ca}) + (P_{pnp} + P_{npn})\ \theta_{ca} + T_a$.

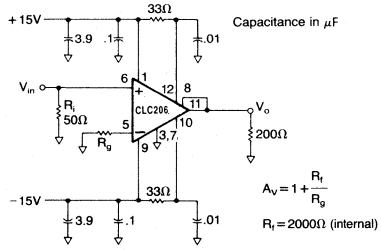


Figure 1: recommended non-inverting gain circuit

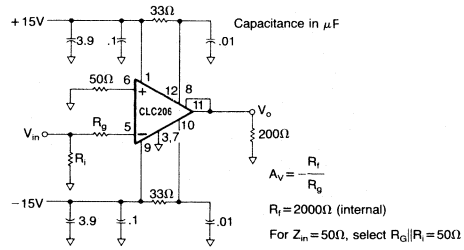


Figure 2: recommended inverting gain circuit

Test fixture schematics are available upon request.

Overdrive Protection

Unlike most other high-speed op amps, the CLC206 is not damaged by saturation caused by overdriving input signals (where V_{in}X gain> V_{out}). The CLC206 self limits the current at the inverting input when the output is saturated (see the inverting input current self limit specification); this ensures that the amplifier will not be damaged due to excessive internal currents during overdrive. For protection against input signals which would exceed either the maximum differential or common mode input voltage, the diode clamp circuits below may be used.

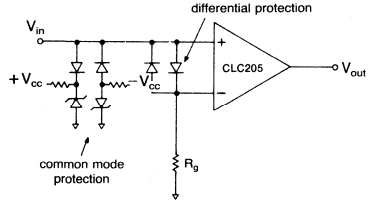


Figure 3: Diode clamp circuits for common mode and differential mode protection

Short Circuit Protection:

Damage caused by short circuits at the output may be prevented by limiting the output current to safe levels. The most simple current limit circuit calls for placing resistors between the output stage collector supplies and the output stage collectors (pins 12 and 10). The value of this resistor is determined by:

$$R_c = \frac{V_c}{I_l} - R_l$$

Where I_l is the desired limit current and R_l is the minimum expected load resistance (0Ω for a short to ground). Bypass capacitors of 0.01μF on should be used on the collectors as in Figures 1 and 2.

A more sophisticated current limit circuit which provides a limit current independent of R_l is shown below.

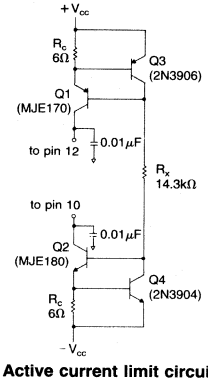


Figure 4: Active current limit circuit (100mA)

With the component values indicated, current limiting occurs at 100mA. For other values of current limit (I_l), select $R_c$to equal V_{be}/I_l. Where V_{be} is the base to emitter voltage drop of Q3 (or Q4) at a current of $[2V_{cc} - 1.4]/R_x$, where $R_x \leq [(2V_{cc} - 1.4)/I_l]\ B_{min}$. Also, B_{min} is the minimum beta of Q1 (or Q2) at a current of I_l. Since the limit current depends on V_{be}, which is temperature dependent, the limit current is likewise temperature dependent. If a temperature-independent current limit circuit is needed, contact Comlinear.

Controlling Bandwidth and Passband Response

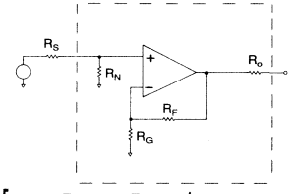
In most applications, a feedback resistor value of 2kΩ will provide optimum performance; nonetheless, some applications may require a resistor of some other value. The response versus R_f plot on the previous page shows how decreasing R_f will increase bandwidth (and frequency response peaking, which may lead to instability). Conversely, large values of feedback resistance tend to roll off the response.

The best settling time performance requires the use of an external feedback resistor (use of the internal resistor results in a 0.1% to 0.2% settling tail). The settling performance may be improved slightly by adding a capacitance of 0.4pF in parallel with the feedback resistor (settling time specifications reflect performance with an external feedback resistor but with no external capacitance).

Noise Analysis

Approximate noise figure can be determined for the CLC206 using the equivalent input noise graph on the preceding page and the equations shown below.

Noise figure is for the network inside this box



$$F = 10\log\left[1 + \frac{R_S}{R_N} + \frac{R_S}{4kT} \cdot \left(i_n^2 + \frac{V_n^2}{R_p^2} + \frac{R_F^2\ i_i^2}{R_p^2\ A_v^2}\right)\right]$$

$$\text{where } R_p = \frac{R_S\ R_N}{R_S + R_N};\ A_v = \frac{R_F}{R_G} + 1$$

$kT = 4.00 \times 10^{-21}$ Joules at 290°K

V_n is spot noise voltage ($V/\sqrt{Hz}$)

i_n is non-inverting spot noise current ($A/\sqrt{Hz}$)

i_i is inverting spot noise current ($A/\sqrt{Hz}$)

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance the performance of the CLC206. Good ground plane construction and power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal stray capacitance to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Evaluation PC boards (part number 730008 for inverting, 730009 for non-inverting) for the CLC206 are available.

Comlinear Corporation

Low Distortion Wideband Op Amp

CLC207

APPLICATIONS:

- fast, precision A/D conversion
- wide dynamic range IF amps
- test waveform generation
- VCO drivers
- DDS postamps
- radar/communication receivers
- line drivers

FEATURES (typical):

- −80/−85dBc 2nd/3rd harmonics at 20MHz
- −3dB bandwidth of 170 MHz
- 0.1% settling in 22ns
- 2400V/μs slew rate
- overdrive protection
- 3MΩ input resistance
- output may be current limited

DESCRIPTION:

The CLC207 is a wideband, low distortion operational amplifier designed specifically for applications requiring both high speed and wide dynamic range. Utilizing Comlinear's proprietary current feedback architecture, the CLC207 offers performance far superior to that of conventional voltage feedback op amps.

The most attractive feature of the CLC207 is its extremely low distortion: −80/−85dBc 2nd/3rd harmonics at 20MHz ($2V_{pp}$, $R_L = 200\Omega$). The CLC207 also provides −3dB bandwidth of 170MHz at a gain of +20, settles to 0.1% in 22ns and slews at a rate of 2400V/μs, yet is unity-gain stable without external compensation. The combination of these features positions the CLC207 as the right choice for high speed applications requiring exceptional signal purity.

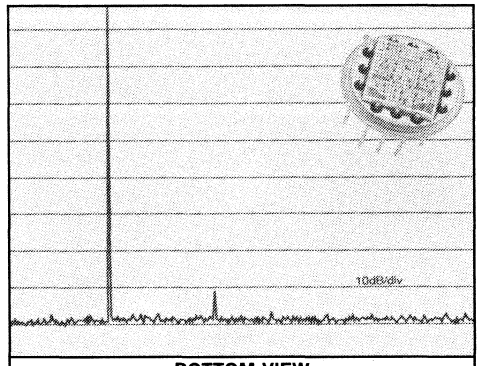
High speed, high resolution A/D and D/A converter systems requiring low distortion operation will find the CLC207 an excellent choice. Wide dynamic range systems such as radar and communication receivers will find that the CLC207's low harmonic distortion and low noise make it an attractive high speed solution.

The addition of the CLC207 to the 205/206 Series of high speed operational amplifiers broadens the selection of features available from which to choose. The CLC205 offers low power operation, the CLC206 offers higher drive operation, and the CLC207 offers operation with extremely low distortion, all of which are pin compatible and overdrive protected.

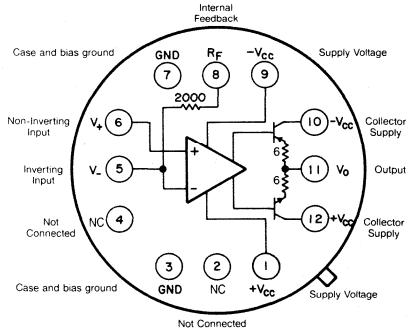
The CLC207 is constructed using thin-film resistor/bipolar transistor technology and is available in three versions. The CLC207AI is specified over a temperature range of –25°C to +85°C. The CLC207AK, which features burn-in and tested hermeticity, is specified and tested over a temperature range of –55°C to +125°C. The CLC207A8C is specified and tested over a temperature range of –55°C to +125°C and is screened to MIL-STD-883 for high-reliability applications. All three versions come in 12-pin, TO-8 packages. The DESC SMD number is 5962-90977.

Typical Performance

parameter	gain setting						units
	+7	+20	+50	−1	−20	−50	
−3dB bandwidth	220	170	80	220	130	80	MHz
rise time	1.7	2.2	4.7	1.7	2.9	4.7	ns
slew rate	2.4	2.4	2.4	2.4	2.4	2.4	V/ns
settling time (to 0.1%)	22	22	20	21	20	19	ns

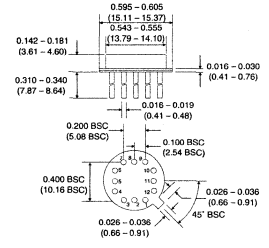


BOTTOM VIEW



Pin 8 provides access to a 2000Ω feedback resistor which can be connected to the output or left open if an external feedback resistor is desired.

Package Dimensions



Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics ($A_V = +20$; $V_{CC} = \pm 15V$; $R_L = 200\Omega$; $R_f = 2k\Omega$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC207AI	+25°C	−25°C	+25°C	+ 85°C		
Ambient Temperature	CLC207A8/AK	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
*−3dB bandwidth	$V_{out}<2V_{pp}$	170	>140	>140	>125	MHz	SSBW
	$V_{out}<10V_{pp}$	100	>72	>80	>80	MHz	LSBW
gain flatness	$V_{out}<2V_{pp}$						
* peaking	0.1 to 35MHz	0	<0.3	<0.3	<0.5	dB	GFPL
* peaking	>35MHz	0	<0.5	<0.5	<0.8	dB	GFPH
* rolloff	at 70MHz	—	<0.8	<0.8	<0.8	dB	GFR
group delay	to 70MHz	3.0±.2	—	—	—	ns	GD
linear phase deviation	to 50MHz	0.8	<3.0	<2.0	<3.0	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.2	<2.6	<2.6	<3.0	ns	TRS
	10V step	4.8	<5.5	<5.5	<5.5	ns	TRL
settling time to 0.1%	10V step, note 2	22	<27	<27	<27	ns	TS
to 0.05%	10V step, note 2	24	<30	<30	<30	ns	TSP
overshoot	5V step	7	<14	<14	<14	%	OS
slew rate	$20V_{pp}$ @ 50MHz	2400	>1800	>2000	>2000	V/μs	SR
DISTORTION AND NOISE RESPONSE, note 3							
*2nd harmonic distortion	$2V_{pp}$, 20MHz, $R_L = 200\Omega$*	−80	<−68	<−76	<−76	dBc	HD2
	$R_L = 100\Omega$	−69	<−64	<−64	<−64	dBc	HD2
*3rd harmonic distortion	$2V_{pp}$, 20MHz, $R_L = 200\Omega$*	−85	<−76	<−76	<−76	dBc	HD3
	$R_L = 100\Omega$	−69	<−64	<−64	<−64	dBc	HD3
equivalent noise input							
voltage	>100kHz	1.6	<1.8	<1.8	<1.8	nV/√Hz	VN
inverting current	>100kHz	20	<23	<23	<23	pA/√Hz	ICN
non-inverting current	>100kHz	2.2	<2.5	<2.5	<2.5	pA/√Hz	NCN
noise floor	>100kHz	−158	<−157	<−157	<−157	dBm_{1Hz}	SNF
integrated noise	1kHz to 150MHz	33	<38	<38	<38	μV	INV
integrated noise	5MHz to 150MHz	33	<38	<38	<38	μV	INV
STATIC DC PERFORMANCE							
*input offset voltage		3.5	<8.0	<8.0	<11.0	mV	VIO
average temperature coefficient		11	<25	<25	<25	μV/°C	DVIO
*input bias current	non-inverting	3.0	<25	<15	<15	μA	IBN
average temperature coefficient		15	<100	<100	<100	nA/°C	DIBN
*input bias current	inverting	2.0	<22	<10	<25	μA	IBI
average temperature coefficient		20	<150	<150	<150	nA/°C	DIBI
*power supply rejection ratio		69	>55	>55	>55	dB	PSRR
common mode rejection ratio		60	>50	>50	>50	dB	CMRR
*supply current	no load	25	<27	<27	<29	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance	DC	3.0	>1.0	>1.0	>1.0	MΩ	RIN
non-inverting input capacitance	70MHz	5.0	<7.0	<7.0	<7.0	pF	CIN
output impedance	DC	—	<0.1	<0.1	<0.1	Ω	RO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO
internal feedback resistor		2.0	—	—	—	kΩ	RF
absolute tolerance		—	—	<0.2	—	%	RFA
temperature coefficient		—	—	−100±40	—	ppm/°C	RFTC
inverting input current self limit		2.2	<3.0	<3.0	<3.2	mA	ICL

Absolute Maximum Ratings

V_{CC}		±20V
I_{out}		±150mA
V_{CM}, V_{out}	$\|V_{CC}\| > 15V$	$\pm(29-\|V_{CC}\|)V$
	$\|V_{CC}\| \leq 15V$	$\pm(\|V_{CC}\|-1)V$
differential input voltage		±3V
junction temperature		+175°C
operating temperature range		
	AI:	−25°C to + 85°C
	A8/AK:	− 55°C to +125°C
storage temperature		−65°C to +150°C
lead temperature (soldering 10s)		+300°C

Recommended Operating Conditions

V_{CC}	±5V to ±15V
I_{out}	±100ma
V_{CM}	$\pm(\|V_{CC}\|-5)V$
gain range	+7 to +50, −1 to −50

Notes:

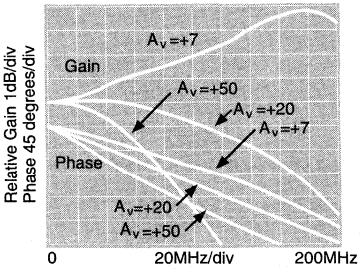
note 1: Parameters preceded by an * are 100% tested. A8 and AK units are tested at –55°C, +25°C and +125°C. AI units are tested at +25°C, though performance at –25°C and +85°C is guaranteed as shown above.

note 2: Settling time specifications require the use of an external feedback resistor (2kΩ).

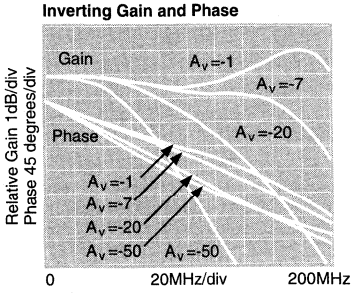
note 3: In AI units, the noise specifications are guaranteed (but not tested) as shown above. A8 and AK units tested with $R_L = 200\Omega$.

Typical Performance Characteristics (T_A=25°C; A_V=+20; V_{CC}=±16V; R_L=200Ω; R_f=2kΩ)

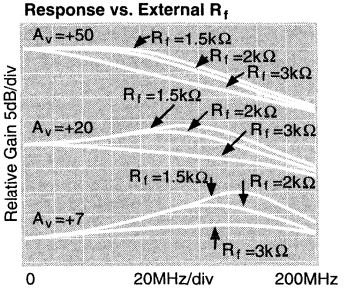
Non-Inverting Gain and Phase



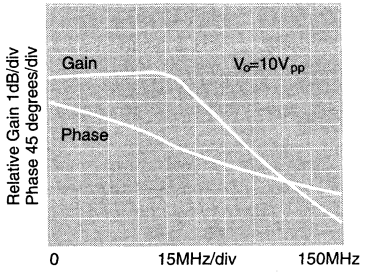
Inverting Gain and Phase



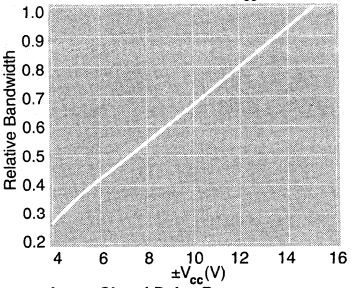
Response vs. External R_f



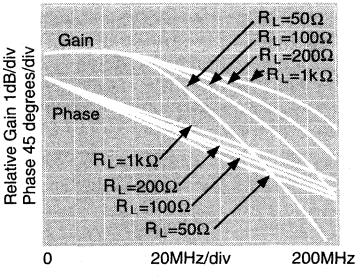
Large Signal Gain and Phase



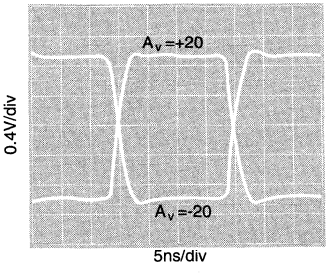
Relative Bandwidth vs. V_{cc}



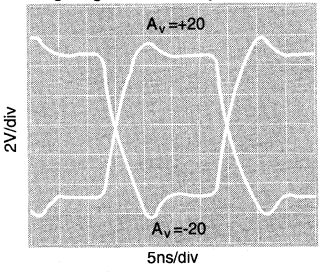
Gain and Phase for Various Loads



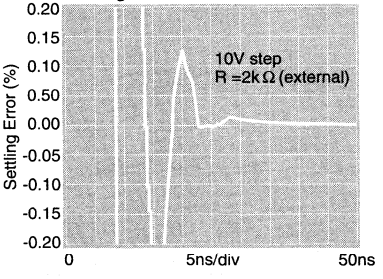
Small Signal Pulse Response



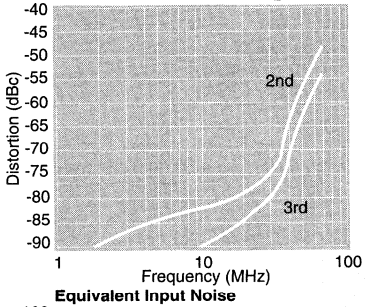
Large Signal Pulse Response



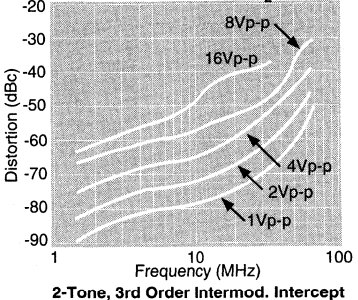
Settling Time



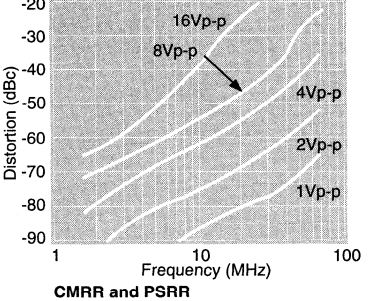
2nd and 3rd Harmonic Distqrtion



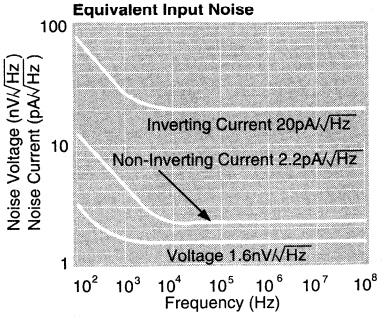
2nd Harmonic Distortion, R_L=100Ω



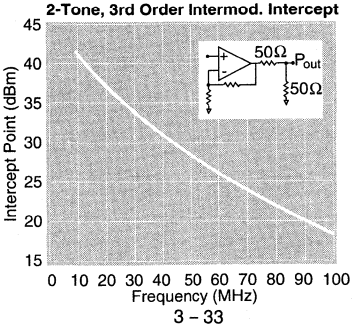
3rd Harmonic Distortion, R_L=100Ω



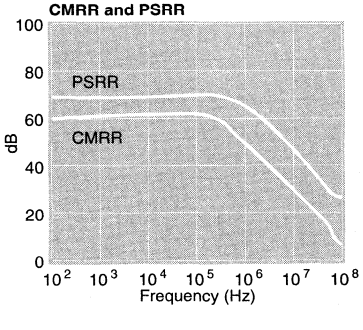
Equivalent Input Noise



2-Tone, 3rd Order Intermod. Intercept



CMRR and PSRR



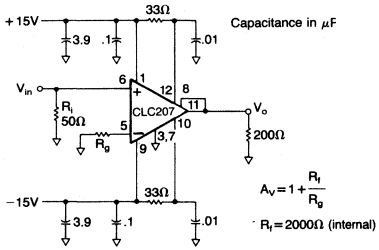


Figure 1: recommended non-inverting gain circuit

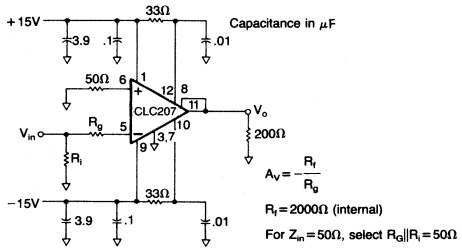


Figure 2: recommended inverting gain circuit

Test fixture schematics are available upon request.

Overdrive Protection

Unlike most other high-speed op amps, the CLC207 is not damaged by saturation caused by overdriving input signals (where $V_{in} \times gain > max.V_{out}$). The CLC207 self limits the current at the inverting input when the output is saturated (see the inverting input current self limit specification); this ensures that the amplifier will not be damaged due to excessive internal currents during overdrive. For protection against input signals which would exceed either the maximum differential or common mode input voltage, the diode clamp circuits below may be used.

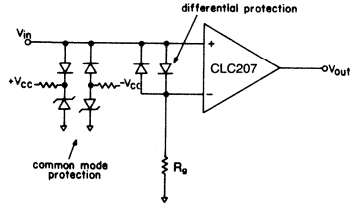


Figure 3: diode clamp circuits for common mode and differential mode protection

Short Circuit Protection

Damage caused by short circuits at the output may be prevented by limiting the output current to safe levels. The most simple current limit circuit calls for placing resistors between the output stage collector supplies and the output stage collectors (pins 12 and 10). The value of this resistor is determined by:

$$R_c = V_c / I_l - R_l$$

Where I_l is the desired limit current and R_l is the minimum expected load resistance (0Ω for a short to ground). Bypass capacitors of 0.01μF on should be used on the collectors as in Figures 1 and 2.

A more sophisticated current limit circuit which provides a limit current independent of R_l is shown below.

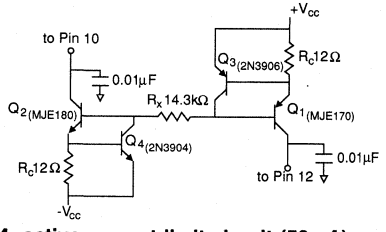


Figure 4: active current limit circuit (50mA)

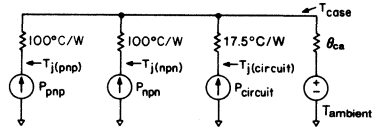
With the component values indicated, current limiting occurs at 50mA. For other values of current limit (I_l), select R_c to equal V_{be}/I_l. Where V_{be} is the base to emitter voltage drop of Q3 (or Q4) at a current of $[2V_{cc}-1.4]/R_x$, where $R_x \leq [(2V_{cc}-1.4)/I_l]\ B_{min}$. Also, B_{min} is the minimum beta of Q1 (or Q2) at a current of I_l. Since the limit current depends on V_{be}, which is temperature dependent, the limit current is likewise temperature dependent. If a temperature-independent current limit circuit is needed, contact Comlinear.

Controlling Bandwidth and Passband Response

In most applications, a feedback resistor value of 2kΩ will provide optimum performance; nonetheless, some applications may require a resistor of some other value. The response versus R_f plot on the previous page shows how decreasing R_f will increase bandwidth (and frequency response peaking, which may lead to instability). Conversely, large values of feedback resistance tend to roll off the response.

The best settling time performance requires the use of an external feedback resistor. (Use of the internal resistor results in 0.1% to 0.2% settling tail.) The settling performance may be improved slightly by adding a capacitance of 0.4pF in parallel with the feedback resistor. (Settling time specifications reflect performance with an external feedback resistor but with no external capacitance.)

Thermal Model



$P_{circuit} = [(+V_{cc}) - (-V_{cc})]^2 / 1.77k\Omega$

$P_{xxx} = [(\pm V_{cc}) - V_{out} - (I_{col})\ (R_{col}+6)]\ (I_{col})$
(% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)
(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

θ_{ca} = 65°C/W in still air without a heatsink
35°C/W in still air with a Thermalloy 2268B
15°C/W in 300ft/min air with a Thermalloy 2268B
(Thermalloy 2240 works equally well.)

$I_{col} = V_{out}/R_{load}$ or 3mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\ (pnp)} = P_{pnp}(200 + \theta_{ca}) + (P_{cir} + P_{npn})\ \theta_{ca} + T_a$,
similar for $T_{j\ (npn)}$.

$T_{j\ (cir)} = P_{cir}(17.5 + \theta_{ca}) + (P_{pnp} + P_{npn})\ \theta_{ca} + T_a$.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance the performance of the CLC207. Good ground plane construction and power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal stray capacitance to the ground plane or other nodes. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Evaluation PC boards (part number 730008 for inverting, 730009 for non-inverting) for the CLC207 are available from Comlinear at minimal cost.

Comlinear Corporation

Fast Settling, Wideband Operational Amplifiers

CLC220

APPLICATIONS:

- very high speed D to A, A to D conversion
- high speed fiber optics systems
- baseband and video communications
- radar and IF processors
- very fast risetime pulse amplifiers

FEATURES:

- −3dB bandwidth of 190MHz
- 0.1% settling in 8ns
- 7000V/μs slew rate
- 1.9ns rise and fall times
- low distortion, linear phase

DESCRIPTION:

The CLC220 is a wide bandwidth DC-coupled operational amplifier that defines the state-of-the-art in high speed op amps. A −3dB bandwidth of DC to 190MHz is achieved using a proprietary Comlinear design. **Ultra-fast settling time (8nsec to 0.1%) and slew rate (7000V/μsec)** make the CLC220 a superior amplifier for pulsed and digital applications.

Since thermal tail has been eliminated, the CLC220 settles fast and remains solidly at the desired level. Flat gain and linear phase (1.2° deviation from linear) from DC to beyond 100MHz help the CLC220 to achieve distortion levels uncommonly low relative to conventional op amps.

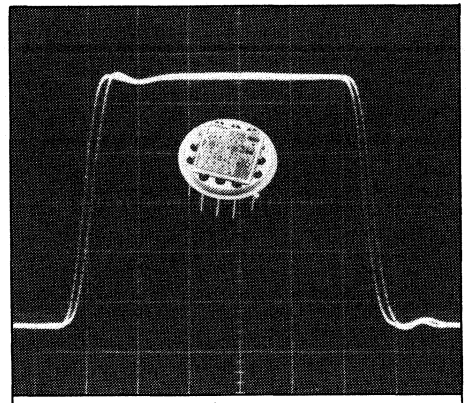
Using the CLC220 is as easy as adding power supplies and a gain-setting resistor. The result is reliable, consistent performance because such characteristics as bandwidth and settling time are virtually independent of gain setting. Unlike conventional op amp designs where the optimum gain-bandwidth product occurs at a high gain, minimum settling time at a gain of −1, maximum slew rate at a gain of +1, et cetera, the CLC220 offers predictable response at gain settings from ±1 to ±50. This, coupled with consistent performance from unit to unit with **no external compensation**, makes the CLC220 a real time and cost-saver in design and production situations alike.

This combination of features makes the CLC220 appropriate for a broad range of applications. The wide bandwidth, DC coupling, and fast settling lend themselves well to high speed D to A and "flash" A to D applications. Both receivers and transmitters in optical fiber systems have similar requirements. High **gain and phase linearity and corresponding low distortion** make the CLC220 ideal for many digital communication system applications, such as in the demodulator, where the need for both DC coupling and high frequency amplification creates requirements that are difficult to meet.

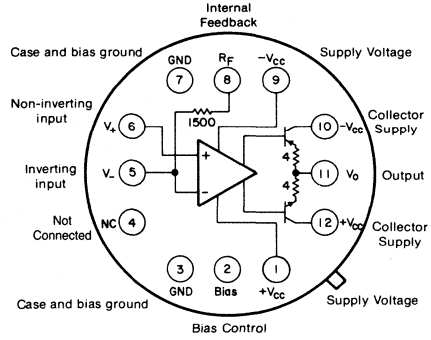
The CLC220 is constructed using thin-film resistor/bipolar transistor technology. The CL220AI is specified over a temperature range of –25°C to +85°C, while the CLC220A8C is specified over a range of –55°C to +125°C and is fully compliant with MIL-STD-883, Level B. Both devices are packaged in 12-pin metal TO-8 cans. The DESC SMD number is 5962-89911.

Typical Performance

parameter	gain setting +4	+20	+50	−4	−20	−50	units
−3dB bandwidth	250	190	120	200	190	150	MHz
rise time (2V)	1.6	1.9	2.3	1.6	1.9	2.3	ns
slew rate	7	7	7	7	7	7	V/ns
settling time (0.1%)	10	8	10	8	8	10	ns

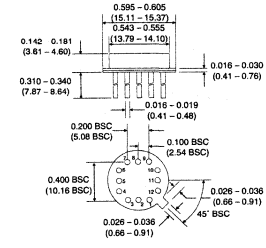


BOTTOM VIEW



Pin 8 provides access to a 1500 ohm feedback resistor. Pin 2 allows the user to reduce the amplifier supply current or to turn the amplifier off completely.

Package Dimensions



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January 1993

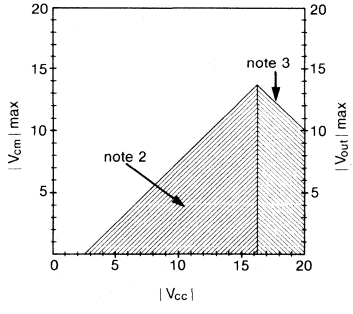
DS220.06

Electrical Characteristics (A_V = +20, V_{CC} = ±15V, R_L = 200Ω, R_f = 1500Ω)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	CLC220AI	+25°C	−25°C	+25°C	+85°C		
Ambient Temperature	CLC220A8	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
*−3dB bandwidth	V_{out}<2V_{pp}	190	>160	>170	>150	MHz	SSBW
gain flatness at	V_{out}<2V_{pp}						
* peaking	0.1 to 50MHz	0	<0.5	<0.3	<0.4	dB	GFPL
* peaking	>50MHz	0	<1.5	<0.6	<1.0	dB	GFPH
* rolloff	at 100MHz	0	<0.4	<0.6	<0.9	dB	GFR
group delay	to 100MHz	3.0±0.3	—	—	—	ns	GD
linear phase deviation	to 100MHz	1.2	<2	<2	<2	°	LPD
reverse isolation	to 100MHz						
non-inverting		60	>50	>50	>50	dB	RINI
inverting		45	>35	>35	>35	dB	RIIN
TIME DOMAIN RESPONSE							
rise and fall time	2V step	1.9	<2.2	<2.1	<2.2	ns	TRS
	5V step	2	<2.6	<2.5	<2.6	ns	TRL
settling time to .02%	5V step[4]	15	—	—	—	ns	TSP
to .1%	5V step[4]	8	<15	<12	<15	ns	TS
overshoot	5V step	7	<15	<12	<12	%	OS
slew rate (overdriven input)		7	>6	>6	>6	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		25	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
*2nd harmonic distortion	2V_{pp}, 20MHz	−58	<−50	<−50	<−50	dBc	HD2
*3rd harmonic distortion	2V_{pp}, 20MHz	−62	<−50	<−50	<−50	dBc	HD3
equivalent noise input							
noise floor	>100kHz	−156	<−150	<−150	<−150	dBm(1Hz)	SNF
integrated noise	1kHz to 200MHz	50	<100	<100	<100	μV	INV
noise floor	>5MHz	−156	<−150	<−150	<−150	dBm(1Hz)	SNF
integrated noise	5MHz to 200MHz	50	<100	<100	<100	μV	INV
STATIC DC PERFORMANCE							
*input offset voltage		10	<25	<25	<25	mV	VIO
average temperature coefficient[1]		35	<120	<120	<120	μV/°C	DVIO
*input bias current	non-inverting	10	<40	<30	<40	μA	IBN
average temperature coefficient[1]		20	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	20	<70	<50	<70	μA	IBI
average temperature coefficient[1]		70	<250	<250	<250	nA/°C	DIBI
*power supply rejection ratio		55	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
*supply current	no load	30	<36	<34	<36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	>100	>100	>100	kΩ	RIN
	capacitance	2.4	<3	<3	<3	pF	CIN
output impedance	at DC	—	<0.1	<0.1	<0.1	Ω	RO
	at 100MHz	1, 35	—	—	—	Ω, nH	ZO
output voltage range	no load	—	>±10	>±10	>±10	V	VO
internal feedback resistor	absolute tolerance	<0.4	—	—	—	%	RFA

Absolute Maximum Ratings

Common Mode and Output Voltage Limits



supply voltage (V_{CC})	±20V
output current	±50mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
	A8: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

***note 1:** Parameters preceded by an * are the final electrical test parameters and are 100% tested. A8 units are tested at –55°C, +25°C, +125°C. AI units are tested only at +25°C although performance at –25°C and +85°C is guaranteed to be better than or equal to the performance specified for A8 devices in the –55°C and +125°C ranges. Maximum temperature coefficient parameters apply only to A8 devices.

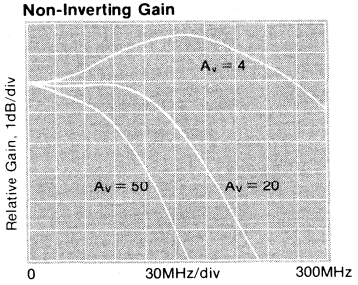
note 2: This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10%), maximum input voltage may be as large as twice the maximum. V_{cm} should never exceed V_{cc} (V_{cm} is the voltage at the non-inverting input, pin 6).

note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{cc} is ± 15V.

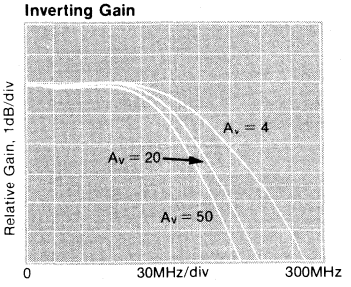
note 4: Settling time specification requires the use of an external feedback resistor (1500Ω).

Typical Performance Characteristics ($T_A = 25°C$, $A_V = 20$, $V_{cc} = \pm 15V$, $R_L = 200\Omega$)

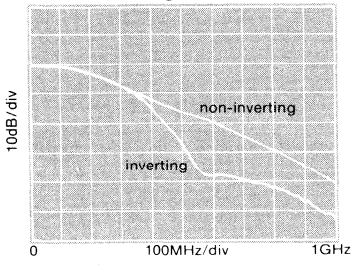
Non-Inverting Gain



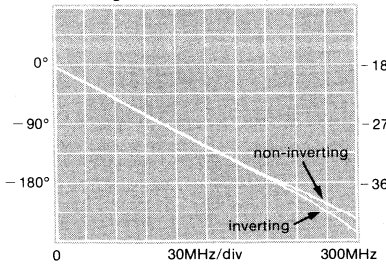
Inverting Gain



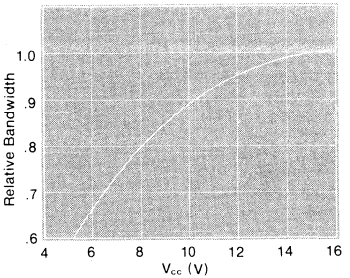
Broadband Inverting and Non-Inverting Gain



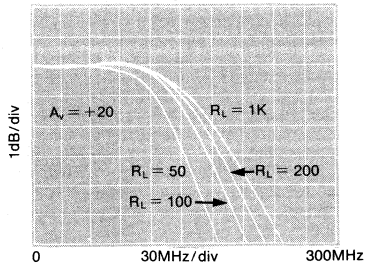
Inverting and Non-Inverting Phase



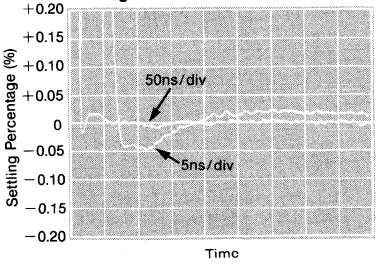
Relative Bandwidth vs. V_{cc}



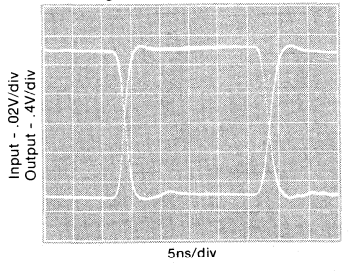
Gain vs. Frequency for Various R_{LS}



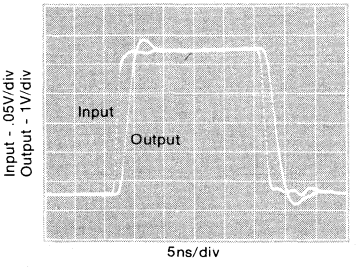
Settling Time



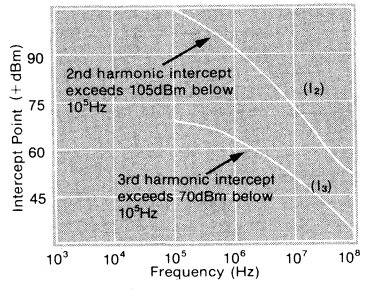
Small Signal Pulse Response (Inv, Non-Inv)



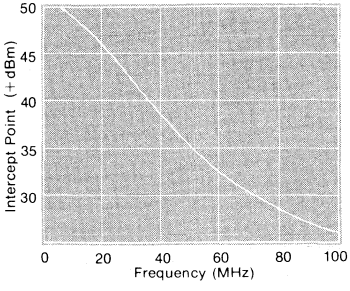
Large Signal Pulse Response



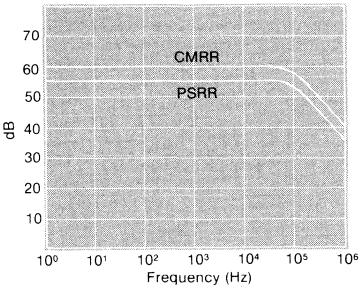
2nd and 3rd Harmonic Distortion Intercept



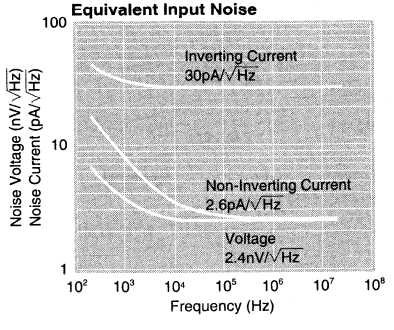
2-Tone 3rd Order Intermod. Intercept

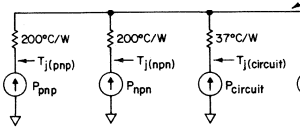


CMRR and PSRR



Equivalent Input Noise





θ_{ca} = 65°C/W in still air without a heatsink
30°C/W in still air with a Thermalloy 2268
15°C/W in 300ft/min air with a Thermalloy 2268

$P_{circuit} = I_{cc}[(+V_{cc}) - (-V_{cc})]$ where $I_{cc} = 26mA$ at $\pm 15V$

$P_{Xxx} = [(\pm V_{cc}) - V_{out} - (I_{col})(R_{col} + 4)](I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 4mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\,(pnp)} = P_{pnp}(200 + \theta_{ca}) + (P_{cir} + P_{npn})\,\theta_{ca} + T_a$, similar for $T_{j\,(npn)}$.

$T_{j\,(cir)} = P_{cir}(37 + \theta_{ca}) + (P_{pnp} + P_{npn})\,\theta_{ca} + T_a$.

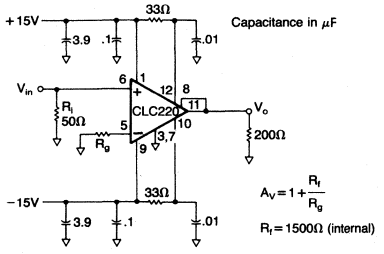


Figure 1: suggested non-inverting gain circuit

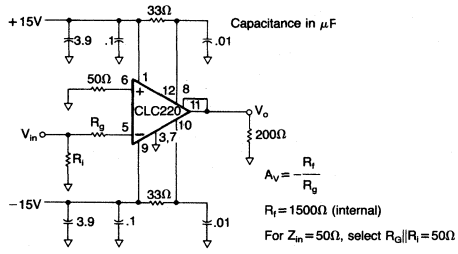


Figure 2: suggested inverting gain circuit

Test fixture schematics are available upon request.

Controlling Bandwidth and Passband Response

As with any op amp, the ratio of the two feedback resistors R_f and R_g determines the gain of the CLC220. Unlike conventional op amps, however, the closed loop pole-zero response of the CLC220 is affected very little by the value of R_g. R_g scales the magnitude of the gain, but does not change the value of the feedback. This is possible due to a proprietary circuit topology. R_f does influence the feedback and so the CLC220 has been internally compensated for optimum performance with $R_f = 1500\Omega$. External R_f values greater than 1500Ω can be used with approximate results as listed in Table 1. Use of R_f values less than 1500Ω will result in extended bandwidth and peaking of the response at high frequencies. For example, $R_f = 1000\Omega$ will result in a −3dB bandwidth of about 300MHz, with approximately 3.5dB of peaking above 200MHz. An RC network with a −3dB bandwidth of about 250MHz could be used at the input to flatten the response, although it will reduce the bandwidth of the overall circuit.

Table 1: Bandwidth versus R_f

R_f (kΩ)	$f \pm 0.3$dB (MHz)	$f - 3.0$dB (MHz)
2	25	80
5	10	30
10	5	15

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{cc} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in Figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available from Comlinear at minimal cost.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

Distortion and Amplification Fidelity

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the CLC220. First, convert the output voltage (V_O) to $V_{RMS} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{RMS}^2))$ to get output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below P, as will the two-tone third order intermodulation products. These approximations are useful for $P < -1$dB compression levels.

Approximate noise figure can be determined for the CLC220 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current at the inverting node. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

For linear operation of the CLC220 at large output voltage swings (DC component not included) and at high frequencies, observe the (AC output voltage) X (frequency) product specification of 600V • MH_Z. Exceeding this rating will cause the signal to be greatly distorted as the amplifier bias control circuit reduces the current available for slewing to prevent damage. At frequencies and voltages within this range the excess slew rate and bandwidth available will ensure the highest possible degree of amplified signal fidelity.

Operation with Reduced Bias Current

Placing a resistor between pins 1 and 2 will cause the CLC220 bias current to be reduced. A value of 20K will cause only a slight reduction, 3K will almost halve the current, while less than 1K will reduce bias to about 5mA and the amplifier will be off. In this condition, the input signal will be greatly attenuated. In the reduced bias, on condition, bandwidth will be roughly proportional to the reduction in bias current. A mechanical or semiconductor switch can be used to turn the amplifier off. Any connection which would cause current to flow out of pin 2 will result in increased bias current and may lead to device destruction from overheating and excessive current.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly qualified applications engineers to provide technical and design assistance.

Comlinear Corporation

Fast Settling, Wideband Operational Amplifiers

CLC221

APPLICATIONS:

- very high speed D to A, A to D conversion
- high speed fiber optics systems
- baseband and video communications
- radar and IF processors
- very fast risetime pulse amplifiers

FEATURES (typical):

- −3dB bandwidth of 170MHz
- 0.5mV input offset voltage, 5μV/°C drift
- 0.1% settling in 15ns
- 6500V/μs slew rate
- 2.1ns rise and fall times

DESCRIPTION:

The CLC221 is a wideband operational amplifier designed for the most demanding high-speed applications. State of the art specifications such as the **6500V/μs slew rate and 15ns settling time** (to 0.1%) make the CLC221 an excellent choice when system speed is a key concern. In addition to the dynamic parameters, the CLC221 has excellent DC performance; the input offset voltage, for example, is typically only 0.5mV and is guaranteed to be less than 1.0mV at +25°C. **The input offset voltage drift is typically only 0.5μV/°C.** With this combination of AC and DC parameters, designers are now free of the speed versus accuracy trade-offs common to most high-speed op amps.

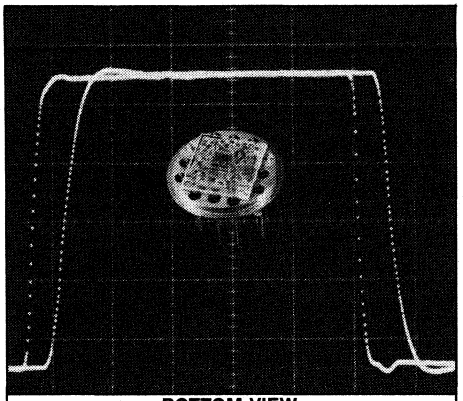
The wide bandwidth, DC coupling, and fast settling lend themselves well to high-speed D to A and "flash" A to D applications. Flat gain and phase response and corresponding low distortion make the CLC221 ideal for many digital system applications, such as in the demodulator where the need for both DC coupling and high-frequency amplification creates requirements that are difficult to meet. Engineers desiring to increase the DC performance or large-signal bandwidth of systems using the original CLC220 may replace it with a CLC221 – in most cases with no design changes (they are pin compatible, however the CLC221 does not have a bias control pin).

The dynamic specifications of the CLC221 are due to Comlinear's proprietary op amp topology, a unique design which provides dynamic performance far beyond that of conventional designs. Unlike conventional designs which show vast performance variations over different gains, the CLC221 provides consistent, predictable performance across its entire gain range (see the table below) and since **the amplifier is inherently stable, no external compensation is required.** The result is shorter design time and the ability to accommodate design changes (in gain, for example) without redesign of compensation circuits or loss of performance.

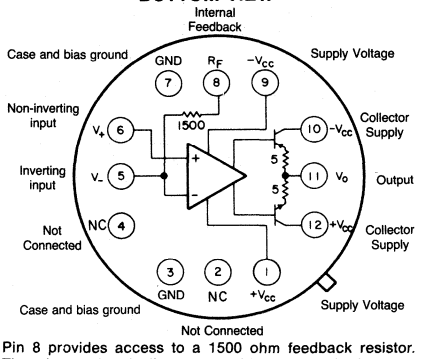
The CLC221 is constructed using thin-film resistor/bipolar transistor technology. The CLC221AI is specified over a temperature range of −25°C to +85°C, while the CLC221A8C is specified over a range of −55°C to +125°C and is fully compliant with MIL-STD-883, Level B. Both devices are packaged in 12-pin metal TO-8 cans. The DESC SMD number is 5962-90836.

Typical Performance

	gain setting						
parameter	+4	+20	+50	−4	−20	−50	units
−3dB bandwidth	250	170	110	200	160	110	MHz
rise time (2V)	1.6	2.1	2.5	1.6	2.1	2.5	ns
slew rate	6.5	6.5	6.5	6.5	6.5	6.5	V/ns
settling time (0.1%)	—	15	16	15	15	16	ns

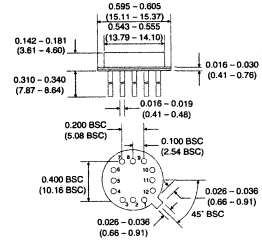


BOTTOM VIEW



Pin 8 provides access to a 1500 ohm feedback resistor. Though not electrically connected to the circuit, the case provides EMI shielding and should be connected to a low impedance signal return.

Package Dimensions



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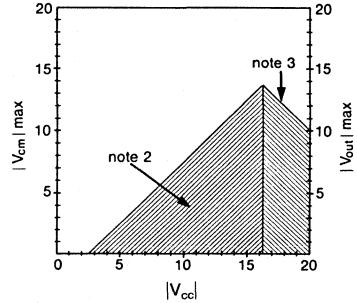
Electrical Characteristics (A_V = +20, V_{CC} = ±15V, R_L = 200Ω, R_f = 1500Ω)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	CLC221A8[1]	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC221AI[1]	+25°C	−25°C	+25°C	+ 85°C		
FREQUENCY DOMAIN RESPONSE							
*−3dB bandwidth	V_{out}<2V_{pp}	170	>150	>150	>125	MHz	SSBW
gain flatness at	V_{out}<2V_{pp}						
* peaking	0.1 to <40MHz	0	<0.5	<0.3	<0.5	dB	GFPL
* peaking	>40MHz	0	<1.5	<0.6	<1.0	dB	GFPH
* rolloff	at 75MHz	0	<0.4	<0.6	<0.9	dB	GFR
group delay	to 75MHz	3.0±0.3	—	—	—	ns	GD
linear phase deviation	to 75MHz	1	<2.5	<2	<3	°	LPD
reverse isolation	to 100MHz						
non-inverting		60	>50	>50	>50	dB	RINI
inverting		45	>35	>35	>35	dB	RIIN
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.1	<2.5	<2.5	<3.0	ns	TRS
	5V step	2.1	<2.5	<2.5	<3.0	ns	TRL
settling time to .02%	5V step	18	—	—	—	ns	TSP
to .1%	5V step	15	<25	<20	<20	ns	TS
overshoot	5V step	7	<15	<12	<12	%	OS
slew rate (overdriven input)		6.5	>5	>5	>5	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		25	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
*2nd harmonic distortion	2V_{pp}, 20MHz	−58	<−50	<−50	<−50	dBc	HD2
*3rd harmonic distortion	2V_{pp}, 20MHz	−62	<−50	<−50	<−50	dBc	HD3
equivalent noise input							
noise floor	>100kHz	−156	<−150	<−150	<−150	dBm(1Hz)	SNF
integrated noise	1kHz to 200MHz	50	<100	<100	<100	μV	INV
noise floor	>5MHz	−156	<−150	<−150	<−150	dBm(1Hz)	SNF
integrated noise	5MHz to 200MHz	50	<100	<100	<100	μV	INV
STATIC DC PERFORMANCE							
*input offset voltage		0.5	<2.2	<1	<2.5	mV	VIO
average temperature coefficient		5	<15	<15	<15	μV/°C	DVIO
*input bias current	non-inverting	5	<36	<20	<20	μA	IBN
average temperature coefficient		50	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	5	<26	<10	<30	μA	IBI
average temperature coefficient		50	<200	<200	<200	nA/°C	DIBI
*power supply rejection ratio		55	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
*supply current	no load	30	<36	<34	<36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	>100	>100	>100	kΩ	RIN
	capacitance	2.4	<3	<3	<3	pF	CIN
output impedance	at DC	—	<0.1	<0.1	<0.1	Ω	RO
	at 75MHz	1, 35	—	—	—	Ω, nH	ZO
output voltage range	no load	—	>±10	>±10	>±10	V	VO
internal feedback resistor	absolute tolerance	<0.4	—	—	—	%	RFA

Absolute Maximum Ratings

Common Mode and Output Voltage Limits



supply voltage (V_{cc})	±20V
output current	±50mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
	A8: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

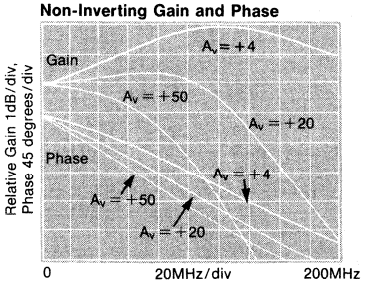
***note 1:** Parameters preceded by an * are the final electrical test parameters and are 100% tested. A8 units are tested at −55°C, +25°C, +125°C. AI units are tested only at +25°C although performance at −25°C and +85°C is guaranteed as indicated above.

note 2: This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10%), maximum input voltage may be as large as twice the maximum. V_{cm} should never exceed V_{cc}(V_{cm} is the voltage at the non-inverting input, pin 6).

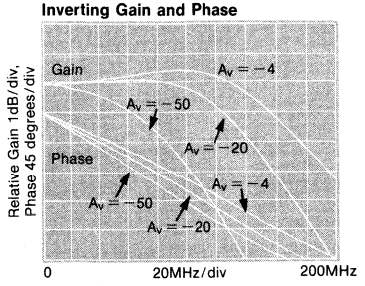
note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{cc} is ± 15V.

Typical Performance Characteristics ($T_A = 25°C$, $A_V = +20$, $V_{CC} = \pm 15V$, $R_L = 200\Omega$)

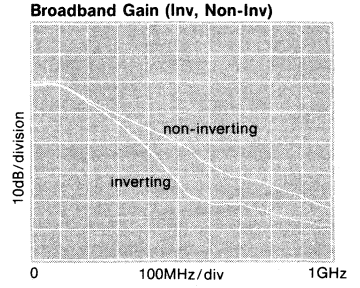
Non-Inverting Gain and Phase



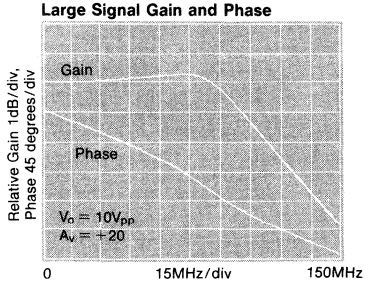
Inverting Gain and Phase



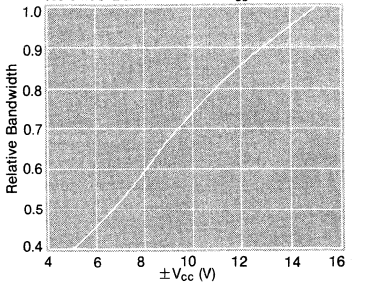
Broadband Gain (Inv, Non-Inv)



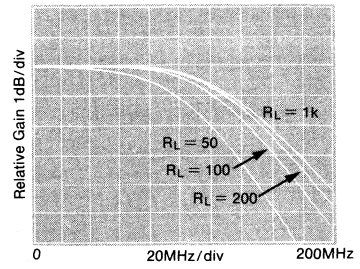
Large Signal Gain and Phase



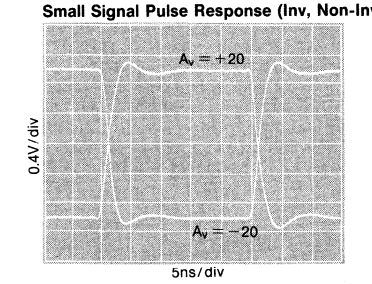
Relative Bandwidth vs. V_{cc}



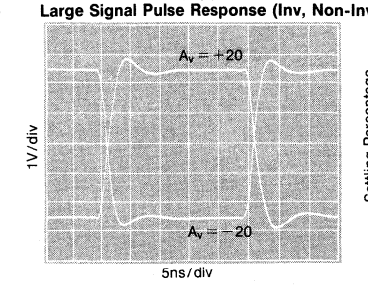
Gain vs. Frequency for Various R_Ls



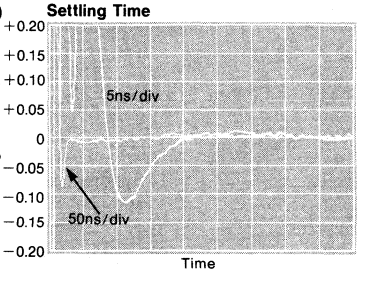
Small Signal Pulse Response (Inv, Non-Inv)



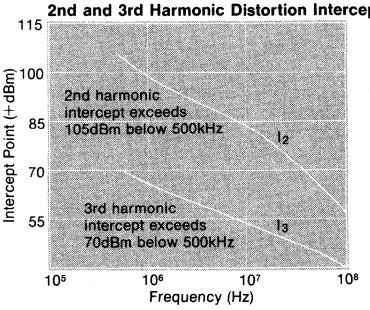
Large Signal Pulse Response (Inv, Non-Inv)



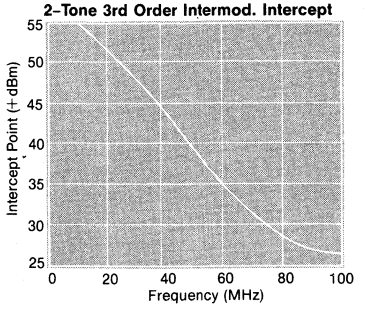
Settling Time



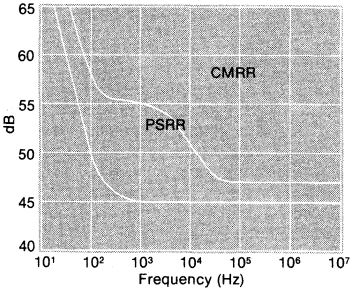
2nd and 3rd Harmonic Distortion Intercept



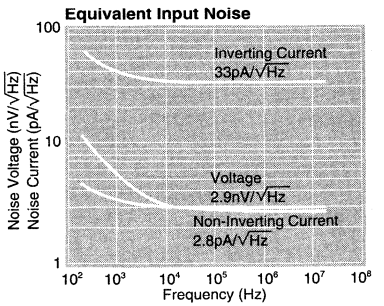
2-Tone 3rd Order Intermod. Intercept

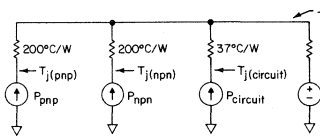


CMRR and PSRR



Equivalent Input Noise





θ_{ca}=65°C/W in still air without a heatsink
35°C/W in still air with a Thermalloy 2268
30°C/W in 300ft/min air with a Thermalloy 2268
(Thermalloy 2240 works equally well.)

$P_{circuit} = I_{cc}\,[(+V_{cc}) - (-V_{cc})]$ where $I_{cc} = 26mA$ at $\pm 15V$

$P_{xxx} = [(\pm V_{cc}) - V_{out} - (I_{col})\,(R_{col} + 5)]\,(I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 4mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\,(pnp)} = P_{pnp}\,(200 + \theta_{ca}) + (P_{cir} + P_{npn})\,\theta_{ca} + T_a$, similar for $T_{j\,(npn)}$.

$T_{j\,(cir)} = P_{cir}\,(37 + \theta_{ca}) + (P_{pnp} + P_{npn})\,\theta_{ca} + T_a$.

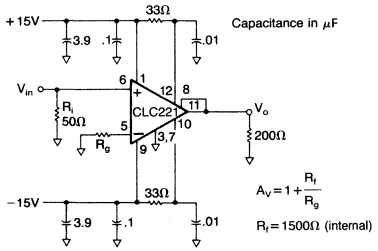


Figure 1: suggested non-inverting gain circuit

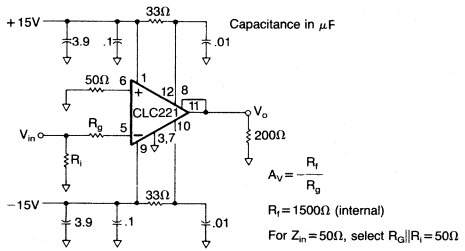


Figure 2: suggested inverting gain circuit

Test fixture layout artwork is available upon request.

CLC221 Operation

The CLC221 is based on Comlinear's proprietary op amp topology, a unique design that uses current feedback instead of the usual voltage feedback. This design provides dynamic performance far beyond that previously available, yet it is used basically the same as the familiar voltage-feedback op amp (see the gain equations above). A complete discussion of current feedback is given in application note AN300-1.

Controlling Bandwidth and Passband Response

In most applications, use of the internal 1500Ω feedback resistor will provide optimum dynamic performance; nonetheless, some designs may require an external feedback resistor of some value other than 1500Ω. The table below shows how bandwidth depends on the value of R_f. Values of feedback resistance greater than 1500Ω will decrease the bandwidth of the amplifier; values of R_f less than 1500Ω will increase the bandwidth (At most gain settings, however, low values of R_f may cause instability unless a small amount of compensation capacitance (typically <0.5pF) is connected in parallel with R_f. At $|A_v| < 20$, R_f must be greater than 1kΩ).

Bandwidth versus R_f

R_f (external)	−3dB Bandwidth (A_v = 20)
1.5kΩ	150MHz
2kΩ	100MHz
3kΩ	60MHz
5kΩ	30MHz

At large closed-loop gains ($|A_v| \geq 50$) the bandwidth may be increased by using a low value of R_f as the table below indicates. External compensation is not required under these high-gain conditions.

Increasing Bandwidth at High Gains

$\|A_v\|$	R_f	−3dB Bandwidth
50	500Ω	130MHz

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{cc} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in Figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available from Comlinear.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

Distortion, Noise, and Amplification Fidelity

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the CLC221. First, convert the output voltage (V_O) to $V_{RMS} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{RMS}^2))$ to get output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below P, as will the two-tone third order intermodulation products. These approximations are useful for P<−1dB compression levels.

Approximate noise figure can be determined for the CLC221 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current at the inverting node. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

For linear operation of the CLC221 at large output voltage swings (DC component not included) and at high frequencies, limit the (AC output voltage) × (frequency) product to 1600V·MHz. Exceeding this rating will cause the signal to be greatly distorted as the amplifier bias control circuit reduces the current available for slewing to prevent damage. At frequencies and voltages within this range the excess slew rate and bandwidth available will ensure the highest possible degree of amplified signal fidelity.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly qualified applications engineers to provide technical and design assistance.

Comlinear Corporation

Fast Settling, Wideband Buff-Amp™ ($A_V = \pm 1$ to ± 5)

CLC231

APPLICATIONS:

- driving flash A/D converters
- precision line driving
  (a gain of 2 cancels matched-line losses)
- DAC current-to-voltage conversion
- low-power, high-speed applications (50mW @ ± 5V)

FEATURES:

- 165MHz closed-loop −3dB bandwidth
- 15ns settling to .05%
- 1mV input offset voltage, 10μV/°C drift
- 100mA output current
- excellent AC and DC linearity

DESCRIPTION:

The CLC231 Buff-Amp™ is a wideband operational amplifier **designed specifically for high-speed, low-gain applications.** The CLC231 is based on Comlinear's proprietary op amp topology—a unique design that both eliminates the gain-bandwidth tradeoff and permits unprecedented high-speed performance. (See table below.)

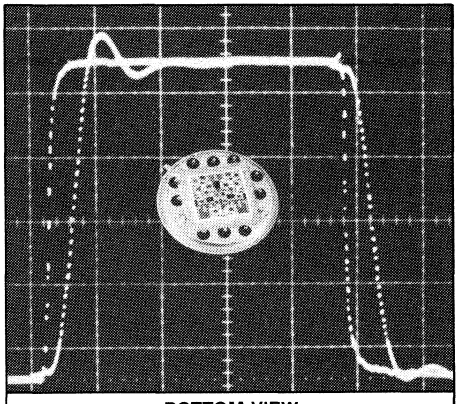
The CLC231 Buff-Amp™ is the **ideal design alternative to low-precision open-loop buffers and oscillation-prone conventional op amps.** The CLC231 offers precise gains from ±1.000 to ±5.000 and linearity that is a true .1%—even for demanding 50 ohm loads. Open-loop buffers, on the other hand, offer a nominal gain of .95 ± .03 and a linearity of only 3% for typical loads. A buffer's settling time may look impressive but it is usually specified at unrealistically large load resistances or when the effects of thermal tail are not included; the CLC231 Buff-Amp™ settles to .05% in 15ns—while driving a 100 ohm load.

Offsets and drifts, usually a low priority in conventional high-speed op amp designs, were not ignored in the CLC231; the input offset voltage is typically 1mV and **input offset voltage drift is only 10μV/°C.** The CLC231 is stable and oscillation-free across the entire gain range and since it's **internally compensated,** the user is saved the trouble of designing external compensation networks and having to "tweak" them in production. The absence of a gain-bandwidth tradeoff in the CLC231 allows performance to be predicted easily; the table below shows how the bandwidth is affected very little by changing the gain setting.

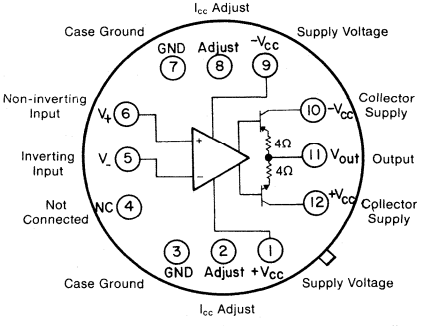
The CLC231 is constructed using thin-film resistor/bipolar transistor technology and is available in three versions. The CLC231AI is specified over a temperature range of –25°C to +85°C. The CLC231AK, which features burn-in and tested hermeticity, is specified and tested over a temperature range of –55°C to +125°C. The CLC231A8C is specified and tested over a temperature range of –55°C to +125°C and is fully compliant with MIL-STD-883, Level B. All three versions are packaged in metal 12-pin TO-8 cans. The DESC SMD number is 5962-89594.

Typical Performance

parameter	gain setting 1	2	5	−1	−2	−5	units
−3dB bandwidth	180	165	130	165	150	115	MHz
rise time (2V)	1.8	2.0	2.5	2.0	2.2	2.9	ns
slew rate	2.5	3	3	3	3	3	V/ns
settling time (to .1%)	12	12	12	12	12	15	ns

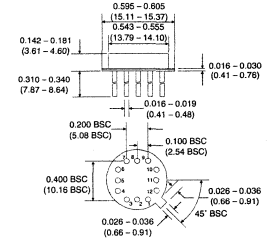


BOTTOM VIEW



Pins 2 and 8 are used to adjust the supply current or to adjust the offset voltage (see text). These pins are normally left unconnected.

Package Dimensions



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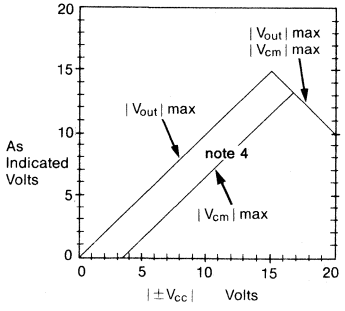
Electrical Characteristics (R_L = 100Ω, R_f = 250Ω, V_{cc} = ±15V, A_v = +2)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC231A8/AK	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC231AI	+25°C	−25°C	+25°C	+85°C		
FREQUENCY DOMAIN PERFORMANCE							
* −3dB bandwidth note 2	$V_{out}\leq 2V_{pp}$	165	>145	>145	>120	MHz	SSBW
	$V_{out}\leq 10V_{pp}$	95	>80	>80	>60	MHz	FPBW
gain flatness note 2	$V_{out}\leq 2V_{pp}$						
* peaking	0.1 to 50MHz	0.1	<0.6	<0.3	<0.6	dB	GFPL
* peaking	>50MHz	0.1	<1.5	<0.3	<0.8	dB	GFPH
* rolloff	at 100MHz	0.4	<0.6	<0.6	<1.0	dB	GFR
group delay	to 100MHz	3.5±0.5	—	—	—	ns	GD
linear phase deviation	to 100MHz	0.5	<2	<2	<2	°	LPD
reverse isolation	to 100MHz						
non-inverting		53	>43	>43	>43	dB	RINI
inverting		36	>26	>26	>26	dB	RIIN
TIME DOMAIN PERFORMANCE							
rise and fall time	2V step	2	<2.4	<2.3	<2.7	ns	TRS
	10V step	5.0	<7.0	<6.5	<6.5	ns	TRL
settling time to .05%	5V step	15	—	—	—	ns	TS
to .1%	2.5V step	12	<22	<17	<22	ns	TSP
overshoot	5V step	5	<15	<10	<15	%	OS
slew rate (overdriven input)		3	>2.5	>2.5	>1.8	V/ns	SR
overload recovery	<1% error						
<50ns pulse, 200% overdrive		120	—	—	—	ns	OR
DISTORTION AND NOISE PERFORMANCE							
* 2nd harmonic distortion	0dBm, 20MHz	−55	<−47	<−47	<−47	dBc	HD2
* 3rd harmonic distortion	0dBm, 20MHz	−59	<−47	<−47	<−47	dBc	HD3
equivalent input noise							
noise floor	>5MHz	−153	<−150	<−150	<−150	dBm(1Hz)	SNF
integrated noise	5MHz to 200MHz	70	<100	<100	<100	μVrms	INV
STATIC, DC PERFORMANCE							
* input offset voltage		1	<4.0	<2.0	<4.5	mV	VIO
temperature coefficient		10	<25	<25	<25	μV/°C	DVIO
* input bias current	non-inverting	5	<29	<21	<31	μA	IBN
temperature coefficient		50	<125	<125	<125	nA/°C	DIBN
* input bias current	inverting	10	<31	<15	<35	μA	IBI
temperature coefficient		125	<200	<200	<200	nA/°C	DIBI
* power supply rejection ratio		50	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
* supply current	no load	18	<22	<22	<22	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		400	>100	>200	>400	kΩ	RIN
capacitance		1.3	<2.5	<2.5	<2.5	pF	CIN
output impedance	at 100MHz	5,37	—	—	—	Ω,nH	ZO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO

Absolute Maximum Ratings

Input and Common Mode Voltage Limits



supply voltage V_{cc}	±20V
output current	±100mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
	A8/AK: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

***note 1:** Parameters preceded by an * are the final electrical test parameters and are 100% tested. A8 and AK units are tested at −55°C, +25°C, and +125°C. AI units are tested only at +25°C although performance at −25°C and +85°C is guaranteed to be better than or equal to the performance of A8 units over their temperature range.

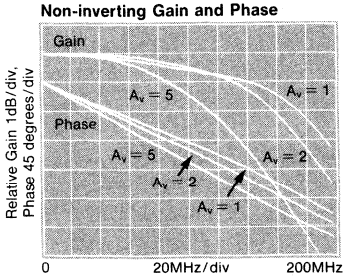
note 2: The output amplitude used in testing is 0.63V_{pp}. Performance is guaranteed for conditions listed.

note 3: In the non-inverting configuration, care should be taken when choosing R_i, the input impedance setting resistor; bias currents of typically 5μA but as high as 24μA can create an input signal large enough to cause overload. It is therefore recommended that $R_i < (V_{cc}/A_v)/24\mu A$.

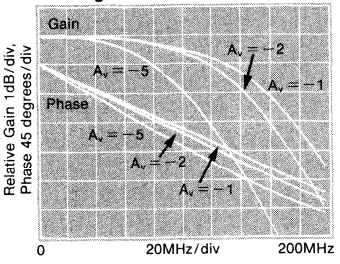
note 4: These ratings protect against damage to the input stage caused by saturation of either the input or output stages at lower supply voltages, and against exceeding transistor collector-emitter breakdown ratings at high supply voltages. V_{out}(max) is calculated by assuming no output saturation. Saturation is allowed to occur up to this calculated level of V_{out}. V_{cm} is defined as the voltage at the non-inverting input, pin 6.

Typical Performance Characteristics ($T_A = 25°C$, $A_v = +2$, $V_{cc} = \pm 15V$, $R_L = 100\Omega$, $R_f = 250\Omega$)

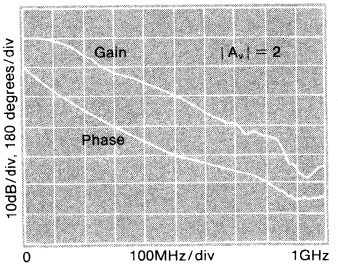
Non-inverting Gain and Phase



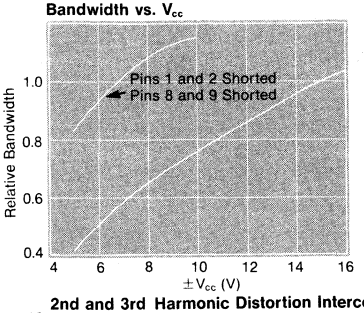
Inverting Gain and Phase



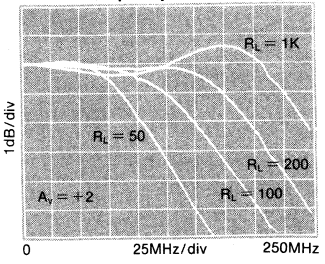
Broadband Gain and Phase



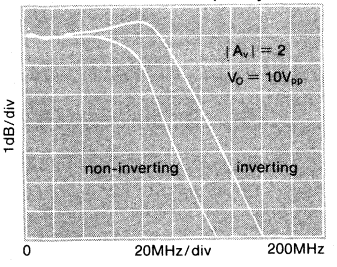
Bandwidth vs. V_{cc}



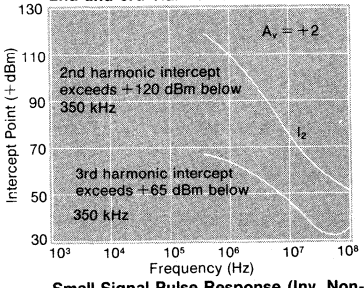
Gain vs. Frequency for Various R_Ls



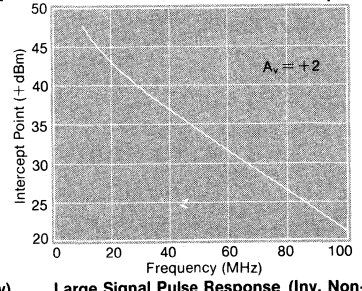
Full Power Gain vs. Frequency



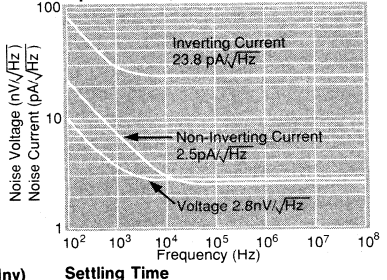
2nd and 3rd Harmonic Distortion Intercept



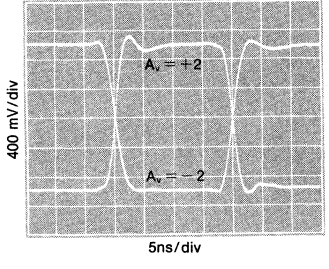
2-Tone 3rd Order Intermod. Intercept



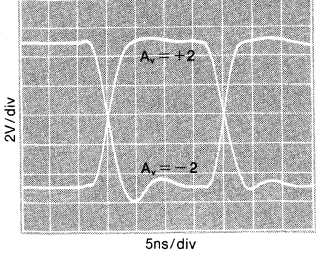
Equivalent Input Noise



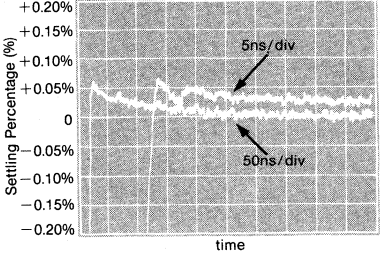
Small Signal Pulse Response (Inv, Non-Inv)



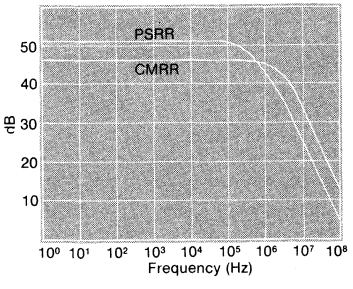
Large Signal Pulse Response (Inv, Non-Inv)



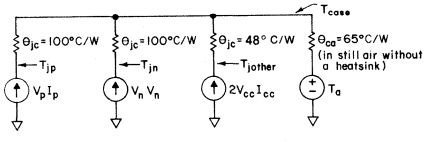
Settling Time



CMRR and PSRR



Thermal Model



$P_{circuit} = I_{cc}[(+V_{cc}) - (-V_{cc})]$ where $I_{cc} = 16mA$ at $\pm 15V$

$P_{XXX} = [(\pm V_{cc}) - V_{out} - (I_{col})(R_{col} + 4)](I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 4mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\,(pnp)} = P_{pnp}(100 + \theta_{ca}) + (P_{cir} + P_{npn})\theta_{ca} + T_a$, similar for $T_{j\,(npn)}$.

$T_{j\,(cir)} = P_{cir}(48 + \theta_{ca}) + (P_{pnp} + P_{npn})\theta_{ca} + T_a$.

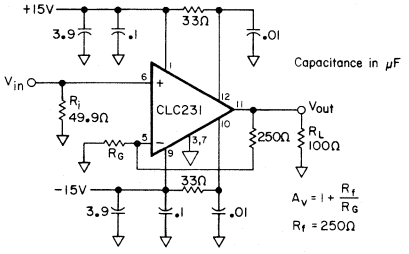


Figure 1: suggested non-inverting gain circuit

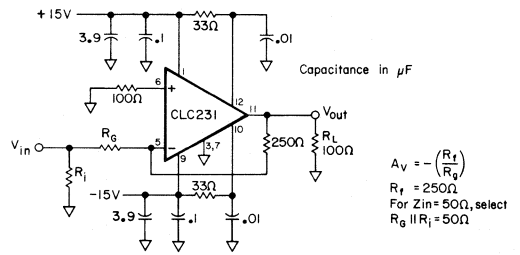


Figure 2: suggested inverting gain circuit

Test fixture schematics are available upon request.

CLC231 Operation

The CLC231 Buff-Amp™ is based on Comlinear's proprietary op amp topology, a design that uses current feedback instead of the usual voltage feedback. A complete discussion of current feedback is given in application note AN300-1.

The use of the CLC231 is basically the same as that of the conventional op amp (see the gain equations above). Since the device is designed specifically for low gain applications, the best performance is obtained when the circuit is used at gains between ±1 and ±5. Additionally, performance is optimum when a 250Ω feedback resistor is used.

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{cc} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available from Comlinear at minimal cost.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

Low V_{cc} Operation: Supply Current Adjustment

The CLC231 is designed to operate on supplies as low as ±5V. In order to improve full bandwidth at reduced supply voltages, the supply current (I_{cc}) must be increased. The plot of Bandwidth vs V_{cc} shows the effect of shorting pins 1 and 2 and pins 8 and 9; this will increase both bandwidth and supply current. Care should be taken to not exceed the maximum junction temperatures; for this reason this technique should not be used with supplies exceeding ±10V. For intermediate values of V_{cc}, external resistors between pins 1 and 2 and pins 8 and 9 can be used.

Offset Voltage Adjustment

If trimming of the input offset voltage ($V_{os} = V_{ni} - V_{in}$) is desired, a resistor value of 10kΩ to 1MΩ placed between pins 8 and 9 will cause V_{os} to become more negative by 8mV to 0.2mV respectively. Similarly, a resistor placed between pins 1 and 2 will cause V_{os} to become more positive.

Distortion and Noise

The graphs of intercept point, I_2 and I_3, versus frequency on the preceding page make it easy to predict the distortion at any frequency given the output voltage of the CLC231. First, convert the output voltage (V_O) to $V_{RMS} = (V_{pp}/2\sqrt{2})$ and then to $P = [(10\log_{10}(20V_{RMS}^2)]$ to get the power output in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below P, as will the two-tone third order intermodulation products. These approximations are useful for P<−1dB compression levels.

Approximate noise figure can be determined for the CLC231 using the equivalent input noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{\frac{i_n^2 R_F^2}{A_v^2} + v_n^2}{4kTR_s\Delta f}\right]$$

Where v_n is the rms noise voltage and i_n is the rms noise current. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly qualified applications engineers to provide technical and design assistance.

Comlinear Corporation

Low Distortion Wideband Op Amp

CLC232

APPLICATIONS:
- flash A/D drivers
- DAC current-to-voltage conversion
- wide dynamic range IF amps
- VCO drivers
- DDS postamps
- radar/communication receivers
- precision line drivers

FEATURES (typical):
- −69dBc 2nd and 3rd harmonics at 20MHz
- −3dB bandwidth of 270MHz
- 0.05% settling in 15ns
- 3000V/μs slew rate
- 1mV input offset voltage, 10μV/°C drift
- ±10V, 100mA max output

DESCRIPTION:

The CLC232 is a wideband low distortion operational amplifier designed specifically for high speed, low gain applications requiring wide dynamic range. Utilizing Comlinear's patented current feedback architecture, the CLC232 offers high speed performance while maintaining DC precision.

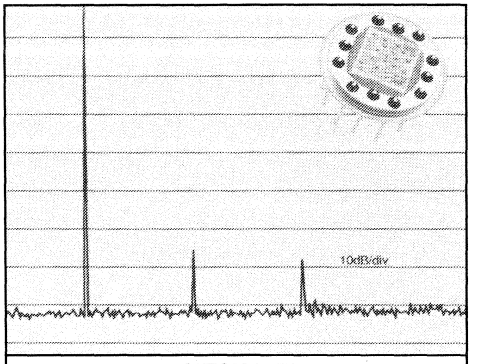
The CLC232 offers precise gains from ±1 to ±5 with a true 0.1% linearity and provides stable, oscillation-free operation across the entire gain range without external compensation. The CLC232, a pin compatible enhanced version of the CLC231, reduces 2nd and 3rd harmonic distortion to an extremely low −69dBc at 20MHz ($2V_{pp}$, $R_L = 100\Omega$). Additional features provided by the CLC232 include a small signal bandwidth of 270MHz, a large signal bandwidth of 95MHz and a 3000V/μs slew rate. The input offset voltage is typically 1mV with an input offset drift of 10μV/°C.

The CLC232 combines these high performance features with its 0.05% settling time of 15ns and its 100mA drive capability to provide high speed, high resolution A/D and D/A converter systems with an attractive solution for driving and buffering. Wide dynamic range systems such as radar and communication receivers requiring low harmonic distortion and low noise will find the CLC232 to be an excellent choice. As a linedriver, the CLC232 set at a gain of 2 cancels matched line losses.

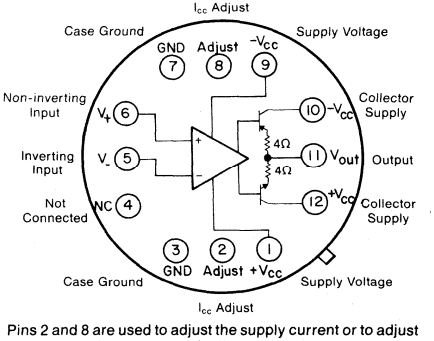
The CLC232 is constructed using thin-film resistor/bipolar transistor technology and is available in three versions. The CLC232AI is specified over a temperature range of –25°C to +85°C. The CLC232AK, which features burn-in and tested hermeticity, is specified and tested over a temperature range of –55°C to +125°C. The CLC232A8C is specified and tested over a temperature range of –55°C to +125°C and is fully compliant with MIL-STD-883 for high-reliability applications. All three versions are packaged in metal 12-pin TO-8 packages. The DESC SMD number is 5962-91665.

Typical Performance

	gain setting						
parameter	1	2	5	−1	−2	−5	units
−3dB bandwidth	430	270	135	220	175	110	MHz
rise time (2V)	1.8	2.0	2.5	2.0	2.2	2.9	ns
slew rate	2.5	3	3	3	3	3	V/ns
settling time (to .1%)	12	12	12	12	12	15	ns

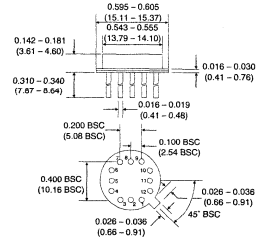


BOTTOM VIEW



Pins 2 and 8 are used to adjust the supply current or to adjust the offset voltage (see text). These pins are normally left unconnected.

Package Dimensions



Electrical Characteristics ($R_L = 100\Omega$; $R_f = 250\Omega$; $V_{cc} = \pm 15V$; $A_v = +2$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	CLC232 A8/AK	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC232 AI	+25°C	−25°C	+25°C	+ 85°C		
FREQUENCY DOMAIN RESPONSE, note 2							
*−3dB bandwidth	$V_{out} \leq 0.63V_{pp}$	270	>200	>200	>200	MHz	SSBW1
	$V_{out} \leq 2V_{pp}$	165	>145	>145	>120	MHz	SSBW2
	$V_{out} \leq 10V_{pp}$	95	>80	>80	>60	MHz	LSBW
gain flatness	$V_{out} \leq 0.63V_{pp}$						
* peaking	0.1 to 50MHz	0.1	<0.6	<0.3	<0.6	dB	GFPL
* peaking	>50MHz	0.1	<1.5	<0.3	<0.8	dB	GFPH
* rolloff	at 100MHz	0.4	<0.6	<0.6	<1.0	dB	GFR
group delay	to 100MHz	3.5 ± .5	—	—	—	ns	GD
linear phase deviation	to 100MHz	0.5	<2.0	<2.0	<2.0	°	LPD
reverse isolation	to 100MHz						
non-inverting		53	>43	>43	>43	dB	RINI
inverting		36	>26	>26	>26	dB	RIIN
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.0	<2.4	<2.3	<2.7	ns	TRS
	10V step	5.0	<7.0	<6.5	<6.5	ns	TRL
settling time to 0.05%	5V step	15	—	—	—	ns	TS
to 0.1%	2.5V step	12	<22	<17	<22	ns	TSP
overshoot	5V step	5	<15	<10	<15	%	OS
slew rate		3000	>2500	>2500	>1800	V/μs	SR
overload recovery	<1% error						
<50ns pulse, 200% overdrive		120	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE, note 3							
*2nd harmonic distortion	$2V_{pp}$, 20MHz	−69	<−64	<−64	<−56	dBc	HD2
*3rd harmonic distortion	$2V_{pp}$, 20MHz	−69	<−64	<−64	<−64	dBc	HD3
equivalent noise input							
voltage	>100kHz	2.8	<3.2	<3.2	<3.5	$nV/\sqrt{Hz}$	VN
inverting current	>100kHz	20	<23	<23	<25	$pA/\sqrt{Hz}$	ICN
non-inverting current	>100kHz	2.3	<2.6	<2.6	<2.9	$pA/\sqrt{Hz}$	NCN
noise floor	>100kHz	−155	<−154	<−154	<−153	dBm_{1Hz}	SNF
integrated noise	1kHz to 200MHz	57	<64	<64	<72	μV	INV
integrated noise	5MHz to 200MHz	57	<64	<64	<72	μV	INV
STATIC DC PERFORMANCE							
*input offset voltage		1	<4.0	<2.0	<4.5	mV	VIO
temperature coefficient		10	<25	<25	<25	μV/°C	DVIO
*input bias current	non-inverting	5	<29	<21	<31	μA	IBN
temperature coefficient		50	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	10	<31	<15	<35	μA	IBI
temperature coefficient		125	<200	<200	<200	nA/°C	DIBI
*power supply rejection ratio		50	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
*supply current	no load	25	<27	<27	<29	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		400	>100	>200	>400	kΩ	RIN
non-inverting input capacitance		1.3	<2.5	<2.5	<2.5	pF	CIN
output impedance	at 100MHz	5, 37	—	—	—	Ω, nH	ZO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO

Absolute Maximum Ratings

V_{CC}		±20V
I_{out}		±100mA
V_{CM}, V_{out}	$\|V_{CC}\| > 15V$	$\pm(30 - \|V_{CC}\|)V$
	$\|V_{CC}\| \leq 15V$	$\pm\|V_{CC}\|V$
differential input voltage		±3V
junction temperature		+175°C
operating temperature range	AI:	−25°C to +85°C
	A8/AK:	−55°C to +125°C
Storage Temperature Range		−65°C to + 150°C
Lead Temperature (soldering 10s)		+300°C

Recommended Operating Conditions

V_{CC}	±5V to ±15V
I_{out}	±75ma
V_{CM}	$\pm(\|V_{CC}\| - 5)V$
gain range	±1 to ±5

Notes:

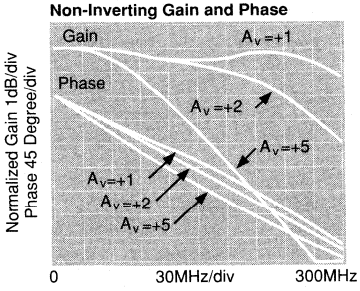
Note 1: Parameters preceded by an * are 100% tested. A8 and AK units are tested at −55°C, +25°C and +125°C. AI units are tested at +25°C, though performance at −25°C and +85°C is guaranteed as shown above.

Note 2: The output amplitude used in testing is $0.63V_{pp}$.Performance is guaranteed as listed above.

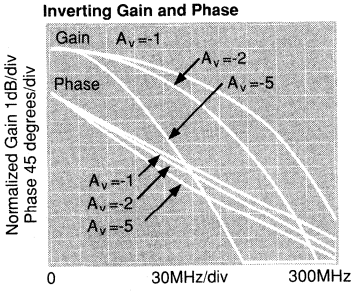
Note 3: In AI units, the noise and distortion specifications are guaranteed (but not tested) as shown above.

Typical Performance Characteristics (T_A=25°C, A_V=+2, V_{CC}=±15V, R_L=100Ω, R_f=250Ω)

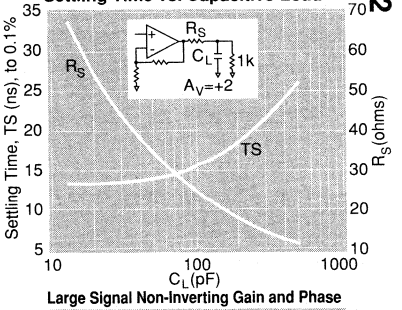
Non-Inverting Gain and Phase



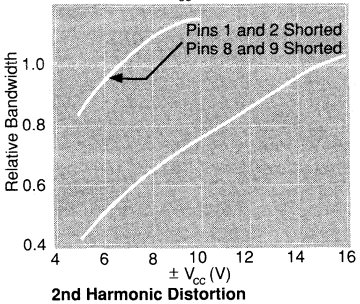
Inverting Gain and Phase



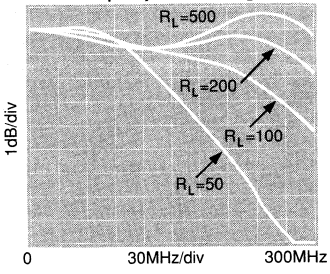
Settling Time vs. Capacitive Load



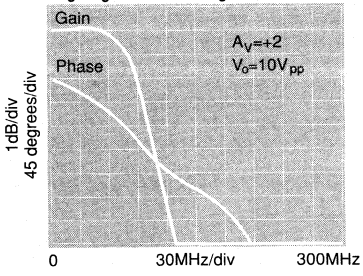
Bandwidth vs. V_{cc}



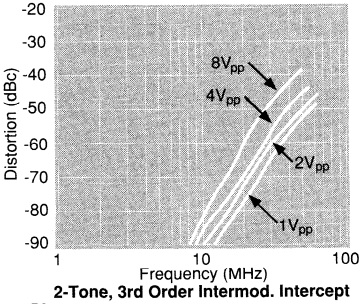
Gain vs. Frequency for Various R_L



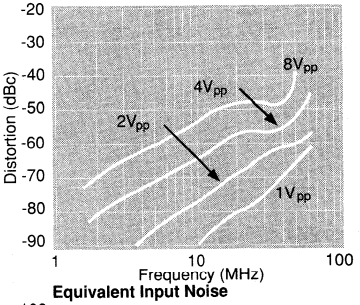
Large Signal Non-Inverting Gain and Phase



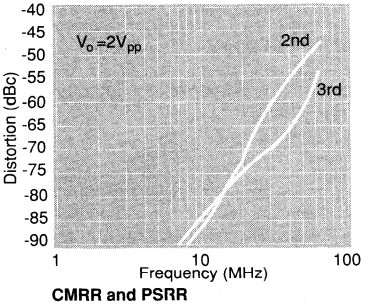
2nd Harmonic Distortion



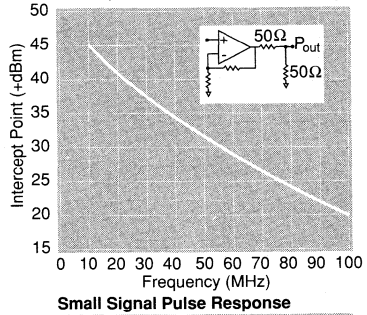
3rd Harmonic Distortion



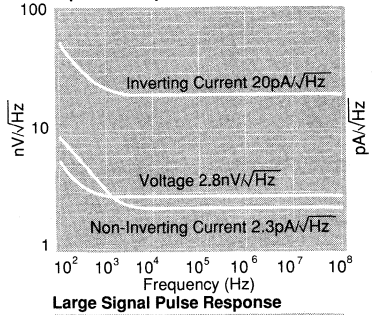
2nd and 3rd Harmonic Distortion: 200Ω Load



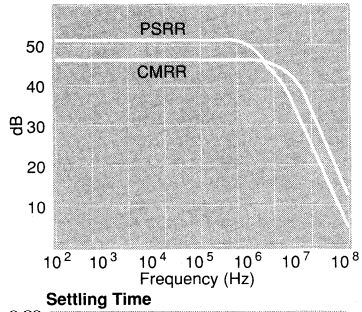
2-Tone, 3rd Order Intermod. Intercept



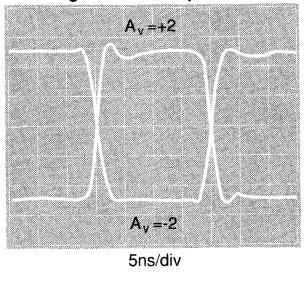
Equivalent Input Noise



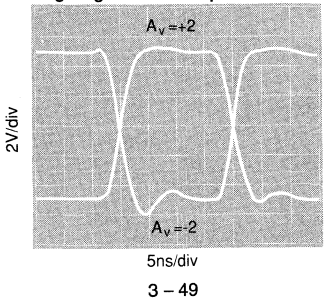
CMRR and PSRR



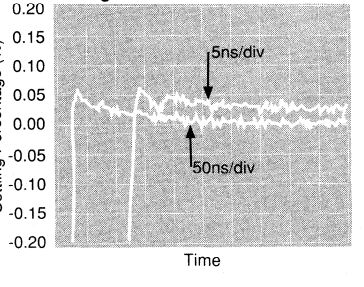
Small Signal Pulse Response



Large Signal Pulse Response



Settling Time



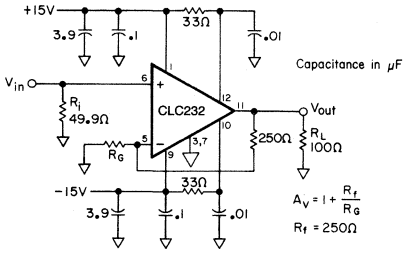


Figure 1: suggested non-inverting gain circuit

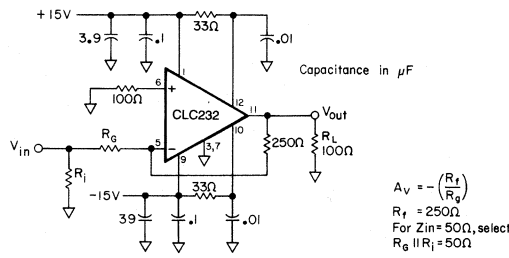


Figure 2: suggested inverting gain circuit

Test fixture schematics are available upon request.

CLC232 Operation

The CLC232 is based on Comlinear's proprietary op amp topology, a design that uses current feedback instead of the usual voltage feedback. A complete discussion of current feedback is given in application note AN300-1.

The use of the CLC232 is basically the same as that of the conventional op amp (see the gain equations above). Since the device is designed specifically for low gain applications, the best performance is obtained when the circuit is used at gains between ±1 and ±5. Additionally, performance is optimum when a 250Ω feedback resistor is used.

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{cc} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in Figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available from Comlinear at minimal cost.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

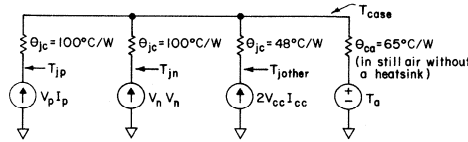
Low V_{cc} Operation: Supply Current Adjustment

The CLC232 is designed to operate on supplies as low as ±5V. In order to improve full bandwidth at reduced supply voltages, the supply current (I_{cc}) must be increased. The plot of Bandwidth vs V_{cc} shows the effect of shorting pins 1 and 2 and pins 8 and 9; this will increase both bandwidth and supply current. Care should be taken to not exceed the maximum junction temperatures; for this reason this technique should not be used with supplies exceeding ±10V. For intermediate values of V_{cc}, external resistors between pins 1 and 2 and pins 8 and 9 can be used.

Offset Voltage Adjustment

If trimming of the input offset voltage ($V_{os} = V_{ni} - V_{in}$) is desired, a resistor value of 10kΩ to 1MΩ placed between pins 8 and 9 will cause V_{os} to become more negative by 8mV to 0.2mV respectively. Similarly, a resistor placed between pins 1 and 2 will cause V_{os} to become more positive.

Thermal Model



$P_{circuit} = I_{cc}[(+V_{cc}) - (-V_{cc})]$ where I_{cc} = 14mA at ±15V

$P_{xxx} = [(\pm V_{cc}) - V_{out} - (I_{col})\ (R_{col} + 4)]\ (I_{col})$ (%duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 12mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\ (pnp)} = P_{pnp}\ (100 + \theta_{ca}) + (P_{cir} + P_{npn})\ \theta_{ca} + T_a$, similar for $T_{j\ (npn)}$.

$T_{j\ (cir)} = P_{cir}\ (48 + \theta_{ca}) + (P_{pnp} + P_{npn})\ \theta_{ca} + T_a$.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly qualified applications engineers to provide technical and design assistance.

Comlinear Corporation

Wideband, High Speed Operational Amplifiers

CLC300

APPLICATIONS:

- digital communications
- baseband and video communications
- instrument input/output amplifiers
- fast A to D, D to A conversion
- graphic CRT video drive amp
- coaxial cable line driver

FEATURES:

- −3dB bandwidth of 85MHz
- new design topology eliminates gain-bandwidth trade-off
- 3000V/μsec slew rate
- 4ns rise and fall time
- 100mA output current
- low distortion, linear phase

DESCRIPTION:

The CLC300 operational amplifier is a unique, proprietary Comlinear design providing a **DC-85MHz –3dB bandwidth that is virtually independent of gain setting.** Rise and fall times of 4nsec and drive capability of $22V_{pp}$ and 100mA add to the CLC300's impressive specifications.

Ease-of-use is a design goal at Comlinear, and the CLC300 is a success in this area as well. Using the CLC300 is as easy as adding power supplies and a gain-setting resistor. And unlike conventional op amp designs in which optimum gain-bandwidth product occurs at a high gain, minimum settling time at a gain of −1, maximum slew rate at a gain of +1, et cetera, the CLC300 offers consistent performance at gain settings from 1 to 40 inverting or non-inverting. As a result, designing with the CLC300 is greatly simplified. And since **no external compensation is necessary,** "tweeks" on the production line have been eliminated, making the CLC300 an efficient component for use in production situations.

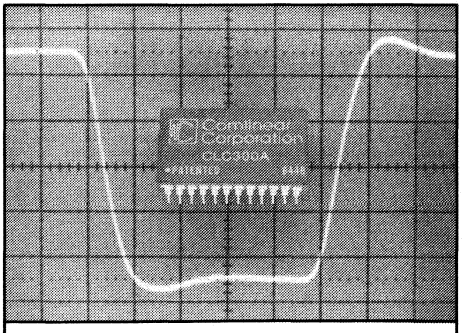
Flat gain and phase response from DC to 45MHz and superior rise and fall times make the CLC300 an ideal amplifier for a broad range of pulse, analog, and digital applications. A **45MHz full power bandwidth** ($20V_{pp}$ into 100Ω) and 3000V/μsec slew rate eliminate the need for power buffers in many applications such as driving "flash" A to D converters or line-driving. For applications requiring lower power consumption, the CLC300 can operate on supplies as low as 5V. Fast overload recovery (20nsec) helps prevent loss of data in communications applications and flat phase response reduces distortion, even when data must be sent over extended lengths of line.

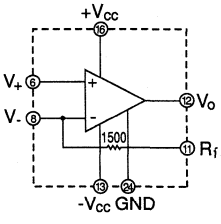
The CLC300A is packaged in a 24-pin ceramic DIP and is specified over a temperature range of –25°C to +85°C. The CLC300B has been discontinued and is no longer in production.

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

(continued on last page)

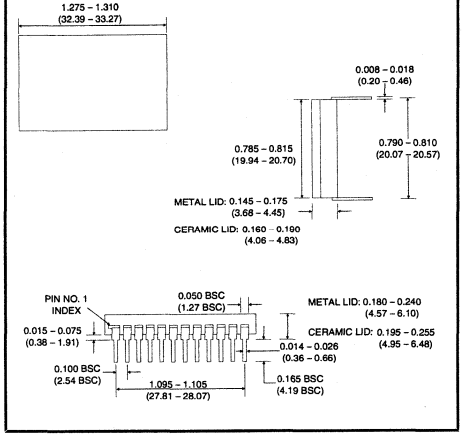




CLC300 Equivalent Circuit Diagram

Pin 11 provides access to a 1500Ω feedback resistor which can be connected to the output or left open if an external feedback resistor is desired. All undesignated pins are internally unconnected.

Package Dimensions



Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics (25°C, R_L=100Ω, R_f = 1500Ω, V_{cc} = ±15V)

magnitude of gain [$\lvert V_{out}/V_{in} \rvert$]	4*	20		40	
Parameter and Conditions	typ	min[2]	typ	max[2]	typ	units
FREQUENCY DOMAIN RESPONSE						
• −3dB bandwidth, V_{out} <4V_{pp}	105	75	85		70	MHz
V_{out} = 20V_{pp}	45		45		45	MHz
• gain flatness, 100KHz to 20MHz	±0.25		±0.08	±0.3	±0.25	dB
20MHz to 45MHz	±0.5		±0.25	±0.6	±1	dB
• phase shift	1		1.6		2	deg/MHz
• deviation from linear phase, DC to 45MHz	2		3		5	degree
• reverse isolation	60		70		70	dB
• distortion—refer to graphs						
TIME DOMAIN RESPONSE						
• rise and fall time, 5V output step	3		4		5	ns
20V output step	7		7		7	ns
• settling time, 10V output step, to .8%	20		20		25	ns
• overshoot (input rise time ≤1ns), 5V output step	5		5		5	%
• slew rate	3		3		3	V/ns
• overload recovery (<50ns pulse width, 200% overdrive)	20		20		20	ns

GENERAL INFORMATION	min[2]	typ	max[2]	units
• input offset voltage (drift)		10(25)	32	mV(μV/°C)
• input bias current (drift), non-inverting input		10(20)	30	μA(nA/°C)
inverting input		30(50)	100	μA(nA/°C)
• equivalent input noise[1], integrated 5MHz to 100MHz (R_S = 50Ω, gain = 20)		22	56	μV
• second/third harmonic distortion (@ 20MHz, +10dBm)		48	38	−dBc
• input impedance, non-inverting input		100K/3		Ω/pF
• power supply rejection ratio (referred to input)	45	60		dB
• common mode rejection ratio (referred to input)		64		dB
• output drive voltage current		10, 100		V, mA
• supply current		24	33	mA

Absolute Maximum Ratings

- supply voltage (±V_{cc}) 16V (±5V min.)
- output current (I_O) 100mA
- input voltage (V_{imax}) ($\lvert V_{cc} \rvert$ −2.5)/A_v
- common mode input voltage ±½$\lvert V_{cc} \rvert$
- power dissipation, refer to graph
- junction temperature (T_J) 150°C
- operating temperature (T_A) −25 to +85°C
- storage temperature −55 to +150°C
- still air thermal resistance (θ_{ca}) 25°C/W

[1] For Noise Figure, refer to Distortion and Noise Section in text.
[2] All min/max parameters are tested 100% at +25°C, A_v = +20, R_L = 100Ω, and V_{cc} = ±15V.
*refer to Low Gain Operation section.

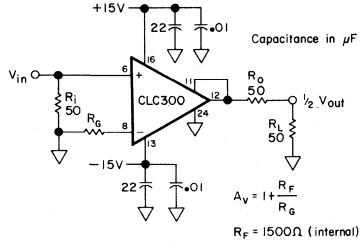


Figure 1: **recommended non-inverting gain circuit**

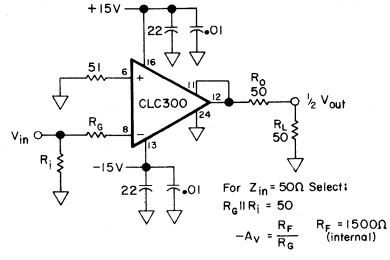
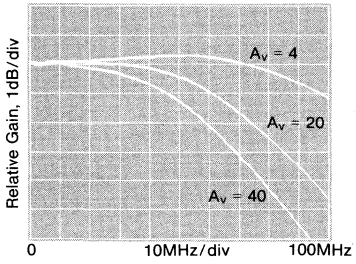


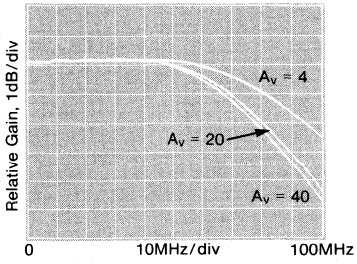
Figure 2: **recommended inverting gain circuit**

Typical Performance Characteristics (25 C, R_L=100Ω, R_f = 1500Ω, V_{cc} = ±15V)

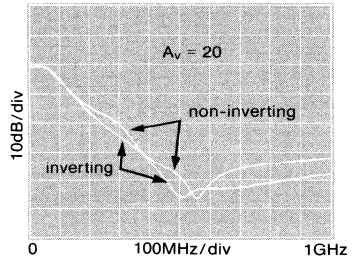
Non-Inverting Gain



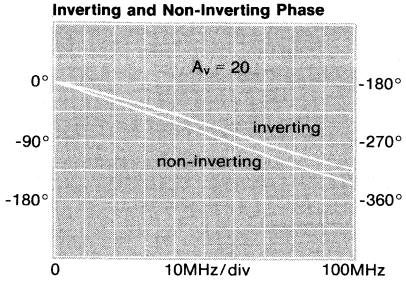
Inverting Gain



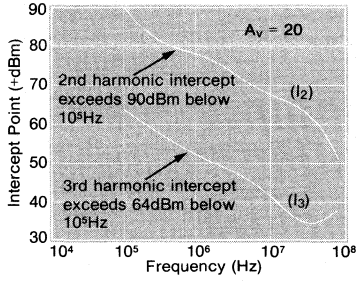
Broadband Inverting and Non-Inverting Gain



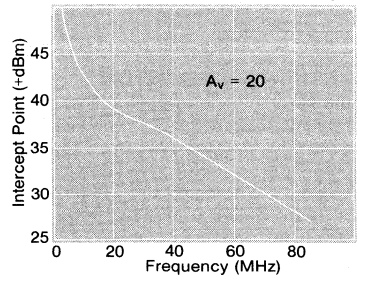
Inverting and Non-Inverting Phase



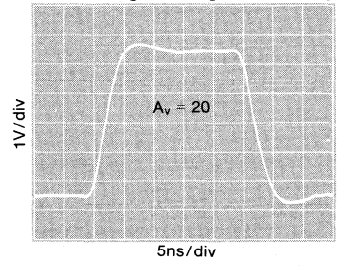
2nd and 3rd Harmonic Distortion Intercept



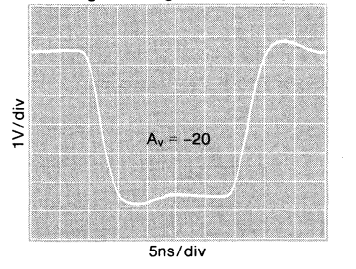
2-Tone 3rd Order Intermod. Intercept



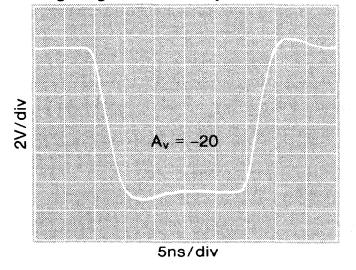
Non-Inverting Small Signal Pulse Response



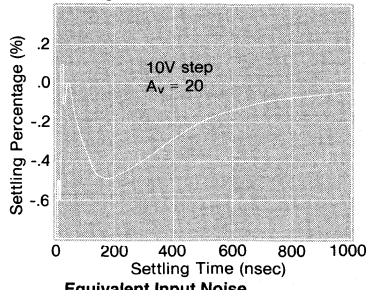
Inverting Small Signal Pulse Response



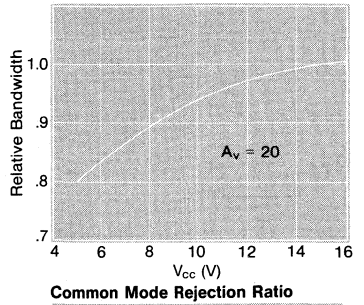
Large Signal Pulse Response



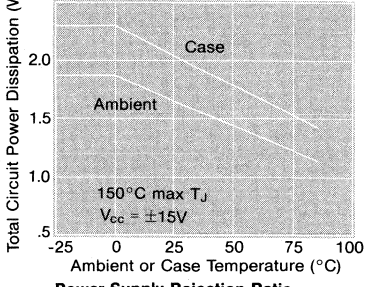
Settling Time



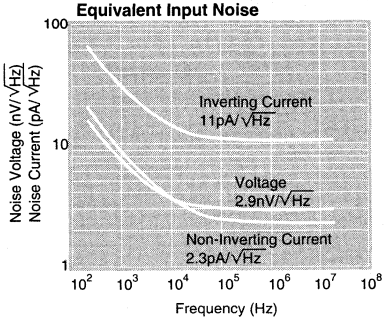
Relative Bandwidth vs. V_{cc}



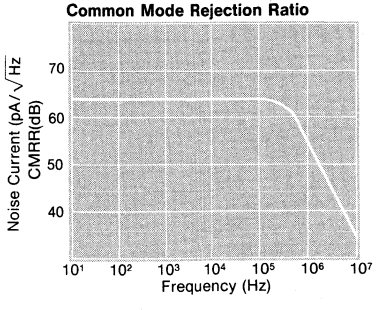
Power Dissipation Derating



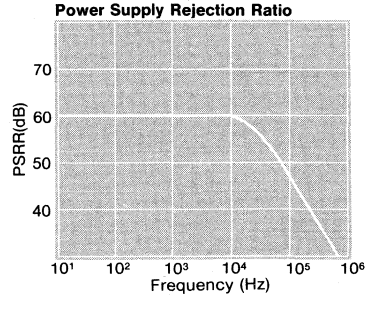
Equivalent Input Noise



Common Mode Rejection Ratio



Power Supply Rejection Ratio



Layout Considerations (continued)

During pc board layout keep all traces short and direct. The resistive bodies of R_F and R_G should be as close as possible to pin 8 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 8 and 6. In other areas, use as much ground plane as possible on one side of the pc board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF should be close to pins 13 and 16. Larger tantalum capacitors should also be placed within one inch of these pins. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches. Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase.

Controlling Bandwidth and Passband Response

As with any op amp, the ratio of the two feedback resistors R_F and R_G determines the gain of the CLC300. Unlike conventional op amps, however, the closed loop pole-zero response of the CLC300 is affected very little by the value of R_G. R_G scales the magnitude of the gain, but does not change the value of the feedback. This is possible due to a proprietary circuit topology. R_F does influence the feedback and so the CLC300 has been internally compensated for optimum performance with $R_F = 1500\Omega$, but any value of $R_F > 500\Omega$ may be used with a single capacitor placed between pins 8 and 12 for compensation. See Table1. As R_F decreases, C_c must increase to maintain flat gain. Large values of R_F and C_c can be used together or separately to reduce the bandwidth. This may be desirable for reducing the noise bandwidth in applications not requiring the full frequency response available.

Table1: Bandwidth versus R_F and C_c (A_V = +20)

R_F (KΩ)	C_c (pF)	$f_{\pm 0.3dB}$ (MHz)	$f_{-3.0dB}$ (MHz)
10.0	0	2	5
5.0	0	3	12
2.0	0	8	40
1.5	0	45	85
1.0	0.3	90	115
.75	1.1	95	130
0.50	1.9	110	135

Low Gain Operation

The small amount of stray capacitance present at the inverting input can cause peaking which increases with decreasing gain. The gain setting resistor R_G is effectively in parallel with this capacitance and so a frequency domain pole results. With small R_G (Gain > 8), this pole is at a high frequency and it affects the closed loop gain of the CLC300 only slightly. At lower values of gain, this pole becomes significant. For example, at a gain of +2, the gain may peak as much as 3dB at 75MHz, and have a bandwidth exceeding 150MHz. The same behavior does not exist for low inverting gains, however, since the inverting input is a virtual ground which maintains a constant voltage across the stray capacitance. Even at inverting gains $\ll 1$, the frequency response remains unchanged.

To avoid the peaking at low non-inverting gains, place a resistor R_p in series with the input signal path just ahead of pin 6, the non-inverting input. This forms a low pass filter with the capacitance at pin 6 which can be made to cancel the peaking due to the capacitance at pin 8, the inverting input. At a gain of +2, for example, choosing R_p such that the source impedance in parallel with R_i (see Figure 1), plus R_p equals175Ω will flatten the frequency response. For larger gains, R_p will decrease.

Settling Time, Offset, and Drift

After an output transition has occurred, the output settles very rapidly to final value and no change occurs for several microseconds. Thereafter, thermal gradients inside the CLC300 will cause the output to begin to drift. When this cannot be tolerated, or when the initial offset voltage and drift is unacceptable, the use of a composite amplifier is advised. This technique reduces the offset and drift to that of a monolithic, low frequency op amp, such as an LF356A. The composite amplifier technique is fully described in the CLC103 Data Sheet.

A simple offset adjustment can be implemented by connecting the wiper of a potentiometer, whose end terminals connect to $\pm$15V, through a 20K resistor to pin 8 of the CLC300. Variations of this technique are described in Application Note 200-1, Designer's Guide for 200 Series Op Amps.

Overload Protection

To avoid damage to the CLC300, care must be taken to insure that the input voltage does not exceed $(|V_{cc}| - 2.5)/A_V$. High speed, low capacitance diodes should be used to limit the maximum input voltage to safe levels if a potential for overload exists.

If in the non-inverting configuration the resistor R_i, which sets the input impedance, is large, the bias current at pin 6, which is typically a few μA but which may be as large as 18μA, can create a large enough input voltage to exceed the overload condition. It is therefore recommended that $R_i < [(|V_{cc}| - 2.5)/A_V]/(18\mu A)$.

Distortion and Noise

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the CLC300. First, convert the output voltage (V_O) to $V_{RMS} = V_{pp}/2\sqrt{2}$ and then to $P = 10\log_{10}(20V_{RMS}^2)$ to get output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$ dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$ dB below P, as will the two tone third order intermodulation products. These approximations are useful for $P < -1$dB compression levels.

Approximate noise figure can be determined for the CLC300 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB:

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so Δf should equal one (1) and v_n and i_n should be read directly off of the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

Application Notes

For information on the use of the CLC300 in a wide variety of applications, refer to application note AN200-1.

Comlinear Corporation

Fast Settling, Wideband Low-Gain Monolithic Op Amps

CLC400

APPLICATIONS:

- fast, precision A/D conversion
- video distribution
- line drivers
- D/A current-to-voltage conversion
- photodiode, CCD preamps
- IF processors
- high-speed communications

FEATURES:

- −3dB bandwidth of 200MHz
- 0.05% settling in 12ns
- low power, 150mW
- low distortion, −60dBc at 20MHz
- stable without compensation
- overload and short circuit protected
- ±1 to ±8 closed-loop gain range

DESCRIPTION:

The CLC400 is a high-speed, fast-settling operational amplifier designed for low-gain applications. Constructed using a unique, proprietary design and an advanced complementary bipolar process, the CLC400 offers performance far beyond that normally offered by ordinary monolithic op amps. In addition, unlike many other high-speed op amps the CLC400 offers both high performance and stability without the need for compensation circuitry—even at a gain of +1.

The fast 12ns settling to 0.05% and its ability to drive capacitive loads makes the CLC400 an ideal flash A/D driver. The wide bandwidth of 200MHz and the very linear phase ensure unsurpassed signal fidelity. Systems employing digital to analog converters also benefit from the use of the CLC400—especially if linearity and drive levels are important to system performance.

The CLC400 provides a simple, high-performance solution for video distribution and line driving applications. The 50mA output current and guaranteed specifications for 100 ohm loads provide ample drive capability and assured performance.

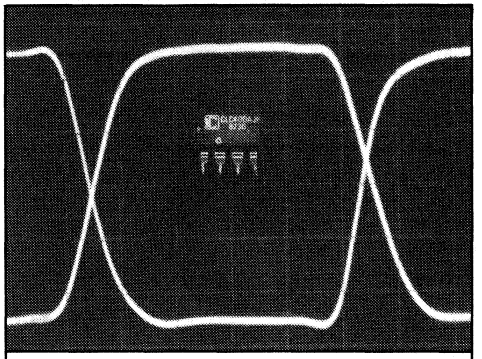
The CLC400 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC400AJP	– 40°C to + 85°C	8-pin plastic DIP
CLC400AJE	– 40°C to + 85°C	8-pin plastic SOIC
CLC400AIB	– 40°C to + 85°C	8-pin hermetic CERDIP
CLC400A8B	– 55°C to + 125°C	8-pin hermetic CERDIP, MIL-STD-883, Level B
CLC400ALC	– 55°C to + 125°C	dice
CLC400AMC	– 55°C to + 125°C	dice qualified to Method 5008, MIL-STD-883, Level B

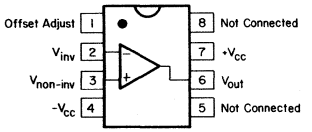
Operation

The CLC400 is based on Comlinear's proprietary op amp topology that uses current feedback instead of the usual voltage feedback. This unique design has many advantages over conventional designs (such as settling time that is relatively independent of gain), yet it is used in basically the same way (see the gain equations in Figures 1 and 2, page 4). However, an understanding of the topology will aid in achieving the best performance. The following discussion will proceed for the non-inverting gain configuration with the inverting mode analysis being very similar.

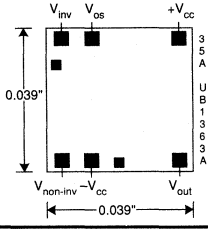
Contact factory for other packages. DESC SMD number, 5962-89970.



PINOUT



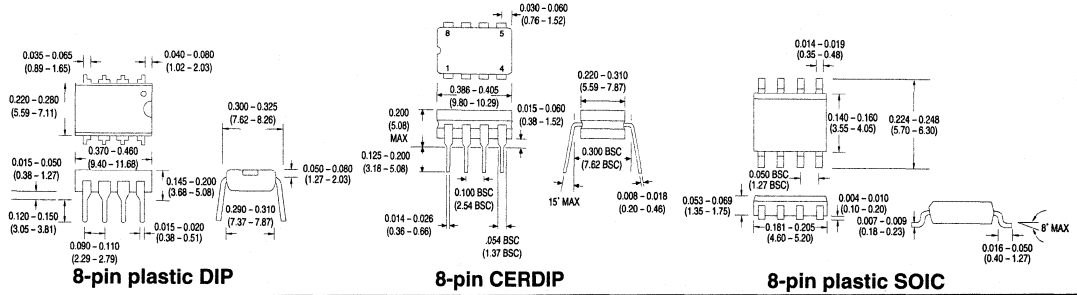
DIP and SO-8 Versions



Chip Topography

Height is 0.014 inches.
NOTE: Backside connected to $-V_{cc}$. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



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January 1993

DS400.05

Electrical Characteristics (A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC400AJ/AI	+25°C	−40°C	+25°C	+85°C		
Ambient Temperature	CLC400A8/AM/AL	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
†−3dB bandwidth	V_{out}<0.5V_{pp}	200	150	150	120	MHz	SSBW
	V_{out}<5V_{pp}, A_v = + 5	50	35	35	35	MHz	LSBW
gain flatness[1]	V_{out}<0.5$_{pp}$						
† peaking	<40MHz	0	0.4	0.3	0.4	dB	GFPL
† peaking	>40MHz	0	0.7	0.5	0.7	dB	GFPH
† rolloff	<75MHz	0.6	1.0	1.0	1.3	dB	GFR
linear phase deviation	to 75MHz	0.2	1.0	1.0	1.2	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	1.6	2.4	2.4	2.4	ns	TRS
	5V step	6.5	10	10	10	ns	TRL
settling time to ±0.1%	2V step	10	13	13	13	ns	TSP
±0.05%	2V step	12	15	15	15	ns	TS
overshoot	0.5V step	0	15	10	10	%	OS
slew rate A_v = +2		700	430	430	430	V/μs	SR
A_v = −2		1600	—	—	—	V/μs	SR1
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	2V_{pp}, 20MHz	−60	−40	−45	−45	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 20MHz	−60	−50	−50	−50	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−157	−154	−154	−153	dBm(1Hz)	SNF
integrated noise	1MHz to 200MHz	40	57	57	63	μV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		2	±8.2	±5.0	±9.0	mV	VIO
average temperature coefficient		20	±40	—	±40	μV/°C	DVIO
*input bias current	non-inverting	10	±36	±20	±20	μA	IBN
average temperature coefficient		100	±200	—	±100	nA/°C	DIBN
*input bias current	inverting	10	±36	±20	±30	μA	IBI
average temperature coefficient		50	±200	—	±100	nA/°C	DIBI
‡power supply rejection ratio		50	45	45	45	dB	PSRR
♠common mode rejection ratio		50	45	45	45	dB	CMRR
*supply current	no load	15	23	23	23	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	200	>50	>100	>100	kΩ	RIN
	capacitance	0.5	<2.0	<2.0	<2.0	pF	CIN
output impedance	at DC	0.1	<0.2	<0.2	<0.2	Ω	RO
output voltage range	no load	±3.5	>3.0	>3.2	>3.2	V	VO
common mode input range	for rated performance	±2.1	>1.2	>2.0	>2.0	V	CMIR
output current	−40°C to +85°C	±70	>35	>50	>50	mA	IO
	−55°C to +125°C	±70	>30	>50	>50	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	±V_{cc}
differential input voltage	10V
junction temperature	+ 175°C
operating temperature range	
AI/AJ:	− 40°C to + 85°C
A8/AM/AL:	− 55°C to + 125°C
storage temperature range	− 65°C to + 150°C
lead solder duration (+ 300°C)	10 sec

Miscellaneous Ratings

recommended gain range ±1 to ±8

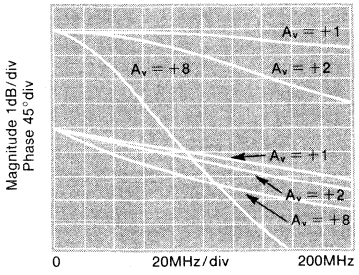
NOTES:

*	AI, AJ	100% tested at + 25°C, sample at + 85°C.
†	AJ	Sample tested at + 25°C.
†	AI	100% tested at + 25°C.
*	A8	100% tested at + 25°C, −55°C, + 125°C.
†	A8	100% tested at + 25°C, sample − 55°C, +125°C.
*	AL,AM	100% wafer probe tested at + 25°C to + 25°C min/max specifications.
♠	SMD	Sample tested at + 25°C, − 55°C, +125°C.

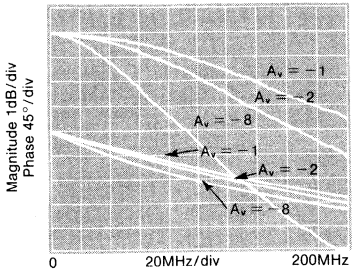
note 1: Gain flatness tests performed from 0.1MHz.

Typical Performance Characteristics ($T_A = 25°C$, $A_V = +2$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$)

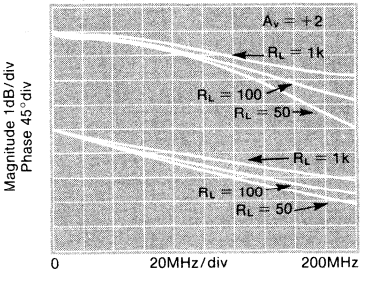
Non-Inverting Frequency Response



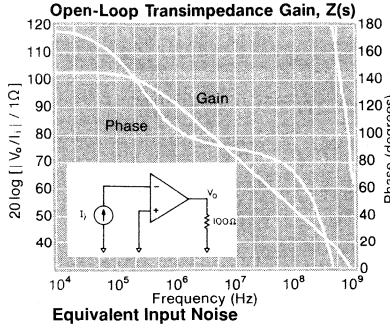
Inverting Frequency Response



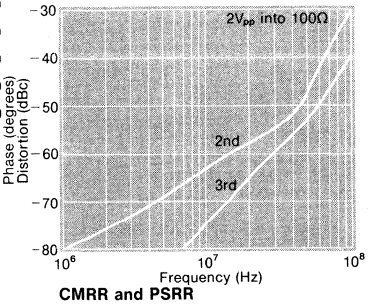
Frequency Response for Various R_Ls



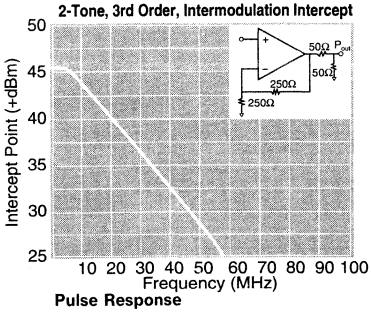
Open-Loop Transimpedance Gain, Z(s)



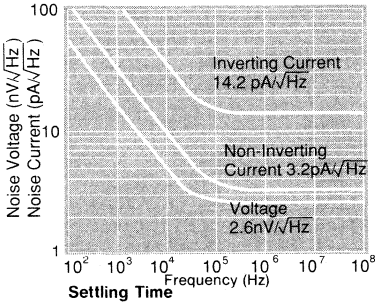
2nd and 3rd Harmonic Distortion



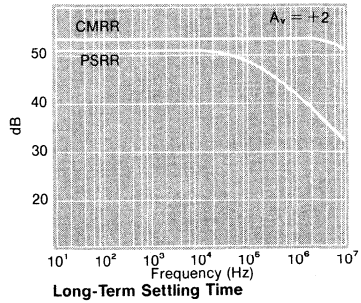
2-Tone, 3rd Order, Intermodulation Intercept



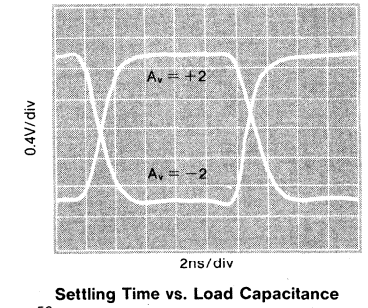
Equivalent Input Noise



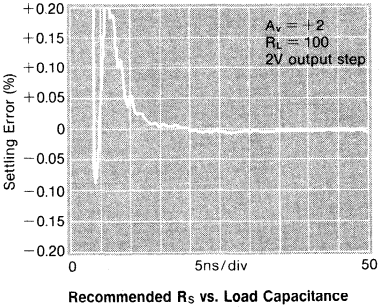
CMRR and PSRR



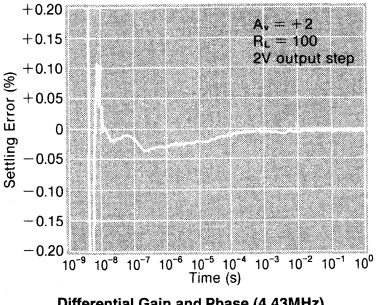
Pulse Response



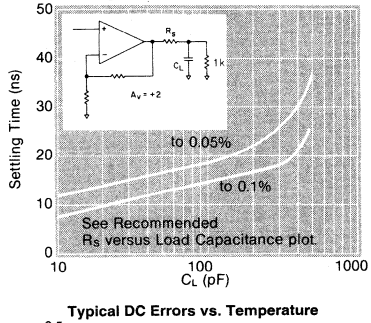
Settling Time



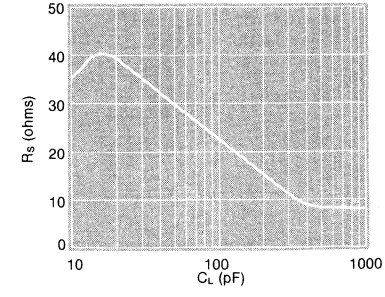
Long-Term Settling Time



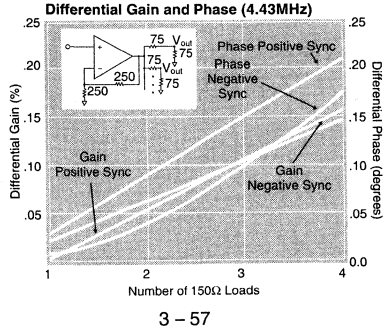
Settling Time vs. Load Capacitance



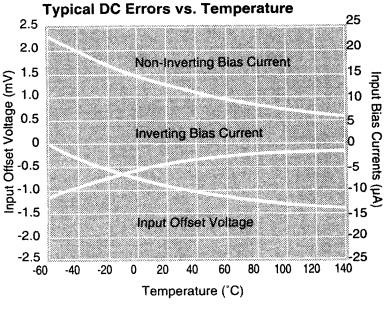
Recommended R_S vs. Load Capacitance



Differential Gain and Phase (4.43MHz)



Typical DC Errors vs. Temperature



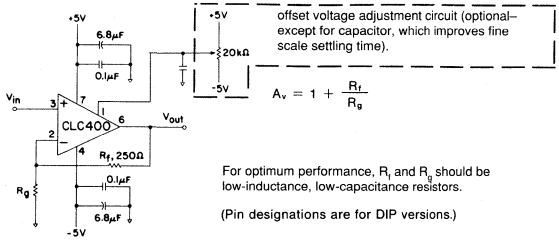


Figure 1: recommended non-inverting gain circuit

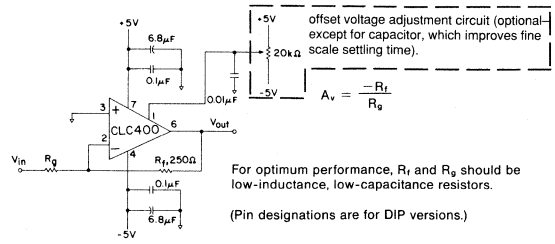


Figure 2: recommended inverting gain circuit

Understanding the Loop Gain

Referring to the equivalent circuit of Figure 3, any current flowing in the inverting input is amplified to a voltage at the output through the transimpedance gain shown on the plots on page 3. This Z(s) is analogous to the open-loop gain of a voltage feedback amplifier.

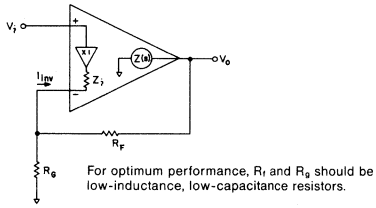


Figure 3: current feedback topology

Developing the non-inverting frequency response for the topology of Figure 3 yields:

$$\frac{V_o}{V_i} = \frac{1 + R_f/R_g}{1 - 1/LG} \qquad \text{Eq. (1)}$$

where LG is the loop gain defined by,

$$LG = \frac{Z(s)}{R_f} \times \frac{1}{1 + Z_i/(R_f \,||\, R_g)} \qquad \text{Eq. (2)}$$

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the LG expression, Equation 2. For an idealized treatment, set $Z_i = 0$ which results in a very simple $LG = Z(s)/R_f$ (Derivation of the transfer function for the case where $Z_i = 0$ is given in Application Note AN300-1). Using the Z(s) (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended $R_f = 250\Omega$, yields a large loop gain at DC. As a result, Equation 1 shows that the closed-loop gain at DC is very close to $(1 + R_f/R_g)$.

At higher frequencies, the roll-off of Z(s) determines the closed-loop frequency response which, ideally, is dependent only on R_f. **The specifications reported on the previous pages are therefore valid only for the specified $R_f = 250\Omega$.** Increasing R_f from 250Ω will decrease the loop gain and bandwidth, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing R_f will hold the frequency response constant while the closed-loop gain can be adjusted using R_g.

The CLC400 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC400, $Z_i = 50\Omega$ leading to a drop in loop gain and bandwidth at high gain settings, as given by Equation 2. The second term in Equation 2 accounts for the division in feedback current that occurs between Z_i and $R_f||R_g$ at the inverting node of the CLC400. This decrease in bandwidth can be circumvented as described in "Increasing Bandwidth at High Gains."

DC Accuracy and Noise

Since the two inputs for the CLC400 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In Equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin resistance.

$$\text{Output Offset } V_o = \pm IBN \times R_s (1 + R_f/R_g) \pm VIO\ (1 + R_f/R_g) \pm IBI \times R_f \qquad \text{Eq. (3)}$$

An important observation is that for fixed R_f, offsets as referred to the input improve as the gain is increased (divide all terms by $1 + R_f/R_g$). A similar result is obtained for noise where noise figure improves as gain increases.

Selecting Between the CLC400 or CLC401

The CLC400 is intended for gains of ±1 to ±8 while the CLC401 is designed for gains of ±7 to ±50. Optimum performance is achieved with a feedback resistor of 250Ω with the CLC400 and 1.5kΩ with the CLC401—this distinction may be important in transimpedance applications such as D/A buffering. Although the CLC400 can be used at higher gains, the CLC401 will provide a wider bandwidth because loop gain losses due to finite Z_i are lower with the larger CLC401 feedback resistor as explained above. On the other hand, the lower recommended feedback resistance of the CLC400 minimizes the output errors due to inverting input noise and bias currents.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting R_f and R_g to make up for the losses in loop gain that occur at these high gain settings due to current division at the inverting input. An approximate relationship may be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, $R_f = 250\Omega$ and $R_g = 250\Omega$). For the CLC400 this gives,

$$R_f = 350 - 50A_v \text{ and } R_g = \frac{350 - 50A_v}{A_v - 1} \qquad \text{Eq. (4)}$$

where A_v is the non-inverting gain. Note that with $A_v = +2$ we get the specified $R_f = 250\Omega$, while at higher gains, a lower value gives stable performance with improved bandwidth.

Capacitive Feedback

Capacitive feedback should not be used with the CLC400 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC400.

Offset Adjustment Pin

Pin 1 can be connected to a potentiometer as shown in Figure 1 and used to adjust the input offset of the CLC400. Full range adjustment of ±5V on pin 1 will yield a ±10mV input offset adjustment range. Pin 1 should always be bypassed to ground with a ceramic capacitor located close to the package for best settling performance.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part no. 730013 for through-hole and 730027 for SOIC) for the CLC400 are available.

Comlinear Corporation

Fast Settling, Wideband High-Gain Monolithic Op Amps

CLC401

APPLICATIONS:

- fast, precision A/D conversion
- photodiode, CCD preamps
- IF processors
- high-speed modems, radios
- line drivers
- DC-coupled log amplifiers
- high-speed communications

FEATURES

- –3dB bandwidth of 150MHz
- 0.1% settling in 10ns
- low power, 150mW
- overdrive and short circuit protected
- stable without compensation
- recommended gain range, ±7 to ±50

DESCRIPTION:

The CLC401 is a wideband, fast-settling op amp designed for applications requiring gains greater than ±7. Constructed using an advanced complementary bipolar process and a proprietary design, the CLC401 features dynamic performance far beyond that of typical high-speed monolithic op amps. For example, at a gain of +20, the –3dB bandwidth is 150MHz and the rise/fall time is only 2.5ns.

The wide bandwidth and linear phase (0.2° deviation from linear at 50MHz) and a very flat gain response makes the CLC401 ideal for many digital communication system applications. For example, demodulators need both DC coupling and high-frequency amplification – requirements that are ordinarily difficult to meet.

The very fast 10ns settling to 0.1% and the ability to drive capacitive loads lend themselves well to flash A/D applications. Systems employing D/A converters also benefit from the settling time and also by the fact that current-to-voltage transimpedance amplification is easily accomplished.

The CLC401 provides a quick, effective design solution. Its stable operation over the entire ±7 to ±50 gain range precludes the need for external compensation. And, unlike many other high-speed op amps, the CLC401's power dissipation of 150mW is compatible with designs which must limit total power dissipation or power supply requirements.

The CLC401 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

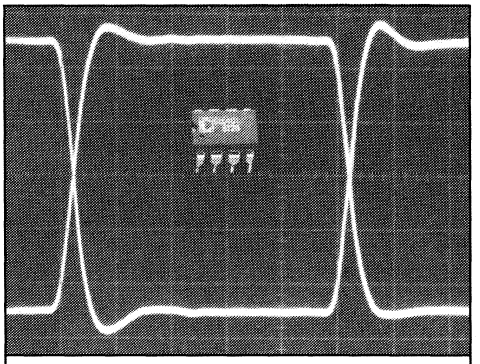
CLC401 AJP	–40°C to +85°C	8-pin plastic DIP
CLC401 AJE	–40°C to +85°C	8-pin plastic SOIC
CLC401 AIB	–40°C to +85°C	8-pin hermetic CERDIP
CLC401 A8B	–55°C to +125°C	8-pin hermetic CERDIP, MIL-STD-883, Level B
CLC401 ALC	–55°C to + 125°C	dice
CLC401 AMC	–55°C to + 125°C	dice-qualified to Method 5008, MIL-STD-883, Level B

Operation

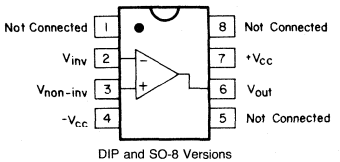
The CLC401 is based on Comlinear's proprietary op amp topology that uses current feedback instead of the usual voltage feedback. This unique design has many advantages over conventional designs (such as settling time that is relatively independent of gain), yet it is used in basically the same way (see the gain equations in Figures 1 and 2, page 4). How-

(Continued on page 4)

Contact factory for other packages. DESC SMD number, 5962-89973.

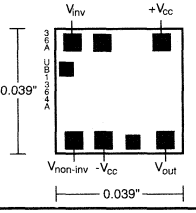


Pinout



DIP and SO-8 Versions

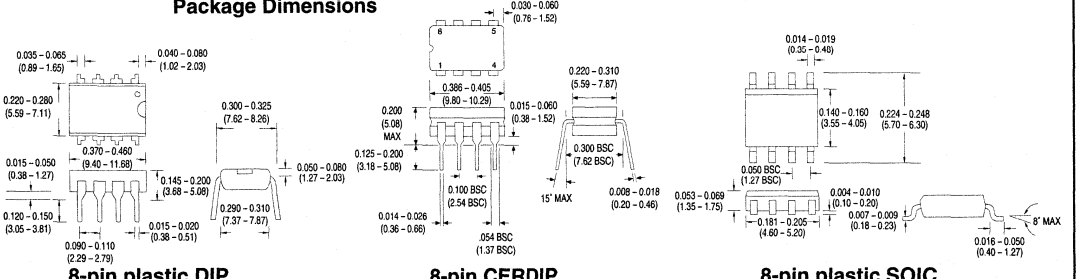
Chip Topography



Height is 0.014 inches.

NOTE: Backside connected to -Vcc. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



8-pin plastic DIP **8-pin CERDIP** **8-pin plastic SOIC**

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics (A_V = +20, V_{CC} = ±5V, R_L = 100Ω, R_f = 1.5kΩ)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC401AJ/AI	+25°C	−40°C	+25°C	+85°C		
Ambient Temperature	CLC401A8/AM/AL	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
†−3dB bandwidth	V_{out}<2V_{pp}	150	>100	>100	>70	MHz	SSBW
	V_{out}<5V_{pp}	100	>65	>65	>55	MHz	LSBW
gain flatness[2]	V_{out}<2V_{pp}						
† peaking	<25MHz	0	<0.1	<0.1	<0.1	dB	GFPL
† peaking	>25MHz	0	<0.2	<0.2	<0.2	dB	GFPH
† rolloff	<50MHz	0.2	<1.0	<1.0	<1.3	dB	GFR
linear phase deviation	DC to 50MHz	0.2	<1.0	<1.0	<1.5	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.5	<3.5	<3.5	<5.0	ns	TRS
	5V step	5	<7.0	<7.0	<8.0	ns	TRL
settling time to ±0.1%	2V step	10	<15	<15	<15	ns	TS
overshoot	2V step	0	<10	<10	<10	%	OS
slew rate		1200	>800	>800	>700	V/μs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	2V_{pp}, 20MHz	−45	<−35	<−35	<−35	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 20MHz	−60	<−50	<−50	<−45	dBc	HD3
equivalent input noise							
noise floor	>1MHz[1]	−158	<−155	<−155	<−154	dBm(1Hz)	SNF
integrated noise	1MHz to 150MHz[1]	35	<50	<50	<55	μV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		3	±10.0	±6.0	±11.0	mV	VIO
average temperature coefficient		20	±50	—	±50	μV/°C	DVIO
*input bias current	non-inverting	10	±36	±20	±20	μA	IBN
average temperature coefficient		100	±200	—	±100	nA/°C	DIBN
*input bias current	inverting	10	46	30	40	μA	IBI
average temperature coefficient		100	±200	—	±100	nA/°C	DIBI
power supply rejection ratio		55	50	50	50	dB	PSRR
♠common mode rejection ratio		55	50	50	50	dB	CMRR
*supply current	no load	15	21	21	21	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	200	>50	>100	>100	kΩ	RIN
	capacitance	0.5	<2.5	<2.5	<2.5	pF	CIN
output impedance	at DC	0.2	<0.3	<0.3	<0.3	Ω	RO
output voltage range	no load	3.5	>3.0	>3.2	>3.2	V	VO
common mode input range	for rated performance	2.8	>2.0	>2.5	>2.5	V	CMIR
output current	−40°C to +85°C	70	>35	>50	>50	mA	IO
	−55°C to +125°C	70	>30	>50	>50	mA	IO

Absolute Maximum Ratings

V_{CC}	±7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	±V_{CC}
differential input voltage	5V
junction temperature range	+175°C
operating temperature range	
AI/AJ:	−40°C to +85°C
A8/AM/AL:	−55°C to +125°C
storage temperature range	−65°C to +150°C
lead solder duration (+300°C)	10 sec

Miscellaneous Ratings

recommended gain range: +7 to +50, -1 to -50

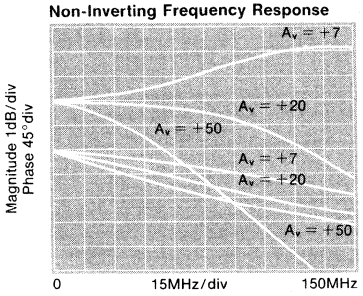
NOTES:

* AI, AJ	100% tested at +25°C, sample +85°C.
† AJ	Sample tested at +25°C.
† AI	100% tested at +25°C.
* A8	100% tested at +25°C, −55°C, +125°C.
† A8	100% tested at +25°C, sample −55°C, +125°C.
* AL, AM	100% wafer probe tested at +25°C to +25°C. min/max specifications.
♠ SMD	Sample tested at + 25°C, − 55°C, + 125°C.

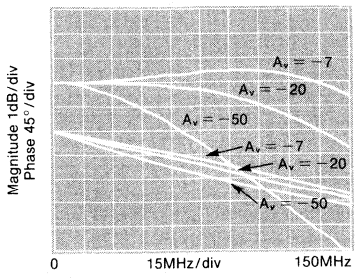
note 1: Noise tests are performed from 5MHz to 200MHz.
note 2: Gain flatness tests are performed from 0.1MHz.

Typical Performance Characteristics ($T_A = 25°C$, $A_v = +20$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$)

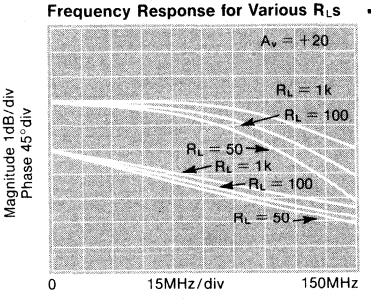
Non-Inverting Frequency Response



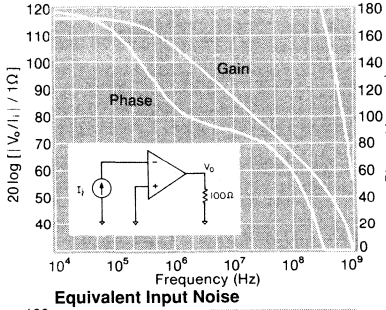
Inverting Frequency Response



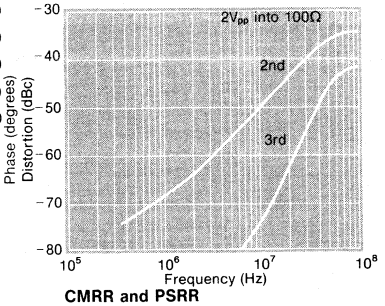
Frequency Response for Various R_Ls



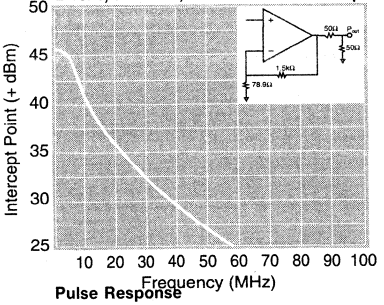
Open-Loop Transimpedance Gain, Z(s)



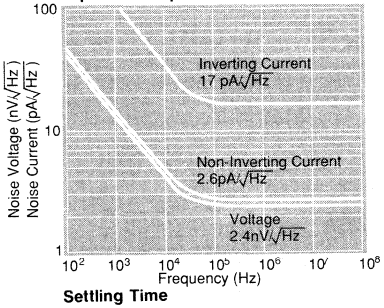
2nd and 3rd Harmonic Distortion



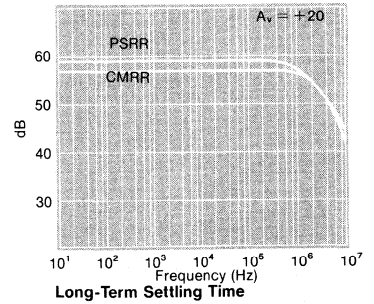
2-Tone, 3rd Order, Intermodulation Intercept



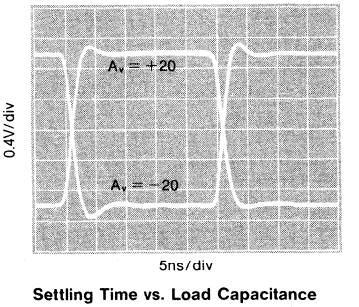
Equivalent Input Noise



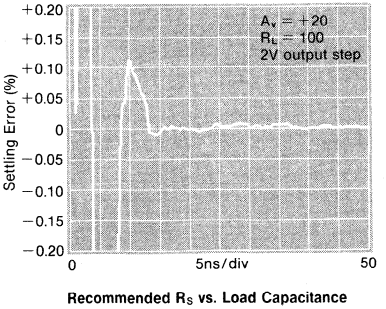
CMRR and PSRR



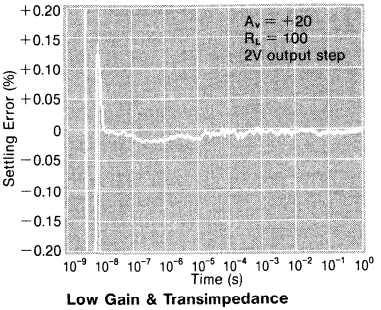
Pulse Response



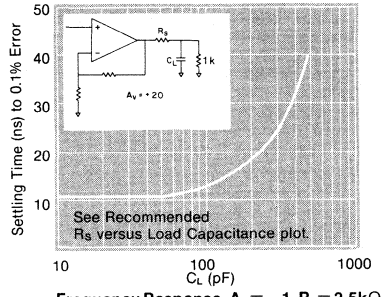
Settling Time



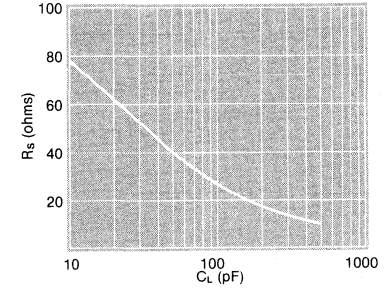
Long-Term Settling Time



Settling Time vs. Load Capacitance



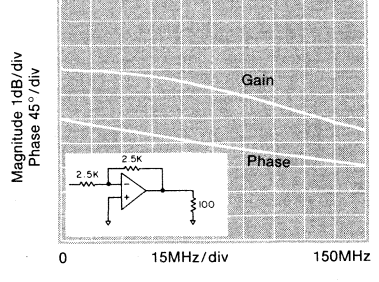
Recommended R_S vs. Load Capacitance

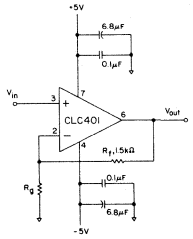


Low Gain & Transimpedance Applications

The CLC401 may be used at gains down to unity ($A_v = \pm 1$) by choosing R_f according to Equation (4) on the following page. The curves to the right show performance at inverting unity gain with $R_f = 2500\Omega$, a configuration appropriate for D/A converter buffering and other transimpedance applications.

Frequency Response, $A_v = -1$, $R_f = 2.5k\Omega$



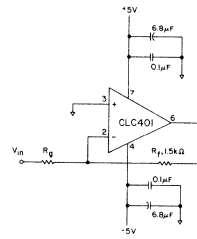


$$A_v = 1 + \frac{R_f}{R_g}$$

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

Figure 1: recommended non-inverting gain circuit



$$A_v = \frac{-R_f}{R_g}$$

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

Figure 2: recommended inverting gain circuit

ever, an understanding of the topology will aid in achieving the best performance. The discussion below will proceed for the non-inverting gain configuration with the inverting mode analysis being very similar.

Understanding the Loop Gain

Referring to the equivalent circuit of Figure 3, any current flowing in the inverting input is amplified to a voltage at the output through the transimpedance gain shown on the plot on page 3. This Z(s) is analogous to the open-loop gain of a voltage feedback amplifier.

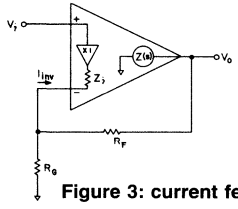


Figure 3: current feedback topology

Developing the non-inverting frequency response for the topology of Figure 3 yields:

$$\frac{V_o}{V_i} = \frac{1 + R_f/R_g}{1 - 1/LG} \qquad \text{eq. (1)}$$

where LG is the loop gain defined by,

$$LG = \frac{Z(s)}{R_f} \times \frac{1}{1 + Z_i/(R_f \,||\, R_g)} \qquad \text{eq. (2)}$$

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the LG expression. For an idealized treatment, set $Z_i = 0$ which results in a very simple $LG = Z(s)/R_f$. (Derivation of the transfer function for the case where $Z_i = 0$ is given in Application Note AN300-1.) Using the Z(s) (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended $R_f = 1.5k\Omega$, yields a large loop gain at DC. As a result, equation 1 shows that the closed-loop gain at DC is very close to $(1 + R_f/R_g)$.

At higher frequencies, the roll-off of Z(s) determines the closed-loop frequency response which, ideally, is dependent only on R_f. **The specifications reported on the previous pages are therefore valid only for the specified $R_f = 1.5k\Omega$.** Increasing R_f from 1.5kΩ will decrease the loop gain and bandwidth, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing R_f will hold the frequency response constant while the closed-loop gain can be adjusted using R_g.

The CLC401 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC401, $Z_i \cong 50\Omega$ leading to a drop in loop gain and bandwidth at high gain settings, as given by equation 2. The second term in equation 2 accounts for the division in feedback current that occurs between Z_i and $R_f \,||\, R_g$ at the inverting node of the CLC400. This decrease in bandwidth can be circumvented as described in "Increasing Bandwidth at High Gains."

DC Accuracy and Noise

Since the two inputs for the CLC401 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin resistance.

$$\text{Output Offset } V_o = \pm \text{IBN} \times R_s\,(1 + R_f/R_g) \pm \text{VIO}\,(1 + R_f/R_g) \pm \text{IBI} \times R_f \qquad \text{eq. (3)}$$

An important observation is that for fixed R_f, offsets as referred to the input improve as the gain is increased (divide all terms by $1 + R_f/R_g$). A similar result is obtained for noise where noise figure improves as gain increases.

Selecting Between the CLC400 or CLC401

The CLC400 is intended for gains of ±1 to ±8 while the CLC401 is designed for gains of ±7 to ±50. Optimum performance is achieved with a feedback resistor of 250Ω with the CLC400 and 1.5kΩ with the CLC401—this distinction may be important in transimpedance applications such as D/A buffering. Although the CLC400 can be used at higher gains, the CLC401 will provide a wider bandwidth because loop gain losses due to finite Z_i are lower with the larger CLC401 feedback resistor as explained above. On the other hand, the lower recommended feedback resistance of the CLC400 minimizes the output errors due to inverting input noise and bias currents.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting R_f and R_g to make up for the losses in loop gain that occur at these high gain settings due to current division at the inverting input. An approximate relationship may be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, $R_f = 1.5k\Omega$ and $R_g = 79\Omega$). For the CLC401 this gives,

$$R_f = 2500 - 50A_v \text{ and } R_g = \frac{2500 - 50A_v}{A_v - 1} \qquad \text{eq. (4)}$$

where A_v is the desired non-inverting gain. Note that with $A_v = +20$ we get the specified $R_f = 1.5k\Omega$, while at higher gains, a lower value gives stable performance with improved bandwidth.

Capacitive Feedback

Capacitive feedback should not be used with the CLC401 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC401.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part no. 730013 for through-hole and 730027 for SOIC) for the CLC401 are available.

Comlinear Corporation

Low-Gain Op Amp with Fast 14-Bit Settling

CLC402

APPLICATIONS:

- high-accuracy A/D systems (12-14 bits)
- high-accuracy D/A converters
- high-speed communications
- IF signal processing
- video distribution

FEATURES (typical):

- 0.0025% settling in 25ns (32ns max.)
- 0.5mV input offset voltage, 3μV/°C drift
- ±1 to ±8 closed-loop gain range
- low power, 150mW
- 0.01%/0.05° differential gain/phase

DESCRIPTION:

The CLC402 is an operational amplifier designed for low-gain applications (±1 to ±8), requiring fast, accurate settling and superior DC accuracy. Settling to 0.0025% in 25ns (32ns guaranteed over temperature), the CLC402 is ideal as the input amplifier in high accuracy (up to 14-bits) A/D systems. Unlike most other high-speed op amps, the CLC402 is free of thermally induced tails in the settling response.

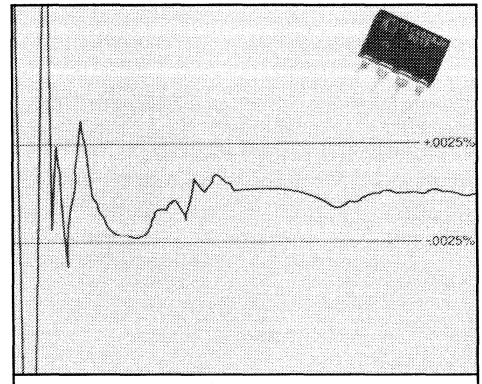
The CLC402 is an upgrade to and pin compatible with the industry standard CLC400. Constructed using a unique, proprietary design and an advanced complementary bipolar process, it offers performance far beyond ordinary monolithic op amps. In addition, unlike many other high-speed op amps, the CLC402 offers both high performance and stability without the need for compensation circuitry – even at a gain of +1.

Supporting the CLC402's excellent pulse performance are improved DC characteristics. The CLC402's input offset voltage is typically 0.5mV and is guaranteed to be less than 1.6mV at +25°C. The input offset voltage drift is typically only 3μV/°C.

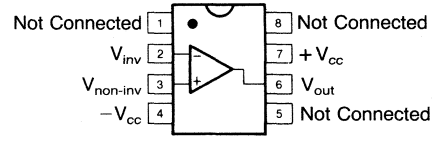
The CLC402 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC402AJP	– 40°C to + 85°C	8-pin plastic DIP
CLC402AJE	– 40°C to + 85°C	8-pin plastic SOIC
CLC402AID	– 40°C to + 85°C	8-pin hermetic side-brazed ceramic DIP
CLC402A8D	– 55°C to + 125°C	8-pin hermetic side-brazed ceramic DIP, MIL-STD-883, Level B
CLC402ALC	– 55°C to + 125°C	dice
CLC402AMC	– 55°C to + 125°C	dice qualified to Method 5008, MIL-STD-883, Level B

Contact factory for other packages. DESC SMD number, 5962-92033.

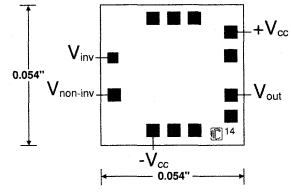


PINOUT



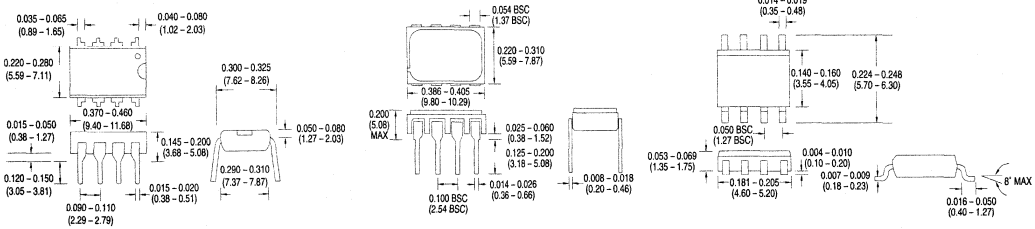
DIP and SO-8 Versions

Chip Topography



Height is 0.014 inches.
NOTE: Backside connected to $-V_{cc}$. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



8-pin plastic DIP **8-pin side-brazed ceramic DIP** **8-pin plastic SOIC**

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics ($R_f = 100\Omega$, $V_{CC} = \pm 5V$, $A_V = +2$, $R_f = 250\Omega$)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC402A8/AL/AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC402AJ/AI	+25°C	−40°C	+25°C	+ 85°C		
FREQUENCY DOMAIN PERFORMANCE							
†-3dB bandwidth	$V_{out}<0.5V_{pp}$	195	>120	>130	>120	MHz	SSBW
	$V_{out}<5V_{pp}$	80	>50	>50	>50	MHz	LSBW
gain flatness[2]	$V_{out}<0.5V_{pp}$						
† peaking	DC to 25MHz	0	<0.4	<0.3	<0.4	dB	GFPL
† peaking	>25MHz	0	<0.7	<0.5	<0.7	dB	GFPH
† rolloff	DC to 50MHz	0.5	<1.0	<1.0	<1.0	dB	GFR
linear phase deviation	DC to 50MHz	0.4	<1.2	<1.0	<1.2	°	LPD
TIME DOMAIN PERFORMANCE							
rise and fall time	0.5V step	2.0	<2.9	<2.7	<2.9	ns	TRS
	5V step	5.0	<8	<8	<8	ns	TRL
settling time to ±0.0025%	2Vstep	25	<32	<32	<32	ns	TS14
±0.01%	2V step	18	<25	<25	<25	ns	TSP
±0.1%	2V step	10	<15	<15	<15	ns	TSS
overshoot	0.5V step	0	<10	<10	<10	%	OS
slew rate		800	>500	>500	>500	V/μs	SR
DISTORTION AND NOISE PERFORMANCE							
†2nd harmonic distortion	$2V_{pp}$, 20MHz	−50	<−38	<−43	<−43	dBc	HD2
†3rd harmonic distortion	$2V_{pp}$, 20MHz	−60	<−53	<−53	<−50	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−157	<−155	<−155	<−155	dBm(1Hz)	SNF
integrated noise	1MHz to 150MHz	40	<49	<49	<49	μV	INV
differential gain[1]		0.01	—	—	—	%	DG
differential phase[1]		0.05	—	—	—	°	DP
STATIC, DC PERFORMANCE							
*input offset voltage		0.5	<2.6	<1.6	<2.8	mV	VIO
average temperature coefficient		3	<12	—	<12	μV/°C	DVIO
*input bias current	noninverting	10	<45	<25	<35	μA	IBN
average temperature coefficient		100	<250	—	<100	nA/°C	DIBN
*input bias current	inverting	10	<50	<30	<40	μA	IBI
average temperature coefficient		100	<250	—	<100	nA/°C	DIBI
†power supply rejection ratio		68	>55	>60	>60	dB	PSRR
common mode rejection ratio		65	>55	>60	>60	dB	CMRR
*supply current	no load	15	<20	<20	<20	mA	ICC
MISCELLANEOUS PERFORMANCE							
noninverting input	resistance	150	>50	>85	>85	kΩ	RIN
	capacitance	3.5	<5.5	<5.5	<5.5	pF	CIN
output impedance	at DC	0.02	<0.1	<0.1	<0.1	Ω	RO
common mode input range		±3.0	>±2.0	>±2.5	>±2.5	V	CMIR
output voltage range	no load	±3.5V	>±3.0	>±3.2	>±3.2	V	VO
output current		±55	>±25	>±45	>±45	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but, maximum reliability will be obtained if I_{out} does not exceed...	70mA
input voltage	$\pm V_{cc}$
junction temperature	+175°C
operating temperature range	
AI/AJ:	− 40°C to +85°C
A8/AM/AL:	− 55°C to +125°C
storage temperature range	− 65°C to +150°C
lead solder duration (+300°C)	10 sec

Miscellaneous Ratings

recommended gain range: ±1 to ±8

Notes:

*	AI, AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested at +25°C, − 55°C, +125°C.
†	A8	100% tested at +25°C, sample at − 55°C, +125°C.
*	AL, AM	100% wafer probe tested at +25°C to +25°C min/max specifications.

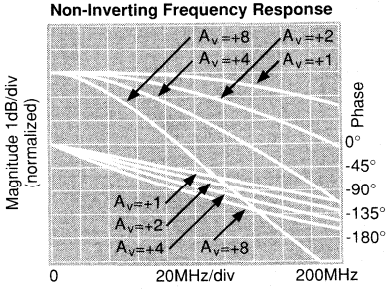
note 1: Differential gain and phase measured at $A_v = +2V$, $R = 250\Omega$, $R_L = 150\Omega$, $1V_{pp}$ equivalent video signal, 0-100 IRE, 40 IRE_{pp}, 0IRE = 0 volts, 75Ω load and 3.58 MHz.

note 2: Gain flatness tests performed from 0.1MHz.

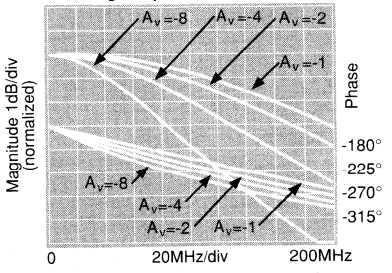
Comlinear reserves the right to change specifications without notice.

Typical Performance Characteristics (T_A =+25°C, A_V =+2, V_{CC} =±5V, R_L =100Ω, R_f =250Ω)

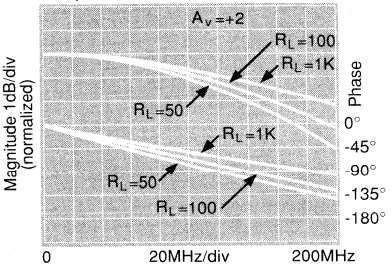
Non-Inverting Frequency Response



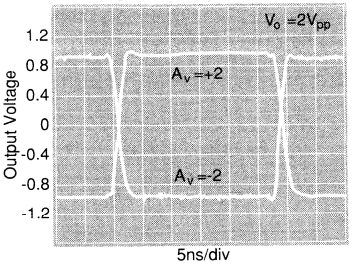
Inverting Frequency Response



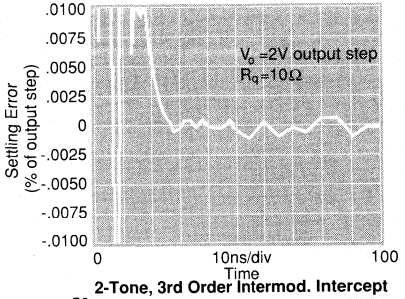
Frequency Response vs. Load (R_L)



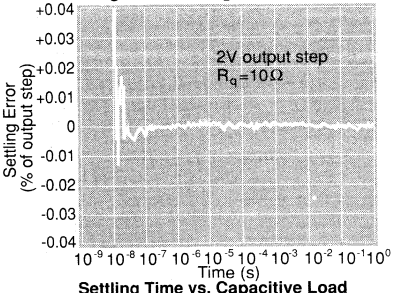
Small Signal Pulse Response



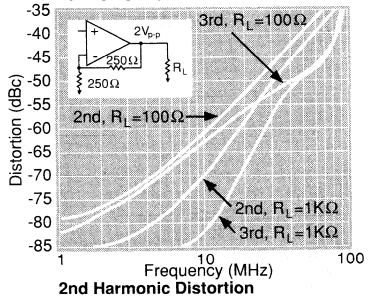
Short Term Settling Response



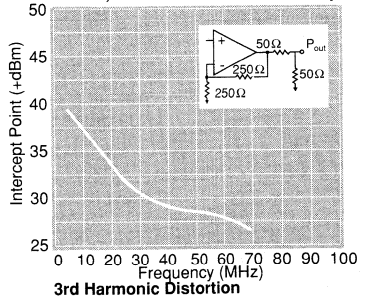
Long-Term Settling



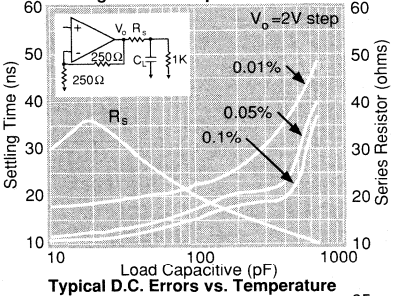
Harmonic Distortion



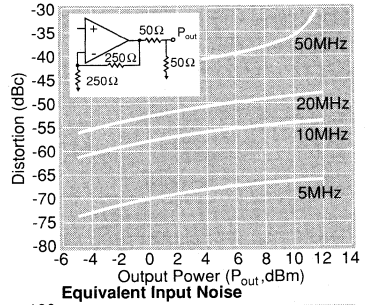
2-Tone, 3rd Order Intermod. Intercept



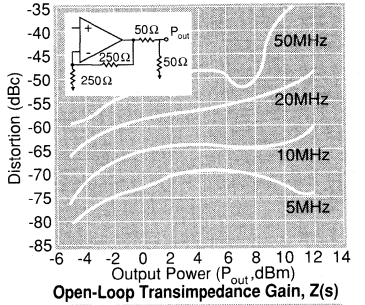
Settling Time vs. Capacitive Load



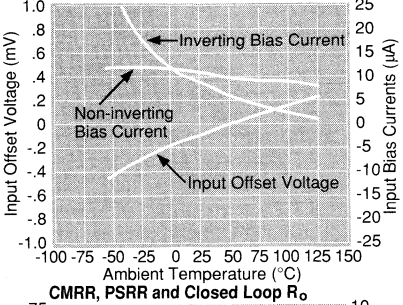
2nd Harmonic Distortion



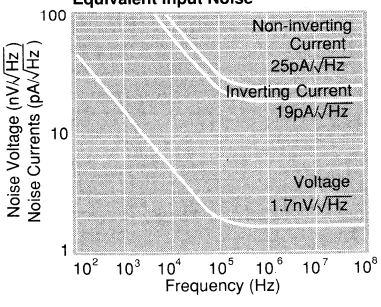
3rd Harmonic Distortion



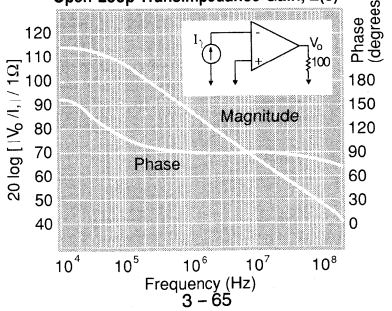
Typical D.C. Errors vs. Temperature



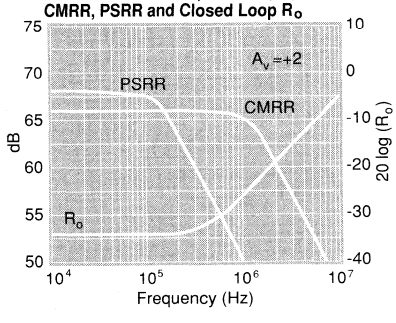
Equivalent Input Noise



Open-Loop Transimpedance Gain, Z(s)



CMRR, PSRR and Closed Loop R_o



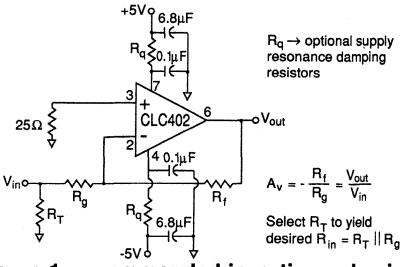


Figure 1: recommended inverting gain circuit

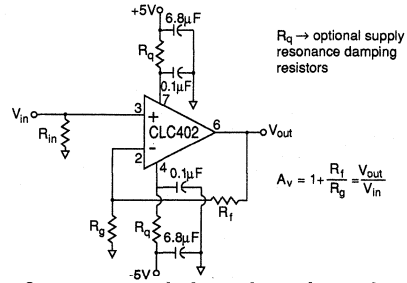


Figure 2: recommended non-inverting gain circuit

Feedback Resistor

The CLC402 achieves its excellent pulse response by using the current feedback topology pioneered by Comlinear Corporation. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The CLC402 is optimized for use with a 250Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 discusses this in detail along with occasions where a different R_f might be advantageous.

Optimizing Settling Time

The CLC402 is capable of extremely fast pulse settling times to very fine scale accuracies (.0025% in 25ns typical). It is also virtually free of any measurable thermal tail effects as shown in the long-term settling time plot on the previous page. Careful attention to parasitic effects is critical to achieving this level of performance.

Generally, open any ground and/or power planes around the device while providing an adjacent ground plane for the 0.1µf ceramic decoupling caps. These caps should be very near the power pins. Connecting the ground return point for the electrolytic capacitors near the load ground point is also very useful. Similarly, for non-inverting applications, connecting R_g to ground near the input terminating resistor ground connection will improve performance. These suggestions become particularly pertinent for fastest settling to lower than 0.1% accuracies.

Using Supply Resistors, R_q

Figures 1 and 2 show a series resistor in the supply leads between the electrolytic and ceramic capacitors. This optional resistor is intended to de-Q any self-resonance between those capacitors and the power supply trace inductance. Any large output voltage step into a significant load, either resistive or capacitive, will necessarily pull a current surge through the supply de-coupling capacitors. This can cause a very low level, high frequency ringing on the power supplies that may not be effectively rejected by the PSRR of the CLC402. This can, in turn, show up at the output as a ringing that will preclude high speed settling to very fine scale accuracies.

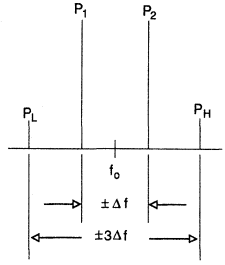
Adding R_q will increase the amplitude of this signal at the supplies but will lower the frequency content to where the CLC402's PSRR can effectively reject it. An R_q of 5 to 10Ω will yield excellent settling performance with minimal impact on other performance parameters.

Driving Capacitive Loads

Either parasitic or load capacitance directly on the output pin can quickly lead to unacceptable levels of ringing in the pulse response. Adding a series resistor, as shown in the plot of R_s vs. C_L on the previous page, will resolve this problem. Parasitic capacitances less than 2pF can be driven without the series resistor. See Application Note OA-15 for additional discussion.

Distortion Performance

The distortion plots show the harmonic distortions and 3rd order intermodulation intercepts under a variety of load, power, and frequency conditions. Generally, going to higher frequencies will degrade the distortion performance as the amplifier loop gain decreases. Further distortion improvements at low frequencies are observed when driving higher impedance loads. The 3rd order intermodulation intercept plot may be used to predict the 3rd order spurious levels given the power levels at the load for two closely spaced signal frequencies. Figure 3 shows the signal and spurious level definitions along with equations for predicting the spurious powers from the intercept value and the two signal powers.



P_1, P_2 – test powers at load

P_L, P_H – 3rd order spurious powers (all in dBm)

IM3 – 3rd order intercept (from datasheet plot)

$P_L = P_2 - 2\,(IM3 - P_1)$

$P_H = P_1 - 2\,(IM3 - P_2)$

Figure 3: 3rd order spurious calculations

DC Accuracy and Noise

The CLC402 offers an improved offset voltage over the comparable CLC400 low gain amplifier. The offset adjustment available on the CLC400 was therefore not included in this part. Figure 4 shows the output offset computational equation for the non-inverting configuration with an example using the typical bias current and offset specifications for $A_v = +2$.

Output Offset

$$V_o = \left(\pm I_{bn} R_{in} \pm V_{io}\right)\left(1 + \frac{R_f}{R_g}\right) \pm I_{bi}\, R_f$$

Example computation for $A_v = +2$, $R_f = 250\Omega$

$V_o = (\pm 10\mu A\,(50\Omega) \pm 0.5mV)\,(2) \pm 10\mu A\,(250\Omega) = \pm 3.5mV$

Figure 4: Output DC offset calculation

This low output offset voltage is a marked improvement over earlier very high speed amplifiers. Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7.

The equivalent input noise plot shows that the CLC402 offers a low $1.7nV/\sqrt{Hz}$ input noise voltage. A low non-inverting source impedance should be used for lowest noise performance due to the relatively high current noise at that input. See Application Note OA-12 for a full discussion of noise calculations for current feedback amplifiers.

Printed Circuit Layout

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC402 are available. This board can be easily modified to include the R_q resistors discussed above. Further layout suggestions may be found in Application Note OA-15.

Comlinear Corporation

Wideband, High-Slew Rate, Monolithic Op Amp

CLC404

APPLICATIONS:

- fast A/D conversion
- line driving
- video distribution
- high-speed communications
- radar, IF processors

FEATURES (typical):

- 165MHz large signal bandwidth ($5V_{pp}$)
- 2600V/μs slew rate
- low power: 110mW
- low distortion: -53dBc at 20MHz
- 10ns settling to 0.2%
- 0.07% differential gain, 0.03° differential phase

DESCRIPTION:

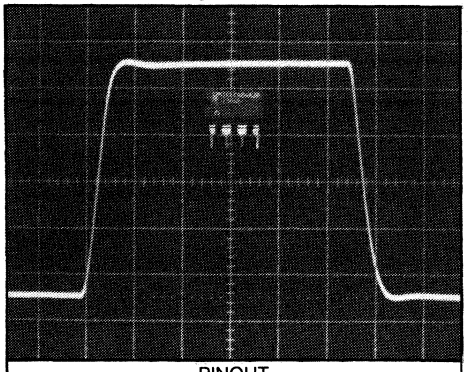
The CLC404 is a high-speed, monolithic op amp that combines low power consumption (110mW typical, 120mW maximum) with superior large signal performance. Operating off of ±5V supplies, the CLC404 demonstrates a large-signal bandwidth ($5V_{pp}$ output) of 165MHz. The bandwidth performance, along with other speed characteristics such as rise and fall time (2.1ns for a 5V step), is nearly identical to the small signal performance since slew rate is not a limiting factor in the CLC404 design.

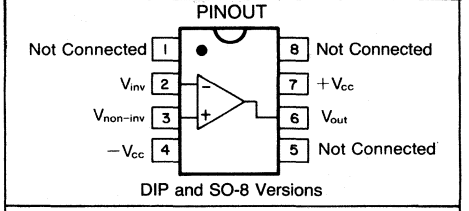
With its 175MHz bandwidth and 10ns settling (to 0.2%), the CLC404 is ideal for driving ultra-fast flash A/D converters. The 0.5° deviation from linear phase, coupled with -53dBc 2nd harmonic distortion and -60dBc 3rd harmonic distortion (both at 20MHz), is well suited for many digital and analog communication applications. These same characteristics, along with 70mA output current, differential gain of 0.07%, and differential phase at 0.03°, make the CLC404 an appropriate high-performance solution for video distribution and line driving applications.

Constructed using an advanced, complementary bipolar process and Comlinear's proven current feedback topologies, the CLC404 provides performance far beyond that of other monolithic op amps. The CLC404 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

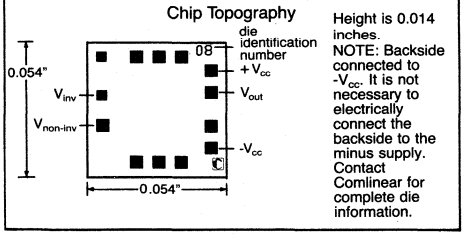
CLC404AJP	– 40°C to + 85°C	8-pin plastic DIP
CLC404AJE	– 40°C to + 85°C	8-pin plastic SOIC
CLC404AID	– 40°C to + 85°C	8-pin hermetic side-brazed ceramic DIP
CLC404A8D	– 55°C to + 125°C	8-pin hermetic side-brazed ceramic DIP, MIL-STD-883, Level B
CLC404ALC	– 55°C to + 125°C	dice
CLC404AMC	– 55°C to + 125°C	dice qualified to Method 5008, MIL-STD-883, Level B

Contact factory for other packages. DESC SMD number, 5962-90994.



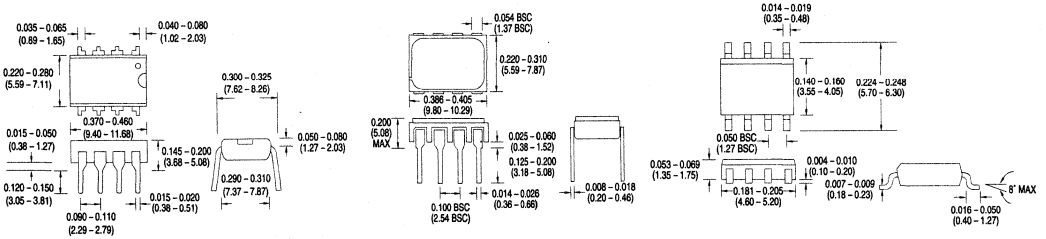


DIP and SO-8 Versions



Height is 0.014 inches.
NOTE: Backside connected to $-V_{cc}$. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



8-pin plastic DIP | 8-pin side-brazed ceramic DIP | 8-pin plastic SOIC

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

DS404.05 January 1993

Electrical Characteristics (A_V = +6, V_{CC} = ±5V, R_f = 500Ω, Rg = 100Ω, R_L = 100Ω)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC404A8/AL/AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC404AJ/AI	+25°C	−40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
†-3dB bandwidth	Vout<$2V_{pp}$	175	>150	>150	>120	MHz	SSBW
-3dB large signal	Vout<$5V_{pp}$	165	>140	>140	>110	MHz	LSBW
gain flatness[3]	Vout<$2V_{pp}$						
† peaking	<40MHz	0	<0.4	<0.3	<0.4	dB	GFPL
† peaking	>40MHz	0	<0.7	<0.5	<0.7	dB	GFPH
† rolloff	<75MHz	0.2	<1.0	<1.0	<1.3	dB	GFR
linear phase deviation	DC to 75MHz	0.5	<1.0	<1.0	<1.2	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.0	<2.4	<2.4	<2.9	ns	TRS
	5V step	2.1	<2.6	<2.6	<3.2	ns	TRL
settling time to ±0.2%	2V step	10	<15	<15	<15	ns	TS
overshoot	2V step	5	<15	<12	<15	%	OS
slew rate (measured at A_v +2)[1]		2600	>2000	>2000	>2000	V/μs	SR
DISTORTION AND NOISE RESPONSE							
† 2nd harmonic distortion	$2V_{pp}$, 20MHz	−53	<−40	<−45	<−45	dBc	HD2
† 3rd harmonic distortion	$2V_{pp}$, 20MHz	−60	<−50	<−50	<−50	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−159	<−157	<−157	<−156	dBm(1Hz)	SNF
integrated noise	1MHz to 200MHz	40	<45	<45	<50	μV	INV
differential gain[2]		0.07	—	—	—	%	DG
differential phase[2]		0.03	—	—	—	°	DP
STATIC, DC PERFORMANCE							
* input offset voltage		2	<±9.0	<±5.0	<±10.0	mV	VIO
average temperature coefficient		30	<±50	—	<±50	μV/°C	DVIO
* input bias current	non-inverting	15	<±44	<±22	<±22	μA	IBN
average temperature coefficient		150	<±275	—	<±200	nA/°C	DIBN
* input bias current	inverting	15	<±40	<±18	<±22	μA	IBI
average temperature coefficient		150	<±275	—	<±200	nA/°C	DIBI
† power supply rejection ratio		52	>45	>48	>45	dB	PSRR
♠ common mode rejection ratio		50	>44	>46	>44	dB	CMRR
* supply current	no load, quiescent	11	<12	<12	<12	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	1000	>250	>500	>1000	kΩ	RIN
	capacitance	1	<2	<2	<2	pF	CIN
output impedance	at DC	0.1	<0.3	<0.2	<0.2	Ω	RO
output voltage range	no load	±3.3	>±2.8	>±3.0	>±3.0	V	VO
common mode input range for rated performance		±2.2	>±1.4	>±1.8	>±2.0	V	CMIR
output current	−40°C to +85°C	±70	>±35	>±50	>±50	mA	IO
	−55°C to +125°C	±70	>±30	>±50	>±50	mA	IO

Absolute Maximum Ratings

V_{CC}	±7V
output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	$\pm V_{CC}$
differential input voltage	10V
junction temperature	+ 175°C
operating temperature range	
AI/AJ:	− 40°C to + 85°C
A8/AM/AL:	− 55°C to + 125°C
storage temperature range	− 65°C to + 150°C
lead solder duration (+ 300°C)	10 sec

Miscellaneous Ratings

recommended gain range: + 2 to + 21, − 1 to − 20

NOTES:

*	AI, AJ	100% tested at + 25°C, sample at + 85°C.
†	AJ	Sample tested at + 25°C.
†	AI	100% tested at + 25°C.
*	A8	100% tested at + 25°C, − 55°C, + 125°C.
†	A8	100% tested at + 25°C, sample − 55°C, + 125°C.
♠	SMD	Sample tested at + 25°C, − 55°C, + 125°C.
*	AL, AM	100% wafer probe tested at + 25°C to + 25°C. min/max specifications.

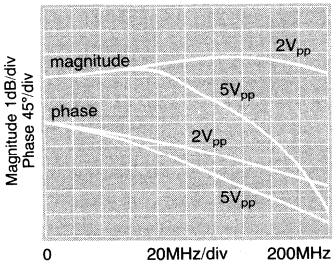
note 1: See the text on the back page of the datasheet.

note 2: Differential gain and phase measured at A_v + 2, R_f 500Ω, R_L 150Ω 1V_{pp} equivalent video signal, 0-100 IRE, 40 IRE$_{pp}$, 0IRE = 0 volts, at 75Ω load and 3.58MHz. See text.

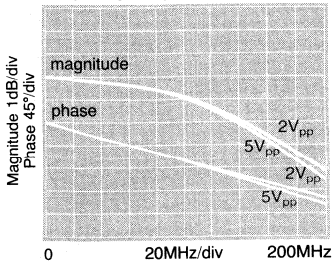
note 3: Gain flatness tests are performed from 0.1MHz.

Typical Performance Characteristics (T_A = +25°C, A_V = +6, R_f = 500Ω, R_L = 100Ω)

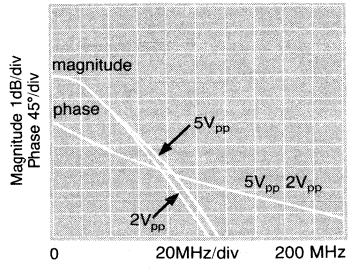
Frequency Response, A_V = +2



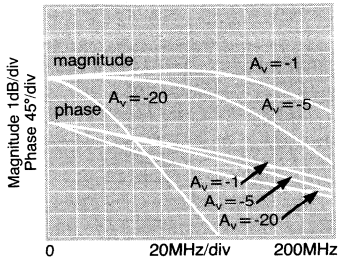
Frequency Response, A_V = +6



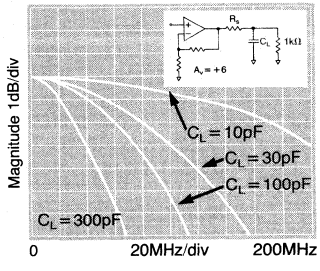
Frequency Response, A_V = +21



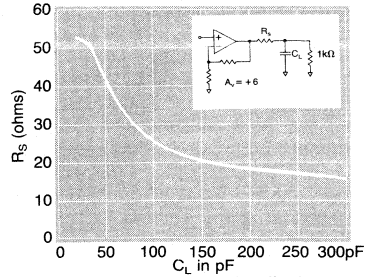
Inverting Frequency Response



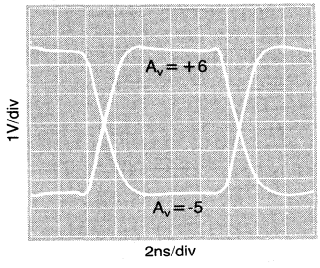
Bandwidth vs Load Capacitance



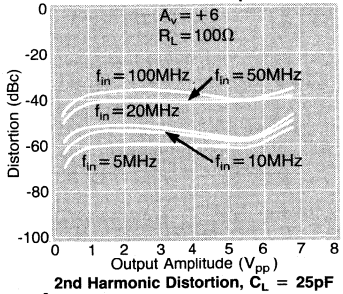
Recommended R_S vs Load Capacitance



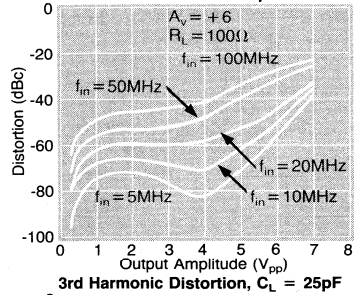
Large Signal Pulse Response



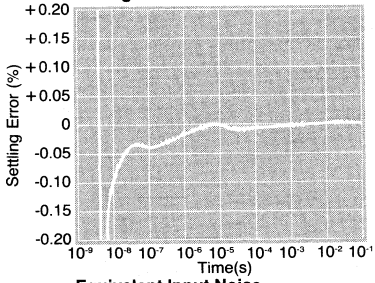
2nd Harmonic Dist. vs Amplitude



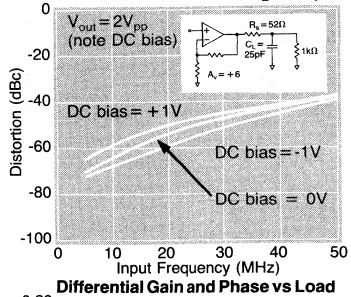
3rd Harmonic Dist. vs Amplitude



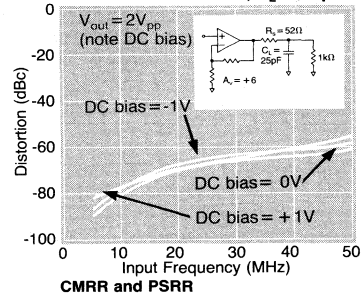
Settling Time



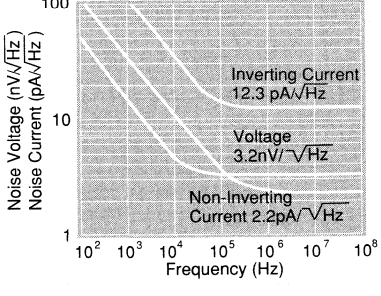
2nd Harmonic Distortion, C_L = 25pF



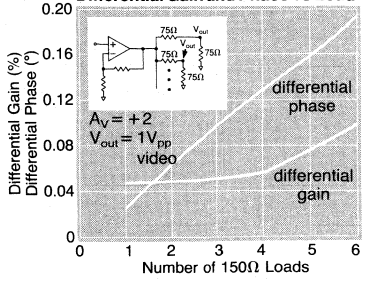
3rd Harmonic Distortion, C_L = 25pF



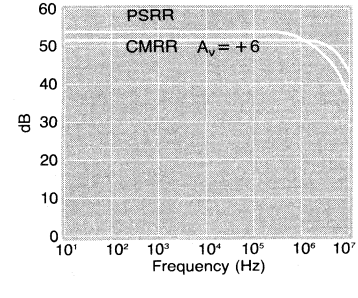
Equivalent Input Noise

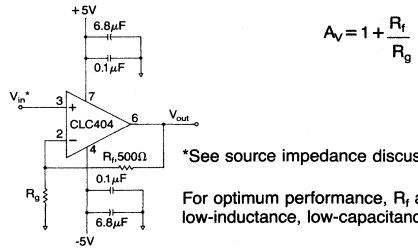


Differential Gain and Phase vs Load



CMRR and PSRR





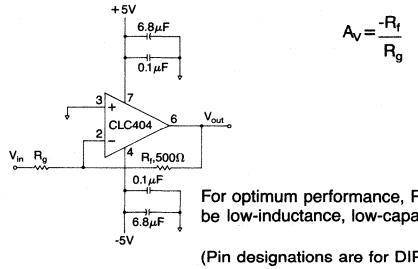
$$A_V = 1 + \frac{R_f}{R_g}$$

*See source impedance discussion.

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

Figure 1: recommended non-inverting gain circuit



$$A_V = \frac{-R_f}{R_g}$$

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

Figure 2: recommended inverting gain circuit

Slew Rate

Slew rate limiting is a nonlinear response which occurs in amplifiers when the output voltage swing approaches hard, abrupt limits in the speed at which it can change. In most applications, this results in an easily identifiable "slew rate" as well as a dramatic increase in distortion for large signal levels. The CLC404 has been designed to provide enough slew rate to avoid slew rate limiting in almost all circuit configurations. The large signal bandwidth of 165MHz, therefore, is nearly the same as the 175MHz small signal bandwidth. The result is a low-distortion, linear system for both small signals *and* large signals.

Slew rate and large signal performance in the CLC404 can best be understood by first comparing the small and large signal performance plots at a gain of +6. In the CLC404, there is almost no difference between large and small signal performance at this gain. Large signal performance in the CLC404 at a gain of +6 is not slew rate limited. (In an amplifier which is slew limiting, the large signal response rolloff has an abrupt break indicating the onset of slew rate limitation.)

The CLC404 reaches slew rate limits only for low non-inverting gains. In other words, slew rate limiting is constrained by common mode voltage swings at the input. (This is different from traditional slew rate constraints.) The large-signal frequency response plot at a gain of +2 shows a break in the response, which shows that slew rate limit has been reached. Note also that the frequency response plots at gain of +21 show that the large signal and small signal responses are nearly identical.

Differential Gain and Phase

Differential gain and phase are measurements useful primarily in composite video channels. Differential gain and phase are measured by monitoring the gain and phase of a high frequency carrier (3.58MHz for NTSC composite video) as the output of the amplifier is swept over a range of DC voltages. Any changes in gain and phase at the carrier frequency are the desired measurement, differential gain and phase.

Specifications for the CLC404 include differential gain and phase. The test signals used are based on a $1V_{pp}$ video level. Test conditions used are the following:

DC sweep range:	0 to 100 IRE units (black to white)
Carrier:	3.58MHz at 40 IRE units peak to peak

The amplifier is specified for a gain of +2, and 150Ω load (for a backmatched 75Ω system). IRE amplitudes are referred to 75Ω, at the load of a video system. This is a different condition from the rest of the specifications ($A_v = +6, R_l = 100\Omega$).

Source Impedance

For best results, source impedance in the non-inverting circuit configuration (see Figure 1) should be kept below 3kΩ. Above 3kΩ it is possible for oscillation to occur, depending on other circuit parasitics. Depending on the signal source, a resistor with a value of less than 3kΩ may be used to terminate the non-inverting input to ground.

Feedback Resistor

In current-feedback op amps, the value of the feedback resistor plays a major role in determining amplifier dynamics. It is important to select the correct value resistor. The CLC404 provides optimum performance with a 500Ω feedback resistor. Furthermore, the specifications shown on the previous pages are valid only when a 500Ω feedback resistor is used. Selection of an incorrect value can lead to severe rolloff in frequency-response (if the resistor value is too large) or peaking or oscillation (if the value is too low). See Comlinear application notes AN and AN 300-1 for a complete discussion of current feedback.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC404 are available.

Comlinear Corporation

Wideband, Low Power Monolithic Op Amp

CLC406

APPLICATIONS:

- video distribution amp
- HDTV amplifier
- flash A/D driver
- D/A transimpedance buffer
- pulse amplifier
- photo-diode amp
- LAN amplifier

FEATURES (typical):

- 160MHz small signal bandwidth
- 50mW power (±5V supplies)
- 0.02%/0.02° differential gain/phase
- 12ns settling to 0.05%
- 1500V/μs slew rate
- 2.2ns rise and fall time ($2V_{pp}$)
- 70mA output current

DESCRIPTION:

The CLC406 is a wideband monolithic operational amplifier designed for low-gain applications where power and cost are of primary concern. Operating from ±5V supplies, the CLC406 consumes only 50mW of power yet maintains a 160MHz small signal bandwidth and a 1500V/μs slew rate. Benefitting from Comlinear's current feedback architecture, the CLC406 offers a gain range of ±1 to ±10 while providing stable, oscillation free operation without external compensation, even at unity gain.

With its exceptional differential gain and phase, typically 0.02% and 0.02° at 3.58MHz, the CLC406 is designed to meet the performance and cost requirements of high volume composite video applications. The CLC406's large signal bandwidth, high slew rate and high drive capability are features well suited for RGB video applications.

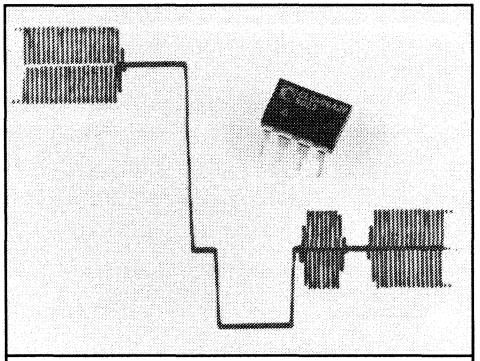
Providing a 12ns settling time to 0.05% (1/2 LSB in 10-bit systems) and −68/−75dBc 2nd/3rd harmonic distortion ($2V_{pp}$ at 10MHz, $R_L = 1k\Omega$), the CLC406 is an excellent choice as a buffer or driver for high speed A/D and D/A converter systems.

Commercial remote sensing applications and battery powered radio transceivers requiring a high performance, low power amplifier will find the CLC406 to be an attractive, cost-effective solution.

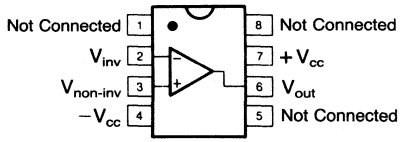
Constructed using an advanced, complementary bipolar process and Comlinear's proven current feedback architectures, the CLC406 is available in several versions to meet a variety of requirements.

CLC406AJP	− 40°C to + 85°C	8-pin plastic DIP
CLC406AJE	− 40°C to + 85°C	8-pin plastic SOIC
CLC406AIB	− 40°C to + 85°C	8-pin hermetic CERDIP
CLC406A8B	− 55°C to + 125°C	8-pin hermetic CERDIP, MIL-STD-883, Level B
CLC406ALC	− 55°C to + 125°C	dice
CLC406AMC	− 55°C to + 125°C	dice qualified to Method 5008, MIL-STD-883, Level B

Contact factory for other packages. DESC SMD number, 5962-92004.

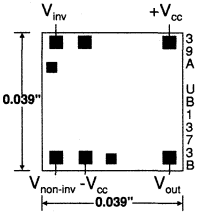


Pinout



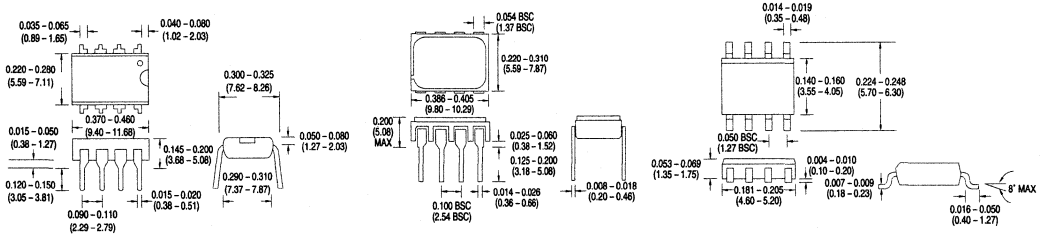
DIP and SO-8 Versions

Chip Topography



Height is 0.014 inches. NOTE: Backside connected to $-V_{cc}$. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



8-pin plastic DIP **8-pin side-brazed ceramic DIP** **8-pin plastic SOIC**

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics ($A_V = +6$; $V_{CC} = \pm 5V$; $R_L = 100\Omega$; $R_f = 500\Omega$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC406AJ/AI	+25°C	−40°C	+25°C	+ 85°C		
Ambient Temperature	CLC406A8/AL/AM	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN PERFORMANCE							
† − 3db bandwidth[1]	$V_{out}<2V_{pp}$	160	>110	>110	>90	MHz	SSBW
	$V_{out}<5V_{pp}$	130	>95	>95	>80	MHz	LSBW
gain flatness[2]	$V_{out}<2V_{pp}$						
† peaking	DC to 25MHz	0	<0.2	<0.2	<0.2	dB	GFPL
† peaking	>25MHz	0	<0.5	<0.5	<0.5	dB	GFPH
† rolloff	DC to 50MHz	0	<0.6	<0.6	<1.0	dB	GFR
linear phase deviation	DC to 75MHz	0.2	<0.8	<0.8	<1.2	°	LPD
differential gain	($A_V = +2$) 150Ω load, 3.58MHz	0.02	<0.04	<0.04	<0.04	%	DG1
	4.43MHz	0.02	<0.04	<0.04	<0.04	%	DG2
differential phase	($A_V = +2$) 150Ω load, 3.58MHz	0.02	<0.04	<0.04	<0.08	°	DP1
	4.43MHz	0.025	<0.05	<0.05	<0.10	°	DP2
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.2	<3.0	<3.0	<3.9	ns	TRS
	4V step	3.0	<3.6	<3.6	<5.0	ns	TRL
settling time to 0.05%	2Vstep	12	<18	<18	<20	ns	TS
overshoot	2V step	8	<15	<15	<15	%	OS
slew rate		1500	>1200	>1200	>1000	V/μs	SR
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	† $2V_{pp}$, 20MHz, $R_L = 100\Omega$	−46	<−42	<−42	<−38	dBc	HD2
	$2V_{pp}$, 10MHz, $R_L = 1k\Omega$	−68	<−62	<−62	<−60	dBc	HD2L
3rd harmonic distortion	† $2V_{pp}$, 20MHz, $R_L = 100\Omega$	−50	<−46	<−46	<−42	dBc	HD3
	$2V_{pp}$, 10MHz, $R_L = 1k\Omega$	−75	<−70	<−70	<−65	dBc	HD3L
equivalent input noise							
non-inverting voltage	>1MHz	2.7	3.4	3.4	3.8	nV/√Hz	VN
inverting current	>1MHz	11.0	13.9	13.9	15.5	pA/√Hz	ICN
non-inverting current	>1MHz	2.1	2.6	2.6	3.0	pA/√Hz	NCN
total noise floor	>1MHz	−157	<−156	<−156	−155	dBm_{1Hz}	SNF
total integrated noise	1MHz to 100MHz	31	<38	<38	<42	μV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		2	<10	<6	<12	mV	VIO
average temperature coefficient		30	<60	—	<60	μV/°C	DVIO
*input bias current	non-inverting	5	<24	<12	<12	μA	IBN
average temperature coefficient		30	<125	—	<50	nA/°C	DIBN
*input bias current	inverting	3	<23	<15	<20	μA	IBI
average temperature coefficient		20	<100	—	<50	nA/°C	DIBI
†power supply rejection ratio		50	>46	>46	>44	dB	PSRR
common mode rejection ratio		50	>45	>45	>43	dB	CMRR
*supply current	no load	5.0	<7.0	<6.7	<6.7	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		1000	>300	>500	>500	kΩ	RIN
non-inverting input capacitance		1.0	<2.0	<2.0	<2.0	pF	CIN
output impedance	DC	0.2	<0.6	<0.3	<0.2	Ω	RO
output voltage range	$R_L = 100\Omega$	+3.1, −2.7	+1.6, −2.5	±2.7	±2.7	V	VO
common mode input range		±2.2	±1.4	±2.0	±2.0	V	CMIR
output current		70	30	50	50	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	$\pm V_{cc}$
differential input voltage	10V
junction temperature	+ 175°C
operating temperature range	
AI/AJ:	− 40°C to + 85°C
A8/AM/AL	− 55°C to + 125°C
storage temperature range	− 65°C to + 150°C
Lead solder duration (+ 300°C)	10 sec

Miscellaneous Ratings

recommended gain range: ±1 to ±10

NOTES:

*	AI, AJ	100% tested at + 25°C, sample at + 85°C.
†	AJ	Sample tested at + 25°C.
†	AI	100% tested at + 25°C.
*	A8	100% tested at + 25°C, − 55°C, + 125°C.
†	A8	100% tested at + 25°C, sample − 55°C, + 125°C.
*	AL, AM	100% wafer probe tested at + 25°C to + 25°C min/max specifications.

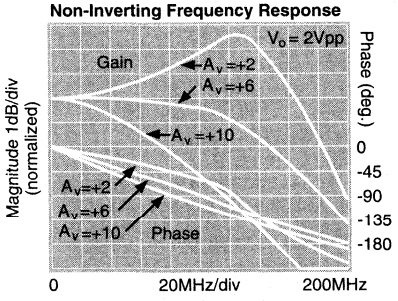
note 1: At − 55°C large signal is $3V_{pp}$

note 2: Gain flatness tests performed from 0.1MHz

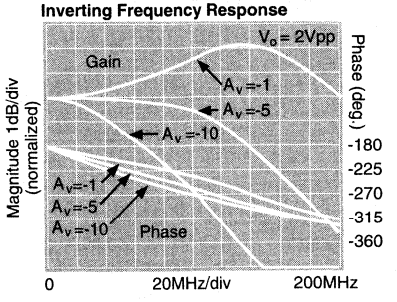
Comlinear reserves the right to change specifications without notice.

Typical Performance Characteristics (T_A =+25° C, A_V =+6, V_{CC} =±5V, R_L =100Ω, R_f =500Ω)

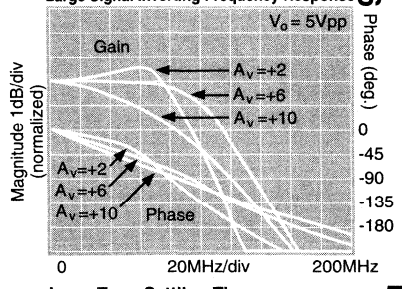
Non-Inverting Frequency Response



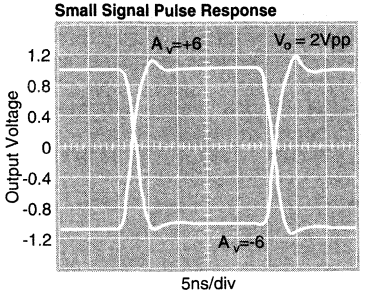
Inverting Frequency Response



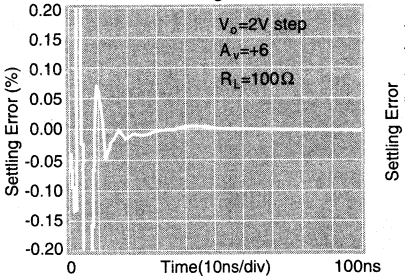
Large Signal Inverting Frequency Response



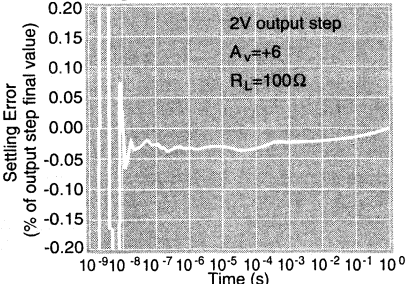
Small Signal Pulse Response



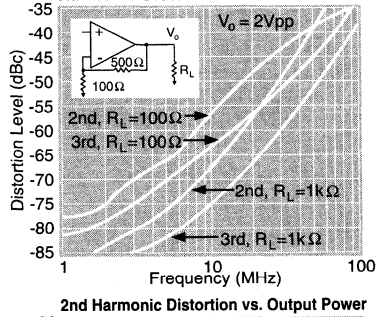
Short-Term Settling Time



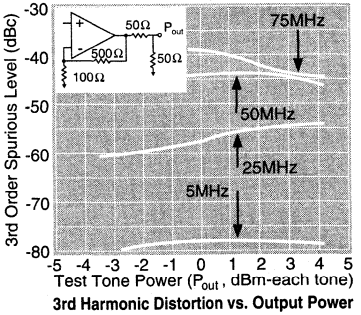
Long-Term Settling Time



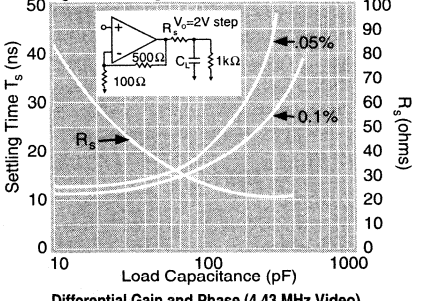
Harmonic Distortion



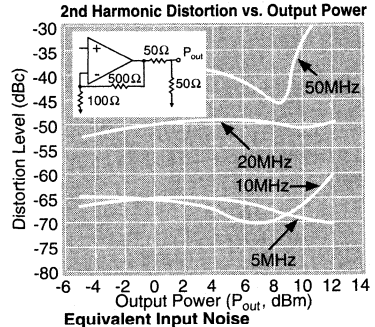
2-Tone, 3rd Order Spurious Levels



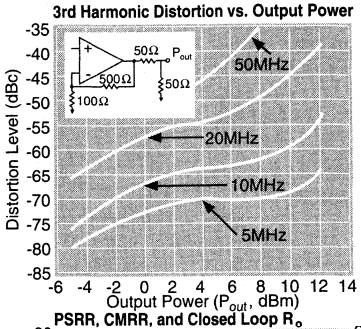
R_s and Settling Time vs. Capacitive Load



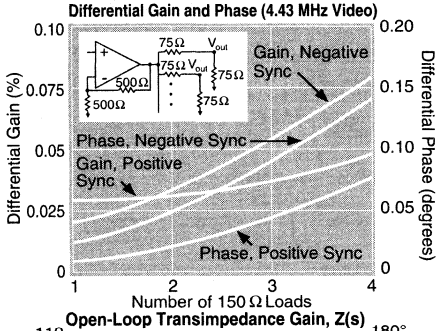
2nd Harmonic Distortion vs. Output Power



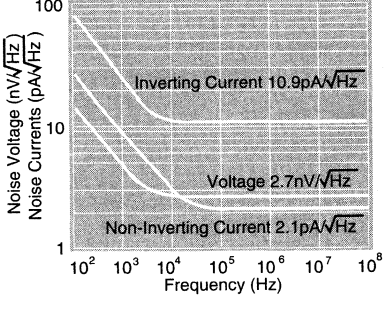
3rd Harmonic Distortion vs. Output Power



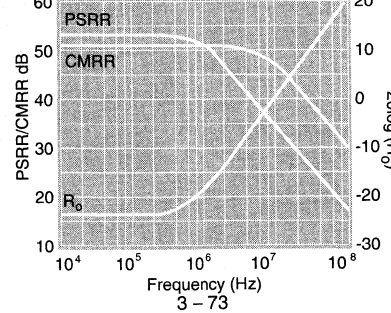
Differential Gain and Phase (4.43 MHz Video)



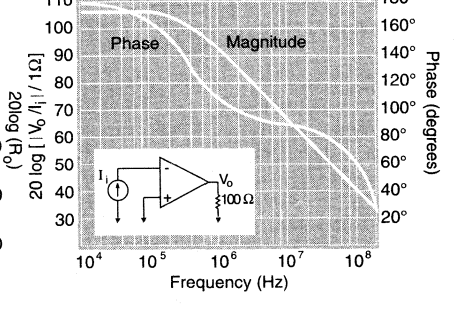
Equivalent Input Noise



PSRR, CMRR, and Closed Loop R_o



Open-Loop Transimpedance Gain, Z(s)



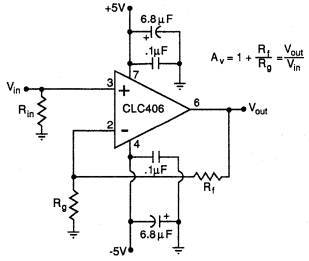


Figure 1: recommended non-inverting gain circuit

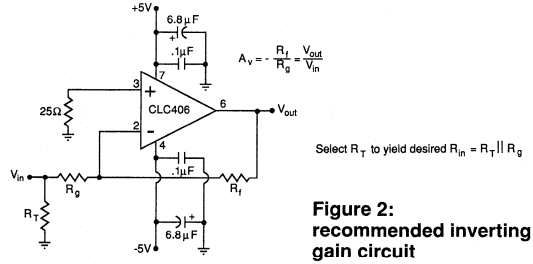


Figure 2: recommended inverting gain circuit

Feedback Resistor

The CLC406 achieves its exceptional AC performance while requiring very low quiescent power by using the current feedback topology and an internal slew rate enhancement circuit. The loop gain and frequency response for a current feedback op amp is predominantly set by the feedback resistor value. The CLC406 is optimized for a gain of +6 to use a 500Ω feedback resistor **(for maximally flat response at a gain of +2, use $R_f = 1k\Omega$).** Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 provides a more detailed discussion of choosing a feedback resistor. A plot found within the CLC415 data sheet entitled "Recommended R_f vs. Gain" is also applicable to the CLC406. The values of R_f found on this plot will optimize the performance of the CLC406 over its ±1 to ±10 gain range. The CLC406, like all current feedback op amps, can be operated at higher than recommended gains with an expected reduction in bandwidth.

Slew Rate and Harmonic Distortion

The current feedback topology yields an inherently high slew rate amplifier. For this reason the CLC406 shows little difference in bandwidth between $2V_{pp}$ and $5V_{pp}$ outputs. The dominant slew rate limiting mechanism is the unity gain buffer used internally from the non-inverting to the inverting inputs. Using a slew enhancement circuit to sense the onset of slew limiting, the buffer stage momentarily increases the quiescent current to handle high slew requirements. Slew rates will decrease when operating the CLC406 at lower non-inverting gains due to the increasing signal swing through the buffer stage which is necessary to maintain a fixed desired output swing. Conversely, slew rates are generally higher and relatively insensitive to gain setting for inverting gain operation. An additional discussion of slew rates can be found in the CLC404 data sheet.

As the output signal swing is increased, the slew enhancement circuit found in the buffer stage acts to suppress harmonic distortions. This is one reason the CLC406 does not exhibit a simple relationship between output power and distortion. For example, the 2-tone, 3rd order spurious plot shows the spurious level to remain nearly constant over test tone power. For this reason the CLC406 does not exhibit an intercept type performance where the relative spurious levels change at twice the rate of the test tone power.

Differential Gain and Phase

Differential gain and phase performance specifications are common to composite video distribution applications. These specifications refer to the change in small signal gain and phase of the color subcarrier frequency (4.43MHz for PAL composite video) as the amplifier output is swept over a range of DC voltages. For this test only, the CLC406 is specified at a gain of +2 while connected to one or more doubly terminated 75Ω loads. Application Note OA-08 provides an additional discussion of differential gain and phase measurements.

Non-inverting Source Impedance

For best operation, the DC source impedance looking out of the non-inverting input should be less than 3kΩ but greater than 20Ω. Parasitic self oscillations may occur in the input transistors if the DC source impedance is out of this range. This impedance also acts as the gain for the non-inverting input bias and noise currents and therefore can become troublesome for high values of DC source impedance. The inverting configuration of Figure 2 shows a 25Ω resistor to ground on the non-inverting input which insures stability but does not provide bias current cancellation. The input bias currents are unrelated for a current feedback amplifier which eliminates the need for source impedance matching to achieve bias current cancellation.

DC Accuracy and Noise

Figure 3 shows an example of the output offset voltage computation. The calculation is developed using typical bias current and offset voltage specifications at 25°C, a gain (Av) of +6 and a non-inverting source impedance (R_s) of 25Ω.

Figure 3: Output Offset Voltage Calculation

Output Offset Voltage $V_o = (\pm I_{bn}R_{in} \pm V_{io})(1 + R_f/R_g) \pm I_{bi}R_f$

$V_o = (\pm 5\mu A(25\Omega) \pm 2mV)(6) \pm 3\mu A(500\Omega) = \pm 14.25mV$

Improved output offset voltage is possible using the composite circuits shown in Application Note OA-07.

The total output spot noise is computed in a similar fashion to the output offset voltage. Using the input spot noise voltage and the two input spot noise currents, the total output spot noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. Application Note OA-12 provides a more detailed discussion of noise calculations for current feedback amplifiers.

Printed Circuit Layout

As with any high speed component, a careful attention to the board layout is necessary for optimum performance. Of particular importance is the careful control of parasitic capacitances on the output pin. As the output impedance plot shows, the closed loop output for the CLC406 eventually becomes inductive as the loop gain rolls off with increasing frequency. Direct capacitive loading on the output pin can quickly lead to peaking in the frequency response, overshoot in the pulse response, ringing or even sustained oscillations. The "Suggested Series R_s vs. C" plot should be used as a starting point when a capacitive load must be driven.

Evaluation boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC406 are available. Further layout suggestions can be found in Application Note OA-15.

Comlinear Corporation

Very Wideband, Low Distortion Monolithic Op Amp

CLC409

APPLICATIONS:

- flash A/D driver
- D/A transimpedance buffer
- wide dynamic range IF amp
- radar/communication receivers
- DDS post-amps
- wideband inverting summer
- line driver

FEATURES (typical):

- 350MHz small signal bandwidth
- −65/−72dBc 2nd/3rd harmonics (20MHz)
- low noise
- 8ns settling to 0.1%
- 1200V/μs slew rate
- 13.5 mA supply current (±5V)
- 70mA output current

DESCRIPTION

The CLC409 is a very wideband, DC coupled monolithic operational amplifier designed specifically for wide dynamic range systems requiring exceptional signal fidelity. Benefitting from Comlinear's current feedback architecture, the CLC409 offers a gain range of ±1 to ±10 while providing stable, oscillation free operation without external compensation, even at unity gain.

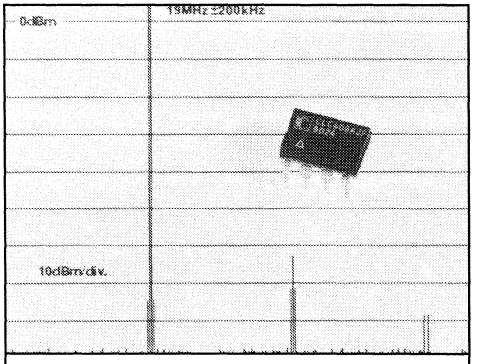
With its 350MHz small signal bandwidth (V_{out}=2V_{pp}), 10-bit distortion levels through 20MHz (R_L=100Ω), 8-bit distortion levels through 60MHz, 2.2nV/$\sqrt{Hz}$ input referred noise and 13.5mA supply current, the CLC409 is the ideal driver or buffer for high speed flash A/D and D/A converters.

Wide dynamic range systems such as radar and communication receivers requiring a wideband amplifier offering exceptional signal purity will find the CLC409's low input referred noise and low harmonic and intermodulation distortion make it an attractive high speed solution.

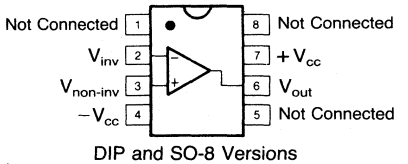
Constructed using an advanced, complimentary biploar process and Comlinear's proven current feedback architecture, the CLC409 is available in several versions to meet a variety of requirements.

CLC409AJP	–40°C to +85°C	8-pin plastic DIP
CLC409AJE	–40°C to +85°C	8-pin plastic SOIC
CLC409AID	–40°C to +85°C	8-pin hermetic side-brazed ceramic DIP
CLC409A8D	–55°C to +125°C	8-pin hermetic side-brazed ceramic DIP, MIL-STD-883, Level B
CLC409ALC	–55°C to +125°C	dice
CLC409AMC	–55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

Contact factory for other packages. DESC SMD number, 5962-92034.

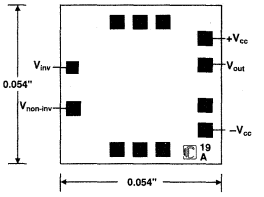


Pinout



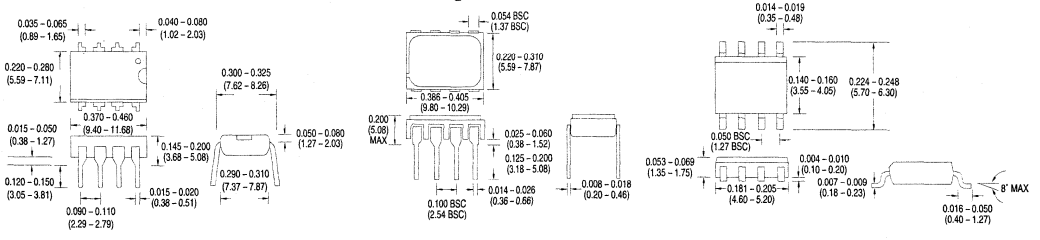
DIP and SO-8 Versions

Chip Topography



Height is 0.014 inches.
NOTE: Backside connected to $-V_{cc}$. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



8-pin plastic DIP **8-pin side-brazed ceramic DIP** **8-pin plastic SOIC**

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics ($A_V = +2$; $V_{CC} = \pm 5V$; $R_L = 100\Omega$; $R_f = 250\Omega$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC409AJ/AI	+25°C	−40°C	+25°C	+ 85°C		
Ambient Temperature	CLC409A8/AL/AM	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN PERFORMANCE							
−3dB bandwidth	$V_{out}<2V_{pp}$	350	>250	>250	>200	MHz	SSBW
	$V_{out}<5V_{pp}$	110	>90	>90	>80	MHz	LSBW
gain flatness[1]	$V_{out}<0.5V_{pp}$						
† peaking	DC to 75MHz	0	<0.4	<0.4	<0.4	dB	GFPL
† peaking	>75MHz	0	<0.8	<0.8	<0.8	dB	GFPH
† rolloff	DC to 125MHz	0.2	<1.0	<1.0	<1.0	dB	GFR1
† rolloff	@ 200MHz	1.0	<2.0	<2.2	<3.0	dB	GFR2
linear phase deviation	DC to 100MHz	0.3	<0.8	<0.8	<1.0	°	LPD
differential gain	150Ω load, 3.58MHz	0.03	<0.07	<0.06	<0.06	%	DG1
	4.43MHz	0.03	<0.07	<0.06	<0.06	%	DG2
differential phase	150Ω load, 3.58MHz	0.01	<0.02	<0.02	<0.02	°	DP1
	4.43MHz	0.01	<0.02	<0.02	<0.02	°	DP2
TIME DOMAIN RESPONSE							
rise and fall time	2V step	1.3	<1.6	<1.6	<1.6	ns	TRS
	5V step	3.5	<4.2	<4.2	<4.6	ns	TRL
settling time to 0.1%	2Vstep	8	<12	<12	<12	ns	TS
overshoot	2V step	5	<15	<18	<18	%	OS
slew rate		1200	>1000	>1000	>1000	V/μs	SR
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	$2V_{pp}$, 5MHz	−86	<−78	<−81	<−81	dBc	HD2L
	† $2V_{pp}$, 20MHz	−65	<−57	<−60	<−60	dBc	HD2
	$2V_{pp}$, 60MHz	−49	<−41	<−44	<−44	dBc	HD2H
3rd harmonic distortion	$2V_{pp}$, 5MHz	−84	<−76	<−76	<−76	dBc	HD3L
	† $2V_{pp}$, 20MHz	−72	<−65	<−65	<−65	dBc	HD3
	$2V_{pp}$, 60MHz	−59	<−52	<−52	<−52	dBc	HD3H
equivalent input noise							
non-inverting voltage	>1MHZ	2.2	<2.8	<2.8	<3.1	nV/√Hz	VN
inverting current	>1MHZ	14.3	<18	<18	<20	pA/√Hz	ICN
non-inverting current	>1MHZ	3.2	<4.0	<4.0	<4.5	pA/√Hz	NCN
total noise floor	>1MHZ	−157	<−155	<−155	<−154	dBm_{1Hz}	SNF
total integrated noise	1MHZ to 150MHz	38	<47	<47	<52	μV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		0.5	<8.5	<4.5	<9.5	mV	VIO
average temperature coefficient		25	<50	—	<50	μV/°C	DVIO
*input bias current	non-inverting	10	<44	<22	<22	μA	IBN
average temperature coefficient		100	<275	—	<125	nA/°C	DIBN
*input bias current	inverting	10	<36	<20	<30	μA	IBI
average temperature coefficient		100	<200	—	<100	nA/°C	DIBI
†power supply rejection ratio		50	>45	>45	>45	dB	PSRR
common mode rejection ratio		50	>45	>45	>45	dB	CMRR
*supply current	no load	13.5	<14.2	<14.2	<14.2	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		1000	>250	>500	>1000	kΩ	RIN
non-inverting input capacitance		1	<2	<2	<2	pF	CIN
output impedance	DC	0.1	<0.3	<0.2	<0.2	Ω	RO
output voltage range	$R_L = 100\Omega$	±3.5	>±3.0	>±3.2	>±3.2	V	VO
common mode input range		±2.2	±1.5	±2.0	±2.0	V	CMIR
output current		70	36	50	50	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but, maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	$\pm V_{cc}$
differential input voltage	10V
junction temperature	+175°C
operating temperature range	
AI/AJ:	−40°C to +85°C
A8/AM/AL:	−55°C to +125°C
storage temperature range	−65°C to +150°C
lead solder duration (+300°C)	10 sec

Miscellaneous Ratings

recommended gain range: ±1 to ±10

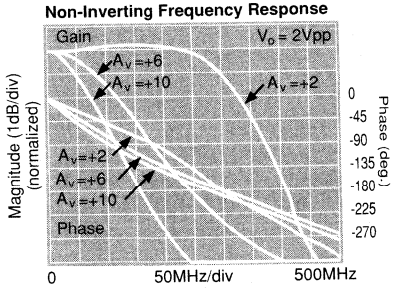
Notes:

*	AI, AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested at +25°C, −55°C, +125°C.
†	A8	100% tested at +25°C, sample at −55°C, +125°C.
*	AL, AM	100% wafer probe tested at +25°C to +25°C min/max specifications.

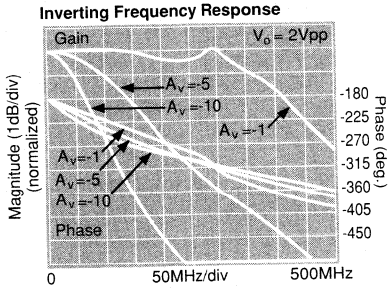
note 1: Gain flatness tests performed from 0.1MHz

Typical Performance Characteristics (T_A =+25°C, A_V =+2, V_{CC}=±5V, R_L=100Ω, R_f=250Ω)

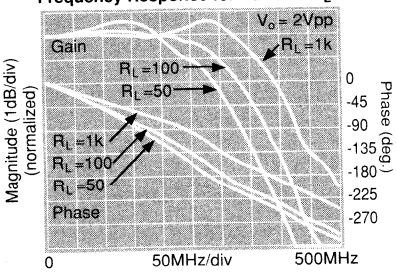
Non-Inverting Frequency Response



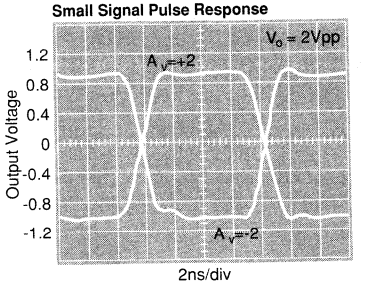
Inverting Frequency Response



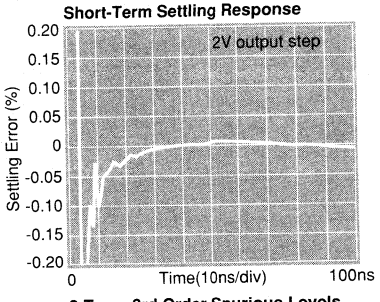
Frequency Response for Various R_Ls



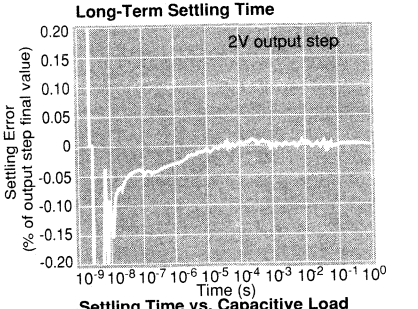
Small Signal Pulse Response



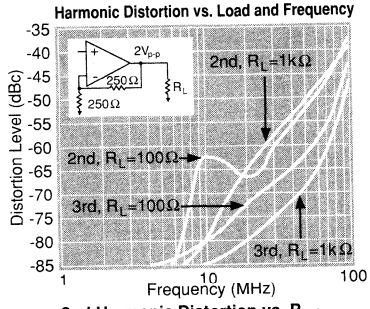
Short-Term Settling Response



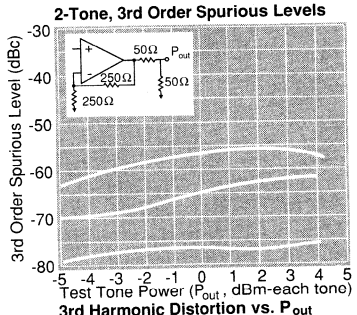
Long-Term Settling Time



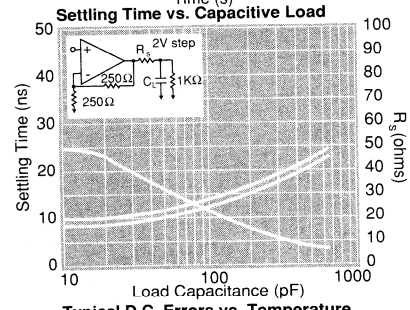
Harmonic Distortion vs. Load and Frequency



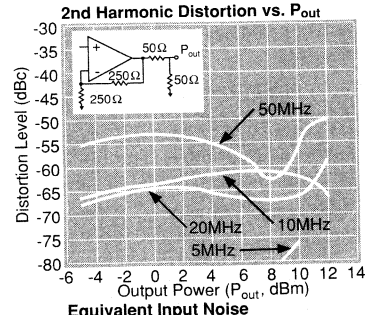
2-Tone, 3rd Order Spurious Levels



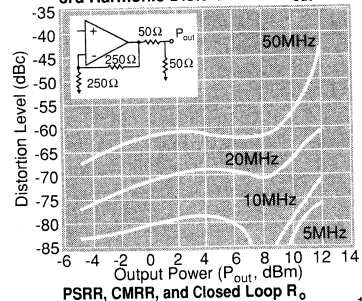
Settling Time vs. Capacitive Load



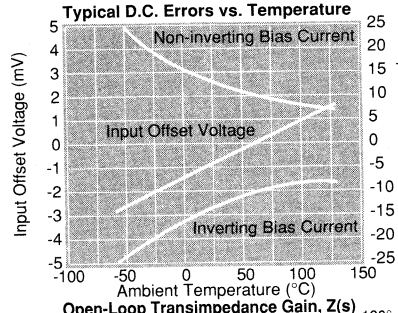
2nd Harmonic Distortion vs. P_{out}



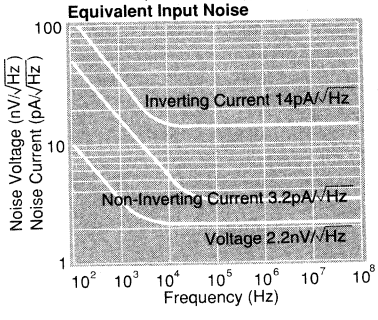
3rd Harmonic Distortion vs. P_{out}



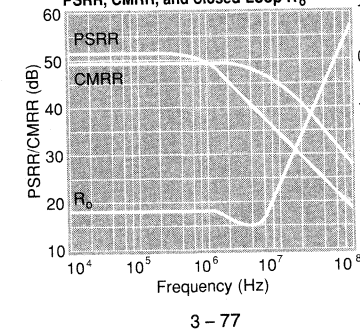
Typical D.C. Errors vs. Temperature



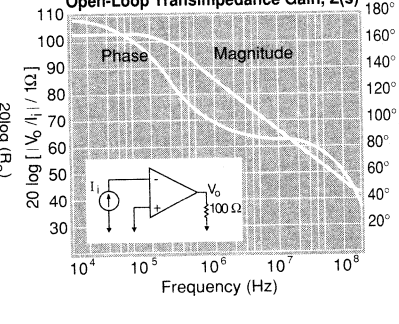
Equivalent Input Noise



PSRR, CMRR, and Closed Loop R_o



Open-Loop Transimpedance Gain, Z(s)



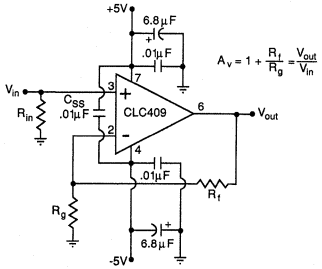


Figure 1: recommended non-inverting gain circuit

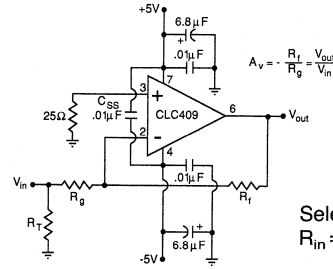


Figure 2: recommended inverting gain circuit

Feedback Resistor

The CLC409 achieves its excellent pulse and distortion performance by using the current feedback topology pioneered by Comlinear Corporation. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The CLC409 is optimized for use with a 250Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 discusses this in detail along with the occasions where a different R_f might be advantageous.

Harmonic Distortion

The CLC409 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high speed flash ADCs, the distortions introduced by the converter will dominate over the low CLC409 distortions shown on the plots on the previous page. The 0.01µF capacitor (C_{ss}) shown across the supplies in Figures 1 and 2 is critical to achieving the lowest 2nd harmonic distortion.

The 2-tone, 3rd-order spurious plot shows a relatively constant difference between the test power level and the spurious level with that difference depending on frequency. The CLC409 does not show an intercept type performance, (where the relative spurious levels change at a 2X rate vs. the test tone powers), due to an internal full power bandwidth enhancement circuit that boosts the performance as the output swing increases while dissipating negligible quiescent power under low output power conditions. This feature enhances the distortion performance and full power bandwidth to match that of much higher quiescent supply current parts.

Figure 3 shows a typical application using the CLC409 to drive an ADC. The series resistor, R_s, between the amplifier output and the ADC input is critical to achieving best system performance. This load capacitance, if applied directly to the output pin, can quickly lead to unacceptable levels of ringing in the pulse response. The plot of R_s and settling time vs. C_L on the previous page is an excellent starting point for setting R_s. The value derived in that plot minimizes the step settling time into a fixed discrete capacitive load. Several additional

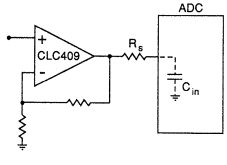


Figure 3: input amplifier to ADC

constraints should be considered, however, in driving the capacitive input of an ADC.

There is an option to increase R_s, bandlimiting at the ADC input for either noise or Nyquist bandlimiting purposes. Increasing R_s too much, however, can induce an unacceptably large input glitch due to switching transients coupling through from the convert signal. Also, C_{in} is oftentimes a voltage dependent capacitance. This input impedance non-linearity will induce distortion terms that will increase as R_s is increased. Only slight adjustments up or down from the recommended R_s value should therefore be attempted in optimizing system performance.

DC Accuracy and Noise

The CLC409 offers an improved offset voltage over the pin compatible CLC400 low gain amplifier. The offset adjustment available on the CLC400 was therefore not included in this part. Figure 4 shows the output offset computation equation for the non-inverting configuration with an example using the typical bias current and offset specifications for $A_v = +2$.

Output Offset

$$V_o = (\pm I_{bn} R_{in} \pm V_{io})(1 + R_f/R_g) \pm I_{bi} R_f$$

Example Computation for $A_v = +2$, $R_f = 250\Omega$, $R_{in} = 25\Omega$:

$V_o = (\pm 10\mu A(25\Omega) \pm 0.5mV)2 \pm 10\mu A(250\Omega) = \pm 3.25mV$

Figure 4: Output DC Offset Calculation

This low output offset voltage is a marked improvement over earlier very high speed amplifiers. Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7.

The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to output offset voltage. Using the input noise voltage and two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12 for a full discussion of noise calculations for current feedback amplifiers.

Printed Circuit Layout

As with any high speed component, a careful attention to the board layout is necessary for optimum performance. Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC409 are available. This additional supply bypassing capacitor, C_{ss}, can easily be added to the board if desired. Further layout suggestions can be found in Application Note OA-15.

Comlinear Corporation

Fast Settling, Video Op Amp with Disable

CLC410

APPLICATIONS:

- video switching and distribution
- analog bus driving (with disable)
- low power "standby" using disable
- fast, precision A/D conversion
- D/A current-to-voltage conversion
- IF processors
- high-speed communications

FEATURES (typical)

- -3dB bandwidth of 200MHz
- 0.05% settling in 12ns
- low power, 160mW (40mW disabled)
- low distortion, -60dBc at 20MHz
- fast disable (200ns)
- differential gain/phase: 0.01%/0.01°
- ±1 to ±8 closed-loop gain range

DESCRIPTION:

The current-feedback CLC410 is a fast-settling, wideband, monolithic op amp with fast disable/enable feature. Designed for low-gain applications ($A_V = \pm 1$ to ± 8), the CLC410 consumes only 160mW of power (180mW max) yet provides a -3dB bandwidth of 200MHz ($A_V = +2$) and 0.05% settling in 12ns (15ns max). Plus, the disable feature provides fast turn-on (100ns) and turn-off (200ns). In addition, the CLC410 offers both high performance and stability without compensation — even at a gain of +1.

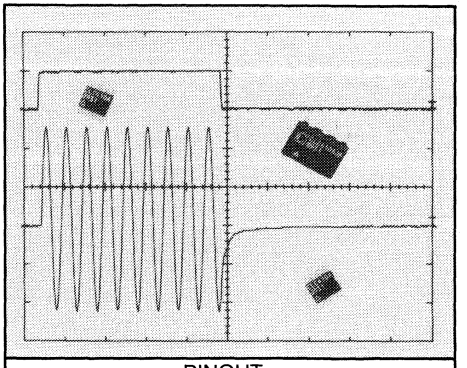
The CLC410 provides a simple, high-performance solution for video switching and distribution applications, especially where analog buses benefit from use of the disable function to "multiplex" signals onto the bus. Differential gain/phase of 0.01%/0.01° provide high fidelity and the 70mA output current offers ample drive capability.

The CLC410's fast settling, low distortion, and high drive capabilities make it an ideal ADC driver. The low 160mW quiescent power consumption and very low 40mW disabled power consumption suggest use where power is critical and/or "system off" power consumption must be minimized.

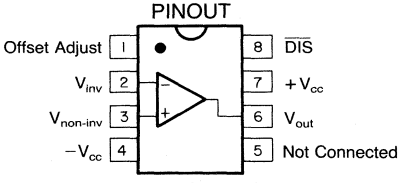
The CLC410 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC410AJP	–40°C to +85°C	8-pin plastic DIP
CLC410AJE	–40°C to +85°C	8-pin plastic SOIC
CLC410AIB	–40°C to +85°C	8-pin hermetic CERDIP
CLC410A8B	–55°C to +125°C	8-pin hermetic CERDIP MIL-STD-883, Level B
CLC410ALC	–55°C to +125°C	dice
CLC410AMC	–55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

Contact factory for other packages. DESC SMD number, 5962-90600.

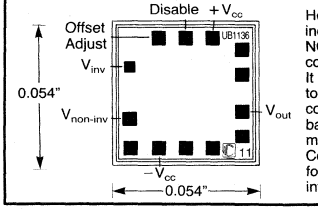


PINOUT



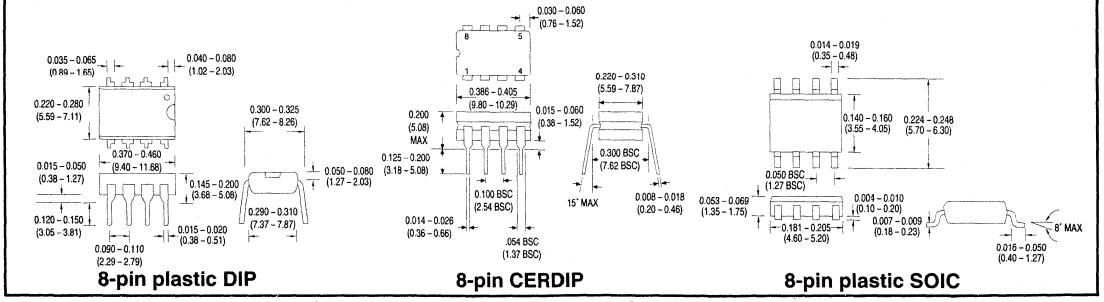
DIP and SO-8 Versions

Chip Topography



Height is 0.014 inches.
NOTE: Backside connected to $-V_{cc}$. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics ($A_V = +2$, $V_{CC} = \pm 5V$, $R_f = 250\Omega$, $R_L = 100\Omega$)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC410A8/AL/AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC410AJ/AI	+25°C	−40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
†-3dB bandwidth	Vout<0.5V_{pp}	200	>150	>150	>120	MHz	SSBW
	Vout<5V_{pp},A_V = +5	50	>35	>35	>35	MHz	LSBW
gain flatness[3]	Vout<0.5V_{pp}						
† peaking	DC to 40MHz	0	<0.4	<0.3	<0.4	dB	GFPL
† peaking	>40MHz	0	<0.7	<0.5	<0.7	dB	GFPH
† rolloff	DC to 75MHz	0.6	<1	<1	<1.3	dB	GFR
linear phase deviation	DC to 75MHz	0.2	<1	<1	<1.2	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	1.6	<2.4	<2.4	<2.4	ns	TRS
	5V step	6.5	<10	<10	<10	ns	TRL
settling time to ±0.1%	2V step	10	<13	<13	<13	ns	TSP
±0.05%	2V step	12	<15	<15	<15	ns	TS
overshoot	0.5V step	0	<15	<10	<10	%	OS
slew rate $A_V = +2$		700	>430	>430	>430	V/μs	SR
$A_V = -2$		1600	—	—	—	V/μs	SR1
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	2V_{pp}, 20MHz	−60	<−40	<−45	<−45	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 20MHz	−60	<−50	<−50	<−50	dBc	HD3
equivalent input noise							
noise floor	>1MHz[1]	−157	<−154	<−154	<−153	dBm(1Hz)	SNF
integrated noise	1MHz to 200MHz[1]	40	<54	<57	<63	μV	INV
differential gain[2]	(see plots)	0.01	0.05	0.04	0.04	%	DG
differential phase[2]	(see plots)	0.01	0.1	0.02	0.02	°	DP
DISABLE/ENABLE PERFORMANCE							
disable time to >50dB attenuation at 10MHz		200	<1000	<1000	<1000	ns	TOFF
enable time		100	<200	<200	<200	ns	TON
$\overline{DIS}$ voltage							
to disable		1.0	0.5	0.5	0.5	V	VDIS
to enable		2.6	2.3	3.2	4.0	V	VEN
$\overline{DIS}$ current (sourced from CLC410, see figure 4)							
to disable		200	250	250	250	μA	IDIS
to enable		80	60	60	60	μA	IEN
off isolation	at 10MHz	59	>55	>55	>55	dB	OSD
STATIC, DC PERFORMANCE							
*input offset voltage		2	<±8.2	<±5.0	<±9.0	mV	VIO
average temperature coefficient		20	<±40	—	<±40	μV/°C	DVIO
*input bias current	non-inverting	10	<±36	<±20	<±20	μA	IBN
average temperature coefficient		100	<±200	—	<±100	nA/°C	DIBN
*input bias current	inverting	10	<±36	<±20	<±30	μA	IBI
average temperature coefficient		50	<±200	—	<±100	nA/°C	DIBI
†power supply rejection ratio		50	>45	>45	>45	dB	PSRR
♠common mode rejection ratio		50	>45	>45	>45	dB	CMRR
*supply current	no load, quiescent	16	<18	<18	<18	mA	ICC
supply current, disabled	no load, quiescent	4	<6	<6	<6	mA	ISD
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	200	>50	>100	>100	kohm	RIN
	capacitance	0.5	<2	<2	<2	pF	CIN
output impedance	at DC	0.1	<0.2	<0.2	<0.2	ohm	RO
output impedance, disabled	resistance, at DC	200	>100	>100	>100	kohm	ROD
	capacitance, at DC	0.5	<2	<2	<2	pF	COD
output voltage range	no load	±3.5	>±3	>±3.2	>±3.2	V	VO
common mode input range for	rated performance	±2.1	>±1.2	>±2	>±2	V	CMIR
output current	−40°C to +85°C	±70	>±35	>±50	>±50	mA	IO
	−55°C to +125°C	±70	>±30	>±50	>±50	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, however, maximum reliability is obtained if I_{out} does not exceed...	70mA
common mode input voltage	$\pm V_{cc}$
differential input voltage	5V
disable input voltage (pin 8)	$+V_{cc}$, −1V
applied output voltage when disabled	$\pm V_{cc}$
junction temperature	+175°C
operating temperature range	
AI/AJ:	−40°C to +85°C
A8/AL/AM:	−55°C to +125°C
storage temperature range	−65°C to +150°C
lead solder duration (+300°C)	10 sec

Miscellaneous Ratings

recommended gain range	±1 to ±8

Notes:

*	AI, AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested at +25°C, −55°C, +125°C.
†	A8	100% tested at +25°C, sample at −55°C, +125°C.
*	AL, AM	100% wafer probe tested at +25°C to +25°C min/max specifications.
♠	SMD	Sample tested at +25°C, −55°C, +125°C.

note 1: Noise tests are performed from 5MHz to 200MHz.

note 2: Differential gain and phase measured at: A_v = +2, R_f = 250Ω, R_L = 150Ω $1V_{pp}$ equivalent video signal, 0-100 IRE, 40IRE$_{pp}$, 3.58 MHz, 0IRE = 0 volts, at 75Ω load. See text.

note 3: Gain flatness tests performed from 0.1MHz.

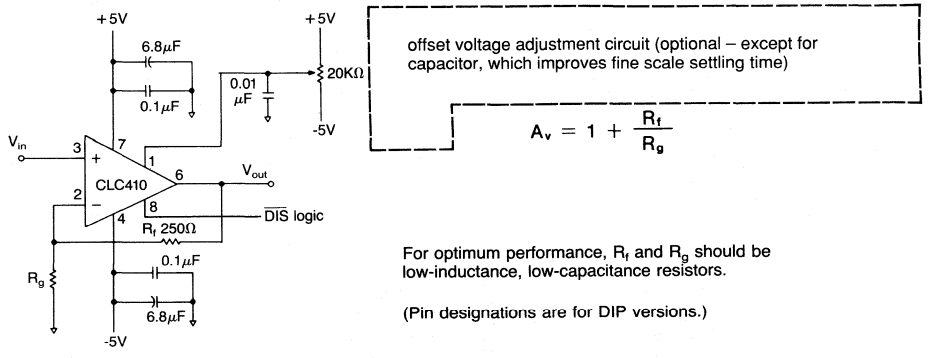


Figure 1: recommended non-inverting gain circuit

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

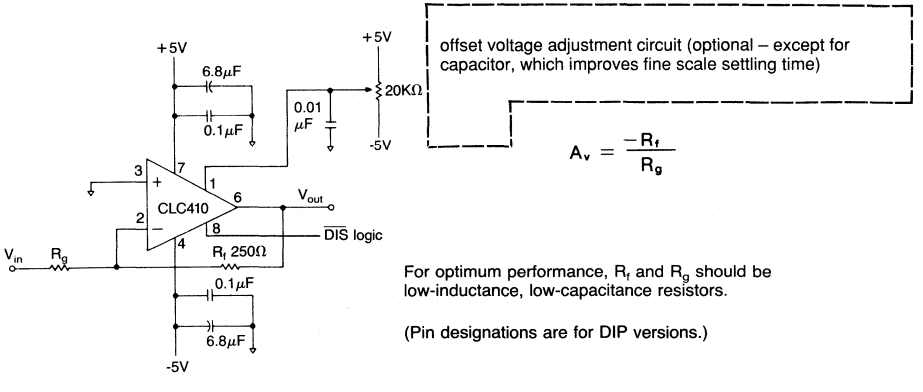


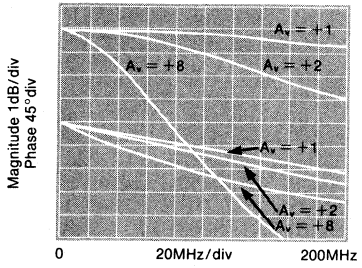
Figure 2: recommended inverting gain circuit

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

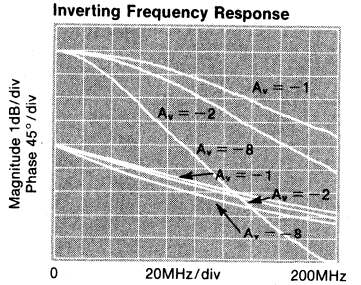
(Pin designations are for DIP versions.)

Typical Performance Characteristics ($T_A = 25°C$, $A_V = +2$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$)

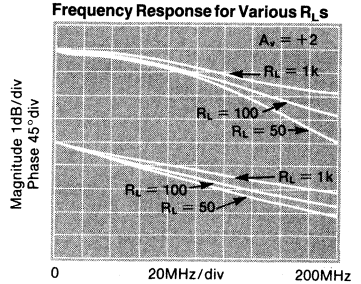
Non-Inverting Frequency Response



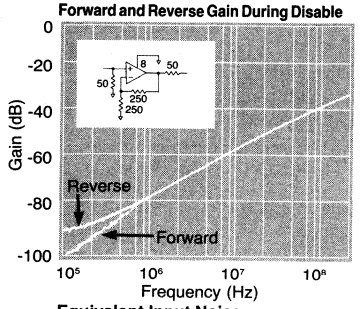
Inverting Frequency Response



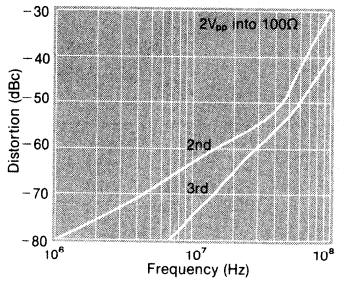
Frequency Response for Various R_Ls



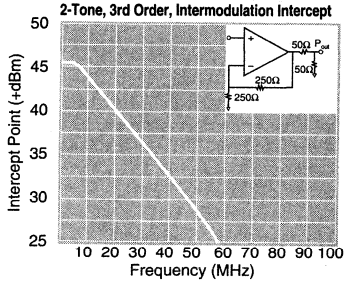
Forward and Reverse Gain During Disable



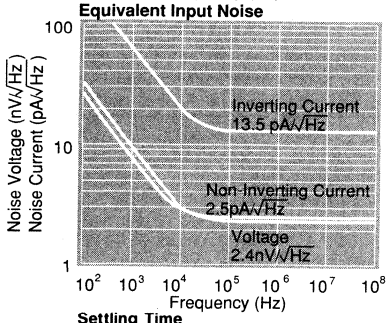
2nd and 3rd Harmonic Distortion



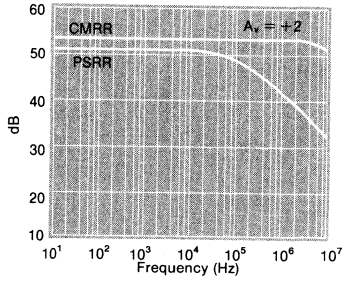
2-Tone, 3rd Order, Intermodulation Intercept



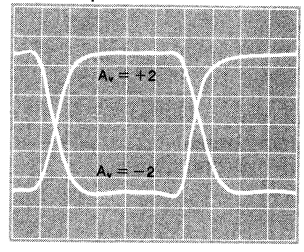
Equivalent Input Noise



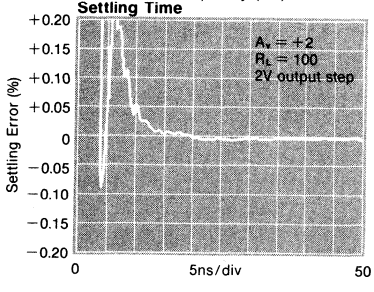
CMRR and PSRR



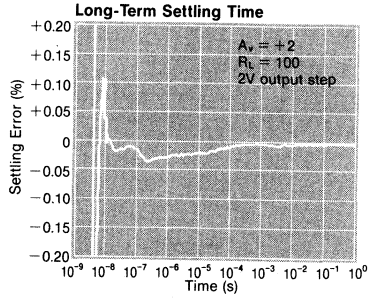
Pulse Response



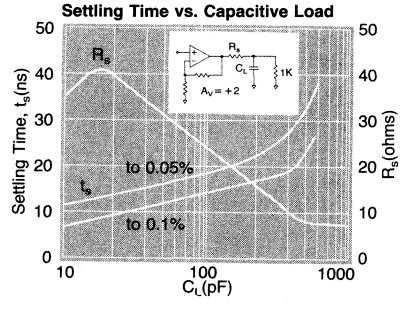
Settling Time



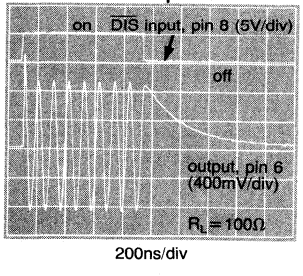
Long-Term Settling Time



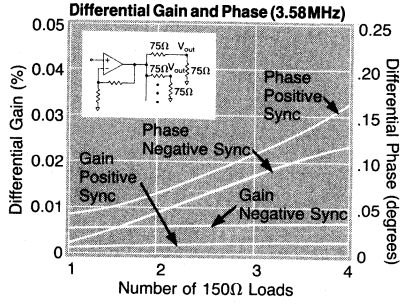
Settling Time vs. Capacitive Load



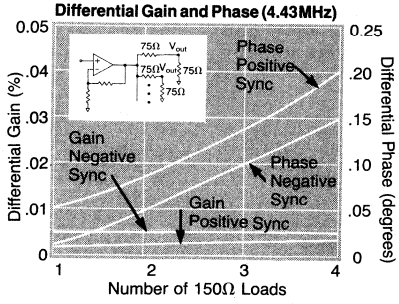
Enable/Disable Response



Differential Gain and Phase (3.58MHz)



Differential Gain and Phase (4.43MHz)



Enable/Disable Operation

The CLC410 has an enable/disable feature that is useful for conserving power and for multiplexing the outputs of several amplifiers onto an analog bus (figure 3A). Disabling an amplifier while not in use reduces power supply current and the output and inverting input pins become a high impedance.

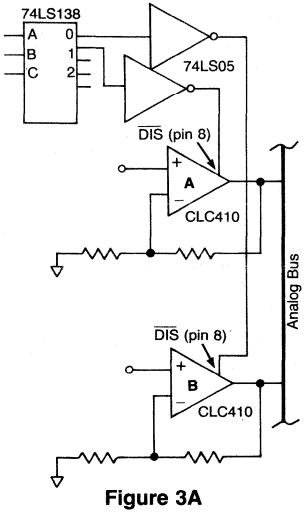


Figure 3A

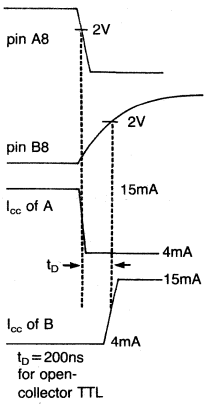


Figure 3B

Pin 8, the $\overline{DIS}$ pin, can be driven from either open-collector TTL or from 5V CMOS. A logic low disables the amplifier and an internal 15KΩ pull-up resistor ensures that the amplifier is enabled if pin 8 is not connected (figure 4). Both TTL and 5V CMOS logic are guaranteed to drive a high enough high-level output voltage (V_{OH}) to ensure that the CLC410 is enabled. Whichever type used, "break-before-make" operation should be established when outputs of several amplifiers are connected together. This is important for avoiding large, transient currents flowing between amplifiers when two or more are simultaneously enabled. Typically, proper operation is ensured if all the amplifiers are driven from the same decoder integrated circuit because logic output rise times tend to be longer than fall times. As a result, the amplifier being disabled will reach the 2V threshold sooner than the amplifier being enabled (see t_D of figure 3B timing diagram).

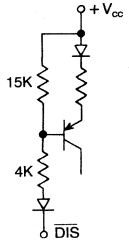


Figure 4: equivalent of $\overline{DIS}$ input

During disable, supply current drops to approximately 4mA and the inverting input and output pin impedances become 200KΩ || 0.5pF each. The total impedance that a disabled amplifier and its associated feedback network presents to the analog bus is determined from figure 5. For example, at a non-inverting gain of 1, the output impedance at video frequencies is 100KΩ || 1pF since the 250Ω feedback resistor is a negligible impedance. Similarly, output impedance is 500Ω || 0.5pF at a non-inverting gain of 2 (with $R_F = R_G = 250\Omega$).

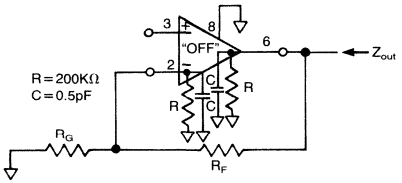


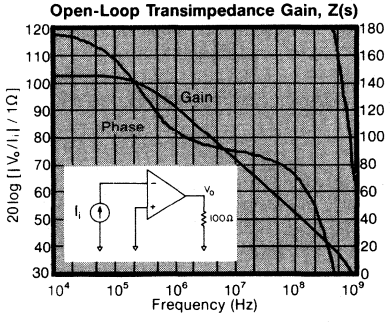
Figure 5

Differential Gain and Phase

Plots on the preceding page illustrate the differential gain and phase performance of the CLC410 at both 3.58 and 4.43MHz. Application Note OA-08 presents a measurement technique for measuring the very low differential gain and phase of the CLC410. Observe that the gain and phase errors remain low even as the output loading increases, making the device attractive for driving multiple video outputs.

Understanding the Loop Gain

The CLC410 is a current-feedback op amp. Referring to the equivalent circuit of figure 6, any current flowing in the inverting input is amplified to a voltage at the output through the transimpedance gain shown below. This Z(s) is analogous to the open-loop gain of a voltage feedback amplifier.



Developing the non-inverting frequency response for the topology of Figure 3 yields:

$$\frac{V_o}{V_i} = \frac{1 + R_f / R_g}{1 - 1 / LG} \qquad \text{eq. (1)}$$

where LG is the loop gain defined by,

$$LG = \frac{Z(s)}{R_f} \times \frac{1}{1 + Z_i / (R_f \| R_g)} \qquad \text{eq. (2)}$$

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the LG expression, eq. 2. For an idealized treatment, set $Z_i = 0$ which results in a very simple $LG = Z(s)/R_f$ (Derivation of the transfer function for the case where $Z_i = 0$ is given in

Application Note AN300-1.) Using the Z(s) (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended $R_f = 250\Omega$, yields a large loop gain at DC. As a result, equation 1 shows that the closed-loop gain at DC is very close to $(1 + R_f/R_g)$.

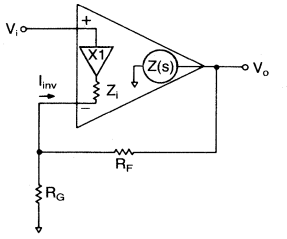


Figure 6: current feedback topology

At higher frequencies, the roll-off of Z(s) determines the closed-loop frequency response which, ideally, is dependent only on R_f. **The specifications reported on the previous pages are therefore valid only for the specified $R_f = 250\Omega$.** Increasing R_f from 250Ω will decrease the loop gain and bandwidth, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing R_f will hold the frequency response constant while the closed-loop gain can be adjusted using R_g.

The CLC410 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC410, $Z_i \cong 50\Omega$ leading to a drop in loop gain and bandwidth at high gain settings, as given by equation 2. The second term in equation 2 accounts for the division in feedback current that occurs between Z_i and $R_f \| R_g$ at the inverting node of the CLC410. This decrease in bandwidth can be circumvented as described in "Increasing Bandwidth at High Gains." Also see "Current Feedback Amplifiers" in the Comlinear Databook for a thorough discusion of current feedback op amps.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting R_f and R_g to make up for the losses in loop gain that occur at these high gain settings due to current division at the inverting input. An approximate relationship may be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, $R_f = 250\Omega$ and $R_g = 250\Omega$). For the CLC410 this gives,

$$R_f = 350 - 50A_v \text{ and } R_g = \frac{350 - 50A_v}{A_v - 1} \quad \text{eq. (3)}$$

where A_v is the non-inverting gain. Note that with $A_v = +2$ we get the specified $R_f = 250\Omega$, while at higher gains, a lower value gives stable performance with improved bandwidth.

DC Accuracy and Noise

Since the two inputs for the CLC410 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In equation 4, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin resistance.

$$\text{Output Offset } V_o = \pm IBN \times R_s(1 + R_f/R_g) \pm VIO(1 + R_f/R_g) \pm IBI \times R_f \quad \text{eq. (4)}$$

An important observation is that for fixed R_f, offsets as referred to the input improve as the gain is increased (divide all terms by $1 + R_f/R_g$). A similar result is obtained for noise where noise figure improves as gain increases.

The input noise plot shown in the CLC400 datasheet applies equally as well to the CLC410.

Capacitive Feedback

Capacitive feedback should not be used with the CLC410 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC410.

Offset Adjustment Pin

Pin 1 can be connected to a potentiometer as shown in Fig. 1 and used to adjust the input offset of the CLC410. Full range adjustment of ± 5V on pin 1 will yield a ± 10mV input offset adjustment range. Pin 1 should always be bypassed to ground with a ceramic capacitor located close to the package for best settling performance.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC410 are available.

Comlinear Corporation

High-Speed Video Op Amp with Disable

CLC411

APPLICATIONS:

- HDTV amplifier
- video line driver
- high-speed analog bus driver
- video signal multiplexer
- DAC output buffer

FEATURES (typical):

- 200MHz small signal bandwidth ($1V_{pp}$)
- ±0.05dB gain flatness to 30MHz
- 0.02%, 0.03° differential gain, phase
- 2300V/µs slew rate
- 10ns disable to high-impedance output
- 70mA continuous output current
- ±4.5V output swing into 100Ω load
- ±4.0V input voltage range

DESCRIPTION

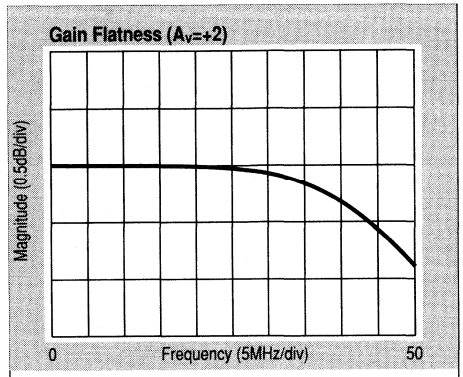
The CLC411 combines a state-of-the-art complementary bipolar process with Comlinear's patented current-feedback architecture to provide a very high-speed op amp operating from ±15V supplies. Drawing only 11mA quiescent current, the CLC411 provides a 200MHz small signal bandwidth and a 2300V/µs slew rate while delivering a continuous 70mA current output with ±4.5V output swing. The CLC411's high-speed performance includes a 15ns settling time to 0.1% (2V step) and a 2.3ns rise and fall time (6V step).

The CLC411 is designed to meet the requirements of professional broadcast video systems including composite video and high definition television. The CLC411 exceeds the HDTV standard for gain flatness to 30MHz with it's ±0.05dB flat frequency response and exceeds composite video standards with its very low differential gain and phase errors of 0.02%, 0.03°. The CLC411 is the op amp of choice for all video systems requiring upward compatibility from NTSC and PAL to HDTV.

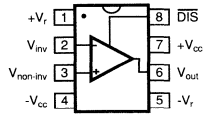
The CLC411 features a very fast disable/enable (10ns/ 55ns) allowing the multiplexing of high-speed signals onto an analog bus through the common output connections of multiple CLC411's. Using the same signal source to drive disable/enable pins is easy since "break-before-make" is guaranteed.

The CLC411 is available in several versions.

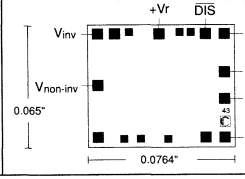
CLC411AJP	-40°C to +85°C	8-pin plastic DIP
CLC411AJE	-40°C to +85°C	8-pin plastic SOIC
CLC411AIB	-40°C to +85°C	8-pin hermetic CerDIP
CLC411A8B	-55°C to +125°C	8-pin hermetic CerDIP, MIL-STD-883
CLC411A8L-2	-55°C to +125°C	20-pin hermetic LCC, MIL-STD-883
CLC411ALC	-55°C to +125°C	dice
CLC411AMC	-55°C to +125°C	dice, MIL-STD-883, Level B



Pinout

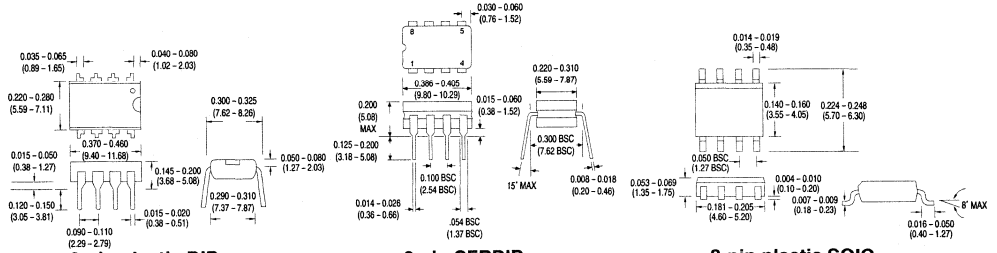


Chip Topography



Thickness is 0.014". Note: Backside connected to -Vcc. It is not necessary to electrically connect the backside to the negative power supply. Contact factory for more information.

Package Dimensions



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DS411.0 (introductory)
January 1993

CLC411 Electrical Characteristics (A_V = +2; V_{cc} = ±15V; R_L = 100Ω; R_f = 301Ω, unless noted)

PARAMETERS	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC411 AJ/AI	+25°C	-40°C	+25°C	+85°C		
Ambient Temperature	CLC411 A8/AM/AL	+25°C	-55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
†-3dB bandwidth	V_{out} < 1V_{pp}	200	150	150	110	MHz	SSBW
	V_{out} < 6V_{pp}	75	50	50	40	MHz	LSBW
gain flatness	V_{out} < 1V_{pp}						
† peaking	DC to 30MHz	0.05	TBD	TBD	TBD	dB	GFPL
† rolloff	DC to 30MHz	0.05	TBD	TBD	TBD	dB	GFRL
† peaking	DC to 200MHz	0.1	0.6	0.5	0.6	dB	GFPH
† rolloff	DC to 60MHz	0.2	0.5	0.4	0.5	dB	GFRH
linear phase deviation	DC to 60MHz	0.3	1.0	1.0	1.0	°	LPD
differential gain	4.43MHz, R_L=150Ω	0.02	TBD	TBD	TBD	%	DG
differential phase	4.43MHz, R_L=150Ω	0.03	TBD	TBD	TBD	°	DP
TIME DOMAIN RESPONSE							
rise and fall time	6V step	2.3	TBD	TBD	TBD	ns	TR
settling time to 0.1%	2V step	15	23	18	23	ns	TS
overshoot	2V step	5	15	10	15	%	OS
slew rate	6V step	2300	TBD	TBD	TBD	V/µs	SR
DISTORTION AND NOISE RESPONSE (note 1)							
†2ND harmonic distortion	2V_{pp}, 20MHz	-48	TBD	TBD	TBD	dBc	HD2
†3RD harmonic distortion	2V_{pp}, 20MHz	-52	TBD	TBD	TBD	dBc	HD3
equivalent noise input							
voltage	>1MHz	2.5	TBD	TBD	TBD	nV/√Hz	VN
inverting current	>1MHz	12.9	TBD	TBD	TBD	pA/√Hz	ICI
non-inverting current	>1MHz	6.3	TBD	TBD	TBD	pA/√Hz	ICN
noise floor	>1MHz	-157	TBD	TBD	TBD	dBm_{1Hz}	SNF
integrated noise	1MHz to 200MHz	45	TBD	TBD	TBD	µV	INV
STATIC DC PERFORMANCE							
*input offset voltage		±2	±13	±9.0	±14	mV	VIO
average temperature coefficient		+30	±50	—	±50	µV/°C	DVIO
*input bias current	non-inverting	12	65	30	±20	µA	IBN
average temperature coefficient		±200	±400	—	±250	nA/°C	DIBN
*input bias current	inverting	±12	±40	±30	±30	µA	IBI
average temperature coefficient		±50	±200	—	±150	nA/°C	DIBI
†power supply rejection ratio		56	48	50	48	dB	PSRR
♠common mode rejection ratio		52	44	46	44	dB	CMRR
*supply current	no load	11	14	12	12	mA	ICC
supply current	disabled	2.5	4.5	3.5	4.5	mA	ICCD
DISABLE/ENABLE PERFORMANCE (note 2)							
disable time	to >50dB attenuation @10MHz	10	30	30	60	ns	TOFF
enable time		55	TBD	TBD	TBD	ns	TON
DIS voltage	pin 8						
to disable		4.5	<3.0	<3.0	<3.0	V	VDIS
to enable		5.5	>7.0	>6.5	>6.5	V	VEN
off isolation	at 10MHz	59	55	55	55	dB	OSD
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		1000	250	750	1000	kΩ	RIN
non-inverting input capacitance		2.0	3.0	3.0	3.0	pF	CIN
output voltage range	no load	±6.0	TBD	±4.5	TBD	V	VO
output voltage range	R_L=100Ω	±4.5	TBD	±4.0	TBD	V	VOL
common mode input range		±4.0	TBD	±3.5	TBD	V	CMIR
output current		70	30	50	40	mA	IO

Absolute Maximum Ratings

V_{cc}	±18V
I_{out}	125mA
common-mode input voltage	±V_{cc}
differential input voltage	±15V
maximum junction temperature	+175°C
operating temperature range	
AJ/AI	-40°C to +85°C
A8/AM/AL:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

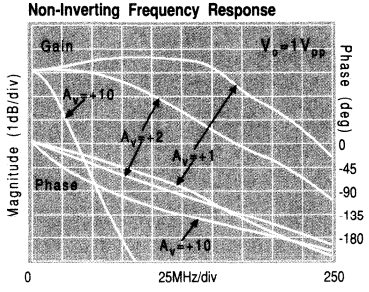
Recommended gain range ±1 to ±10V/V

Notes:

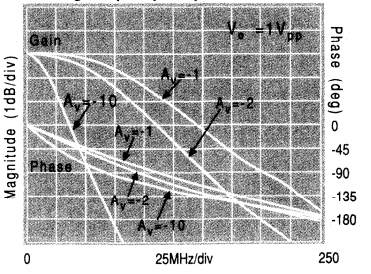
* AJ,AI : 100% tested at +25°C, sample at +85°C.
† AJ : Sample tested at +25°C.
† AI : 100% tested at +25°C.
* A8 : 100% tested at +25°C, -55°C, +125°C.
† A8 : 100% tested at +25°C, sample at -55°C, +125°C
* AL, AM : 100% wafer probed +25°C to +25°C min/max specs.
♠ SMD : Sample tested at +25°C, -55°C and +125°C.
note 1) : Specifications guaranteed using 0.01µF bypass capacitors on pins 1 & 5.
note 2) : Break before make is guaranteed.

CLC411 Typical Performance (T_A=+25°C, A_V=+2, V_{CC}=±15V, R_L=100Ω, R_f=301Ω, unless noted)

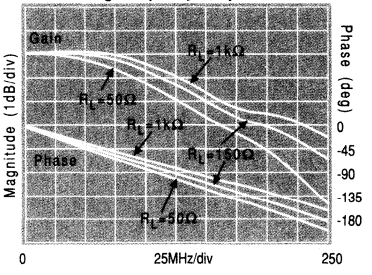
Non-Inverting Frequency Response



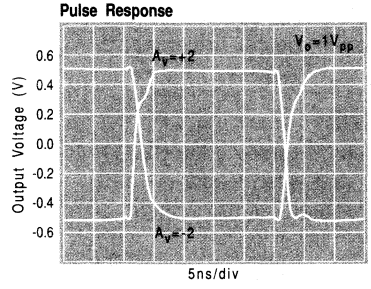
Inverting Frequency Response



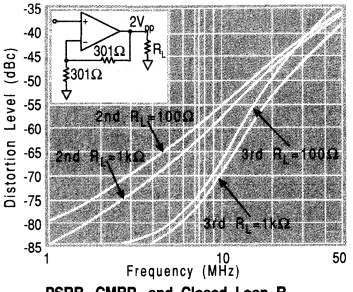
Non-Inverting Frequency Response vs. Load



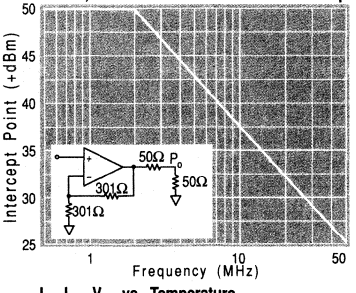
Pulse Response



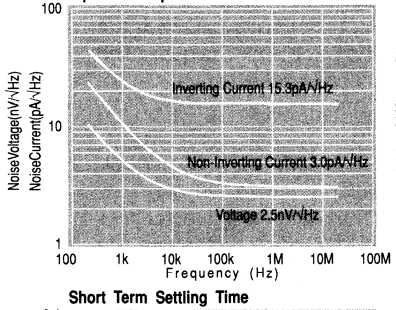
2nd and 3rd Harmonic Distortion



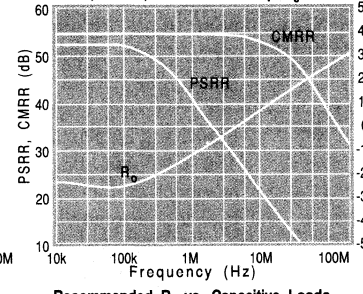
2-Tone, 3rd Order Intermodulation Intercept



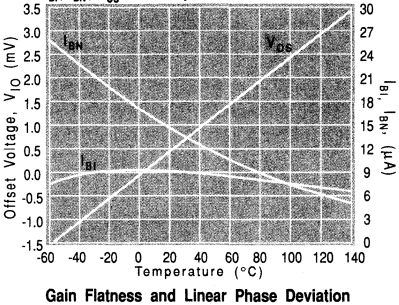
Equivalent Input Noise



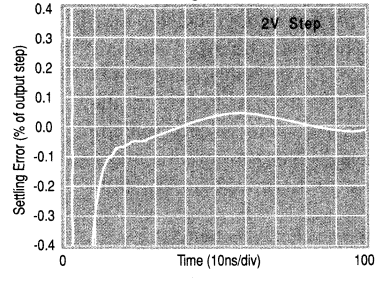
PSRR, CMRR, and Closed Loop R_o



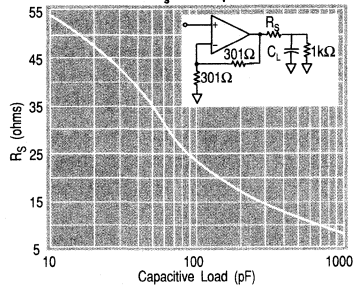
I_{BI}, I_{BN}, V_{OS} vs. Temperature



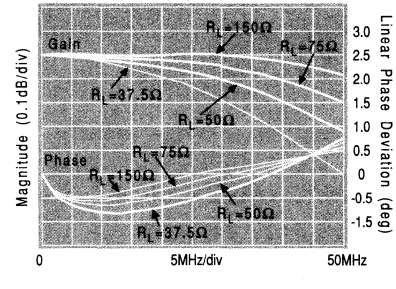
Short Term Settling Time



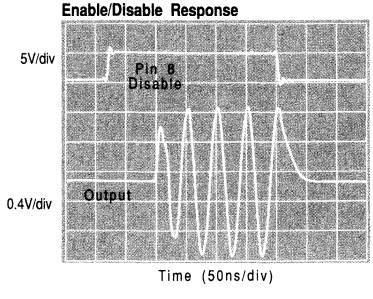
Recommended R_s vs. Capacitive Loads



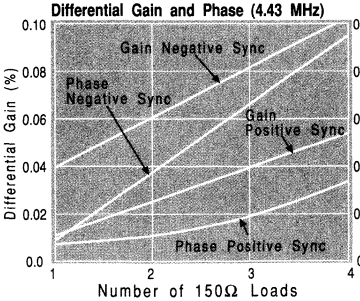
Gain Flatness and Linear Phase Deviation



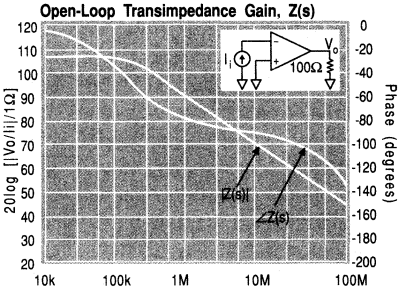
Enable/Disable Response



Differential Gain and Phase (4.43 MHz)



Open-Loop Transimpedance Gain, Z(s)



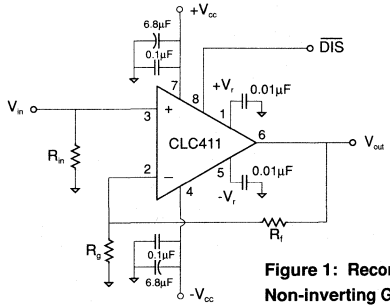


Figure 1: Recommended Non-inverting Gain Circuit

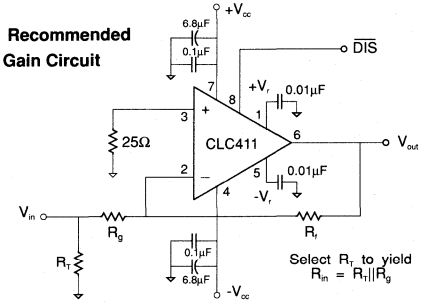


Figure 2: Recommended Inverting Gain Circuit

Description

The CLC411 is a high-speed current-feedback operational amplifier which operates from ±15V power supplies. The external supplies ($\pm V_{CC}$) are regulated to lower voltages internally. The amplifier itself sees approximately ±6.5V rails. Thus the device yields performance comparable to Comlinear's ±5V devices, but with higher supply voltages. There is no degradation in rated specifications when the CLC411 is operated from ±12V. A slight reduction in bandwidth will be observed with ±10V supplies. Operation at less than ±10V is not recommended.

A block diagram of the amplifier and regulator topology is shown in Figure 3, "CLC411 Equivalent Circuit." The regulators derive their reference voltage from an internal floating zener voltage source. External control of the zener reference pins can be used to level-shift amplifier operation which is discussed in detail in the section

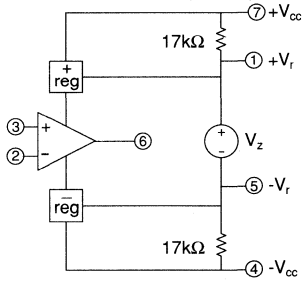


Figure 3: CLC411 Equivalent Circuit

entitled "Extending Input/Output Range with V_r."

Power Supply Decoupling

There are four pins associated with the power supplies. The V_{CC} pins (4,7) are the external supply voltages. The V_r pins (5,1) are connected to internal reference nodes. Figures 1 and 2 , "Recommended Non-inverting Gain Circuit" and "Recommended Inverting Gain Circuit" show the recommended supply decoupling scheme with four ceramic and two electrolytic capacitors. The ceramic capacitors must be placed immediately adjacent to the device pins and connected directly to a good low-inductance ground plane. Bypassing the V_r pins will reduce high frequency noise (>10MHz) in the amplifier. If this noise is not a concern these capacitors may be eliminated.

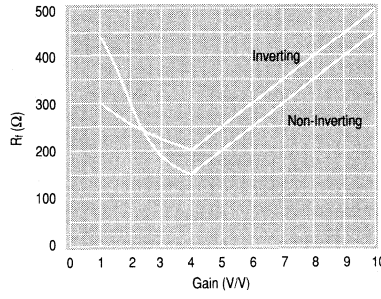
Differential Gain and Phase

The differential gain and phase errors of the CLC411 driving one doubly-terminated video load (R_L=150Ω) are specified and guaranteed in the "Electrical Characteristics" table. The "Typical Performance" plot, "Differential Gain and Phase (4.43MHz)" shows the differential gain and phase performance of the CLC411 when driving from one to four video loads. Application note OA-08, "Differential Gain and Phase for Composite Video Systems," describes in detail the techniques used to measure differential gain and phase.

Feedback Resistor

The loop gain and frequency response for a current-feedback operational amplifier is determined largely by the feedback resistor, R_f. The electrical characteristics and typical performance plots contained within the datasheet, unless otherwise stated, specify an R_f of 301Ω, a gain of +2V/V and operation with ±15V power supplies. The frequency response at different gain settings and supply voltages can be optimized by selecting a different value of R_f. Generally, lowering R_f will peak the frequency response and extend the bandwidth while increasing its value will roll off the response. For unity-gain voltage follower circuits, a non-zero R_f must be used with current-feedback operational

Figure4: Recommended R_f vs. Gain



amplifiers such as the CLC411.

Application note OA-13, "Current-Feedback Loop-Gain Analysis and Performance Enhancements," explains the ramifications of R_f and how to use it to tailor the desired frequency response with respect to gain. The equations found in the application note should be considered as a starting point for the selection of R_f. The equations do not factor in the effects of parasitic capacitance found on the inverting input, the output nor across the feedback resistor. Equations in OA-13 require values for R_f (301Ω), Av (+2) and R_i (inverting input resistance, 50Ω). Combining these values yields a Z_t* (optimum feedback transimpedance) of 400Ω. Figure 4 entitled "Recommended R_f vs. Gain" will enable the selection of the feedback resistor that provides a maximally flat frequency response for the CLC411 over its gain range. The linear portion of the two curves (i.e. A_V>4) results from the limitation on R_g (i.e. $R_g \geq 50\Omega$).

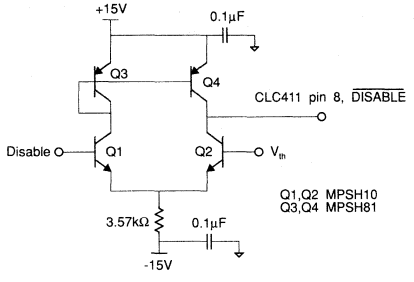


Figure 5A: Disable Interface

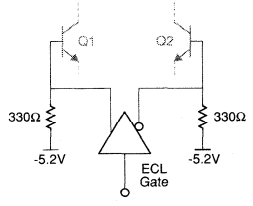


Figure 5B: Differential ECL Interface

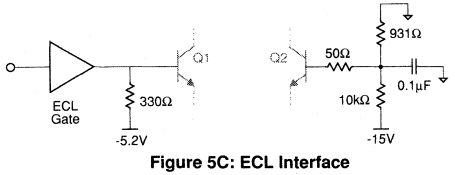


Figure 5C: ECL Interface

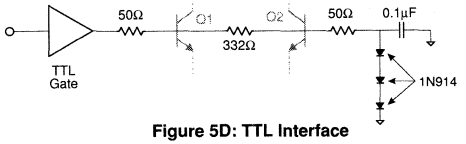


Figure 5D: TTL Interface

Enable/Disable Operation

The disable feature allows the outputs of several CLC411 devices to be connected onto a common analog bus forming a high-speed analog multiplexer. When disabled, the output and inverting inputs of the CLC411 become high impedances. The disable pin has an internal pull-up resistor which is pulled-up to an internal voltage, not to the external supply. The CLC411 is enabled when pin 8 is left open or pulled-up to ≥+7V and disabled when grounded or pulled below +3V. CMOS logic devices are necessary to drive the disable pin. For example, CMOS logic with $V_{DD} \geq +7V$ will guarantee proper operation over temperature. TTL voltage levels are inadequate for controlling the disable feature.

For faster enable/disable operation than 15V CMOS logic devices will allow, the circuit of Figure 5 is recommended. A fast four-transistor comparator, Figure 5A, interfaces between the CLC411 DISABLE pin and several standard logic families. This circuit has a differential input between the bases of Q1 and Q2. As such it may be driven directly from differential ECL logic, as in shown in Figure 5B. Single-ended logic families may also be used by establishing an appropriate threshold voltage on the V_{th} input, the base of Q2. Figures 5C and 5D illustrate a single-ended ECL and TTL interface respectively. The Disable input, the base of Q1, is driven above and below the threshold, V_{th}.

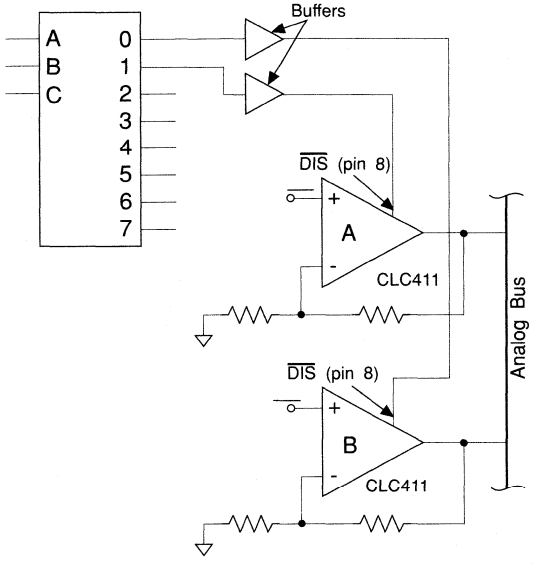


Figure 6: General Multiplexing Circuit

Fastest switching speeds result when the differential voltage between the bases of Q1 and Q2 is kept to less than one volt. Single-ended ECL, Figure 5C, maintains this desired maximum differential input voltage. TTL and CMOS have higher V_{high} to V_{low} excursions. The

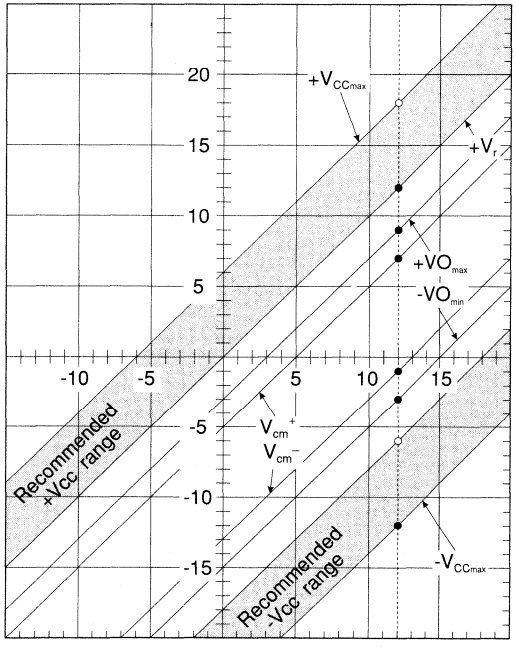
circuit of figure 5D will ensure the voltage applied between the bases of Q1 and Q2 does not cause excessive switching delays in the CLC411. Under the above proscribed four-transistor interface, all variations were evaluated with approximately 1ns rise and fall times which produced switching speeds equivalent to the rated disable/enable switching times found in the "CLC411 Electrical Characteristics" table.

A general multiplexer configuration using several CLC411s is illustrated in figure 6, where a typical 8-to-1 digital mux is used to control the switching operation of the paralleled CLC411s. Since "break-before-make" is a guaranteed specification of the CLC411 this configuration works nicely. Notice the buffers used in driving the disable pins of the CLC411s. These buffers may be 15V CMOS logic devices mentioned previously or any variation of the four-transistor comparator illustrated above.

Extending Input/Output Range with V_r

As can be seen in Figure 3, the magnitude of the internal regulated supply voltages is fixed by V_z. In normal operation, with ±15V external supplies, $+V_r$ is nominally +9V when left floating. CMIR (common mode input range) and VO (output voltage range, no load) are specified under these conditions. These parameters implicitly have 0V as their midpoint, i.e. the VO range is ±6V, centered at 0V.

Figure 7: DC Parameters as a Function of $+V_r$



An external voltage source can be applied to $+V_r$ to shift the range of the input/output voltages. For example, if it were desired to move the positive VO range from +6V to a +9V maximum in unipolar operation, Figure 7, "DC Parameters as a Function of $+V_r$", is used to determine the required supply and $+V_r$ voltages. Referring to Figure 7, locate the point on the $+VO_{MAX}$ line where the ordinate is +9V. Draw a vertical line from this point intersecting the other lines in the graph. The circuit voltages are the ordinates of these intersections. For this example these points are shown in the graph as solid dots. The required voltage sources are $+V_r$=+12V, $+V_{CC}$=+12V, $-V_{CC}$=-12V. When these supply and reference voltages are applied, the range for VO is -3V to +9V, and CMIR ranges from -1V to +7V. The difference between the minimum and maximum voltages is constant, i.e. 12V for VO, only the midpoint has been shifted, i.e. from 0V to +3V for VO.

Note that in this example the $-V_r$ pin has been left open (or bypassed to reduce high-frequency noise). The difference between $+V_r$ and $-V_r$ is fixed by V_z. A level-shifting voltage can be applied to only one of the reference pins, not both. If extended operation were needed in the negative direction, Figure 4 may be used by changing the signs, and applying the resultant negative voltage to the $-V_r$ pin. It is recommended that $+V_r$ be used for positive shifts, and $-V_r$ for negative shifts of input/output voltage range.

Printed Circuit Layout & Evaluation Board

Refer to application note OA-15, "Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers," for board layout guidelines and construction techniques. Two very important points to consider before creating a layout which are found in the above application note are worth reiteration. First the input and output pins are sensitive to parasitic capacitances. These parasitic capacitances can cause frequency-response peaking or sustained oscillation. To minimize the adverse effect of parasitic capacitances, the ground plane should be removed from those pins to a distance of at least 0.25" Second, leads should be kept as short as possible in the finished layout. In particular, the feedback resistor should have its shortest lead on the inverting input side of the CLC411. The output is less sensitive to parasitic capacitance and therefore can drive the longer of the two feedback resistor connections. The evaluation board available for the CLC411 (part #730013 for through-hole packages, 730027 for SO-8) may be used as a reference for proper board layout. Application schematics for this evaluation board are in the product accessories section of the Comlinear databook.

Comlinear Corporation

Dual Wideband Video Op Amp

Preliminary CLC412

APPLICATIONS:

- HDTV, NTSC & PAL video systems
- video switching and distribution
- muliti-channel tele-communications amplifier
- wideband active filters
- cable drivers
- dc coupled single-to-differential conversions

FEATURES (typical):

- 250MHz -3dB bandwidth (SOIC)
- 0.1dB gain flatness to 30MHz
- 5mA per channel quiescent current
- 0.01%, 0.025° differential gain, phase
- -82dBc channel isolation @ 10MHz (SOIC)
- 1300V/µs slew rate
- 70mA continuous output current
- gain range ±1 to ±10V/V

DESCRIPTION

The CLC412 combines a high-speed complementary bi-polar process with Comlinear's proprietary current-feedback topology to produce a very high-speed dual op amp. The CLC412 provides a 250MHz -3dB bandwidth (SOIC) at a gain of +2 and a 1300V/µs slew rate while consuming only 50mW per amplifier from ±5V supplies.

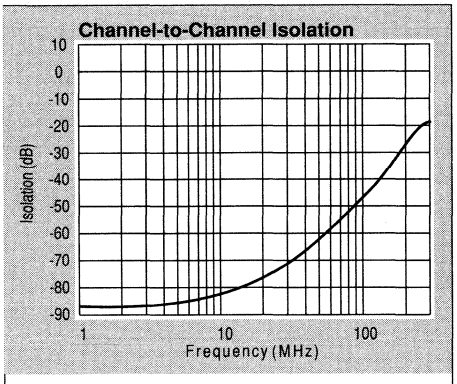
The CLC412 offers exceptional video performance with its 0.01% and 0.025° differential gain and phase errors for NTSC and PAL video signals while driving one back terminated 75Ω load. The CLC412 also offers flat gain response to 30MHz of 0.1dB and high channel-channel isolation at 10MHz of -82dB (SOIC), -68dB (PDIP). Additionally, each amplifier delivers a 70mA continuous output current (R_L=100Ω). This level of performance makes the CLC412 an ideal dual op amp for many professional video applications.

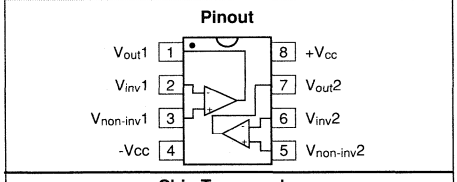
The CLC412 is also well suited for wideband signal conditioning active filters such as anti-aliasing filters for high-speed A/D converters. Its small 8-pin SOIC package, low power requirement and low noise and distortion allow the CLC412 to serve portable RF applications such as tele-video/communications.

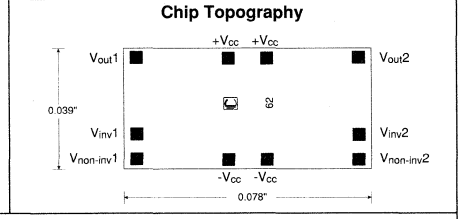
The CLC412 is available in the following versions.

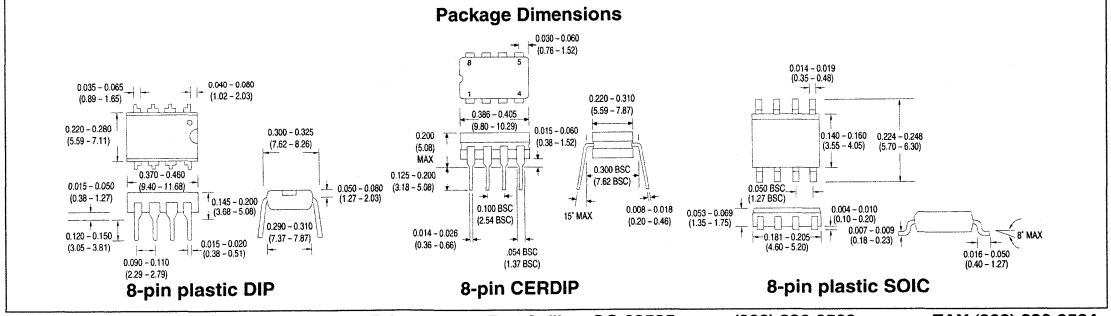
CLC412AJP	-40°C to +85°C	8-pin Plastic DIP
CLC412AJE	-40°C to +85°C	8-pin Plastic SOIC
CLC412AIB	-40°C to +85°C	8-pin CERDIP
CLC412A8B	-55°C to +125°C	8-pin CERDIP, MIL-STD-883, Level B
CLC412A8L-2	-55°C to +125°C	20-pin LCC, MIL-STD-883, Level B
CLC412ALC	-55°C to +125°C	dice
CLC412AMC	-55°C to +125°C	dice, MIL-STD-883, Level B

Contact factory for other packages and DESC SMD number.









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CLC412 Electrical Characteristics (A_V = +2; R_f = 750Ω; V_{CC} = ±5V; R_L = 100Ω)

PARAMETERS	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC412 AJP	+25°C	-40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
†-3dB bandwidth (AJP)[1]	V_{out} < 0.5V_{pp}	320	205	205	145	MHz	SSBW
(AJP)[1]	V_{out} < 4.0V_{pp}	105	80[2]	80	65	MHz	LSBW
gain flatness	V_{out} < 0.5V_{pp}						
† peaking	DC to 30MHz	0.0	0.3	0.2	0.3	dB	GFP
† rolloff	DC to 30MHz	0.1	TBD	TBD	TBD	dB	GFR
† rolloff	f_o=200MHz	1.5	2.7	2.7	8	dB	GFR
linear phase deviation	DC to 75MHz	0.1	TBD	TBD	TBD	°	LPD
differential gain	3.58 & 4.43MHz, R_L=150Ω	0.01	TBD	TBD	TBD	%	DG
differential phase	3.58 & 4.43MHz, R_L=150Ω	0.025	0.05	0.05	0.10	°	DP
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	1.1	1.7	1.7	2.4	ns	TRS
	4V step	3.2	4.4[2]	4.4	4.8	ns	TRL
settling time to 0.05%	2V step	12	18	18	20	ns	TSS
overshoot	0.5V step	TBD	TBD	TBD	TBD	%	OS
slew rate	2V step	1300	1000	1000	800	V/µs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	$2V_{pp}$, 20MHz	- 46	- 42	- 42	- 38	dBc	HD2
†3rd harmonic distortion	$2V_{pp}$, 20MHz	- 50	- 46	- 46	- 42	dBc	HD3
3rd order intermodulation intercept	10MHz	TBD				dBm	IMD
equivalent noise input							
non-inverting voltage	>1MHz	2.7	3.4	3.4	3.8	nV/√Hz	VN
inverting current	>1MHz	11.0	13.9	13.9	15.5	pA/√Hz	NICN
non-inverting current	>1MHz	2.1	2.6	2.6	3.0	pA/√Hz	ICN
noise floor	>1MHz	- 157	- 156	- 156	- 155	dBm_{1Hz}	SNF
crosstalk (AJP)[1]	10MHz	68	62	62	62	dB	XTLK
STATIC DC PERFORMANCE							
*input offset voltage		± 2	± 10	± 6	± 12	mV	VIO
average drift		± 30	60	—	60	µV/°C	DVIO
*input bias current	non-inverting	5	28	12	12	µA	IBN
average drift		30	187	—	90	A/°C	DIBN
input bias current	inverting	± 3	25	15	20	µA	IBI
average drift		± 20	125	—	80	nA/°C	DIBI
†power supply rejection ratio	DC	50	46	46	44	dB	PSRR
♠common mode rejection ratio	DC	50	45	45	42	dB	CMRR
*supply current	R_L= ∞	10.2	13.6	12.8	12.8	mA	ICC
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	1000	300	500	500	kΩ	RIN
input capacitance	non-inverting	1.0	2.0	2.0	2.0	pF	CIN
output resistance	closed loop	0.2	0.6	0.3	0.2	Ω	ROUT
output voltage range	R_L= ∞	+ 3.8,-3.3	+ 3.6,-2.9	+ 3.7,-3.0	+ 3.7,-3.0	V	VO
	R_L=100Ω	+ 3.1,-2.9	+ 1.6,-2.5	± 2.7	± 2.7	V	VOL
	R_L=100Ω (0° to 70°C)			+ 2.5,-2.6		V	VOL
input voltage range	common mode	± 2.2	± 1.4	± 2.0	± 2.0	V	CMIR
output current		70	25	45	45	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} short circuit protected to ground, however maximum reliabiliy is obtained if I_{out} does not exceed...	150mA
common-mode input voltage	±V_{cc}
maximum junction temperature	+175°C
operating temperature range	
AJ/AI	-40°C to +85°C
A8/AM/AL:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

Recommended gain range ±1 to ±10V/V

Notes:

* AJ,AI : 100% tested at +25°C, sample tested at +85°C.
† AJ : Sample tested at +25°C.
† AI : 100% tested at +25°C.
* A8 : 100% tested at +25°C, -55°C, +125°C.
† A8 : 100% tested at +25°C, sample at -55°C, +125°C
* AL, AM : 100% wafer probed +25°C to +25°C min/max specs.
♠ SMD : Sample tested at +25°C, -55°C, +125°C.
note 1) : Due to differing package parasitics, performance is package dependant, and therefore will be specified separately.
note 2) : Specification is guaranteed at V_{out}=3Vpp.

Comlinear Corporation

Quad, Low-Power Monolithic Op Amp

CLC414

APPLICATIONS:
- composite video distribution amps
- HDTV amplifiers
- RGB-video amplifiers
- CCD signal processing
- active filters
- instrumentation diff amps
- general purpose high density requirements

FEATURES (typical):
- 90MHz small-signal bandwidth
- 2.5mA quiescent current per amplifier
- 70dB channel isolation @ 5MHz
- 0.1%/0.12° differential gain/phase
- 16ns settling to 0.1%
- 1000V/µs slew rate
- 3.3ns rise and fall time ($2V_{pp}$)
- 70mA output current

DESCRIPTION:

The CLC414 is a low-power, quad, monolithic operational amplifier designed for intermediate-gain applications where power and cost per channel are of primary concern. Benefiting from Comlinear's current feedback architecture, the CLC414 offers a gain range of ±1 to ±10 while providing stable, oscillation-free operation without external compensation, even at unity gain.

Operating from ±5V supplies, the CLC414 consumes only 25mW of power per channel, yet maintains a 90MHz small-signal bandwidth and a 1000V/µs slew rate. The CLC414 also provides wide channel isolation with its 70dB crosstalk (input referred at 5MHz). Applications requiring a high- density solution to high-speed amplification such as active filters and instrumentation diff amps will benefit from the CLC414's four integrated, wideband op amps in one 14-pin package.

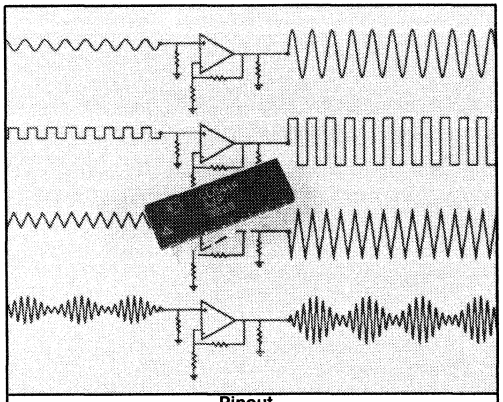
Commercial remote-sensing applications and battery-powered radio transceivers requiring high-performance, low-power amplifiers will find the CLC414 to be an attractive, cost- effective solution. In composite video switching and distribution applications, the CLC414 offers differential gain and phase performance of 0.1%, 0.12° at 3.58MHz.

The lower power CLC414 and the wideband CLC415 are quad versions of the CLC406. Both of these quads afford the designer lower power consumption and lower cost per channel with the additional benefit of requiring less board space per amplifier.

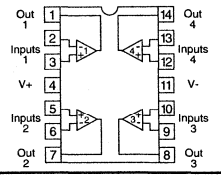
Constructed using an advanced, complementary bipolar process and Comlinear's proven current feedback architectures, the CLC414 is available in several versions to meet a variety of requirements.

CLC414AJP	-40°C to +85°C	14-pin plastic DIP
CLC414AJE	-40°C to +85°C	14-pin plastic SOIC
CLC414AID	-40°C to +85°C	14-pin hermetic side-brazed ceramic DIP
CLC414A8D	-55°C to +125°C	14-pin hermetic side-brazed ceramic DIP, ML-STD-883, Level B
CLC414ALC	-55°C to +125°C	dice
CLC414AMC	-55°C to +125°C	dice qualified to Method 5008, MIL- STD-883, Level B

Contact factory for other packages. DESC SMD number 5962-91693.

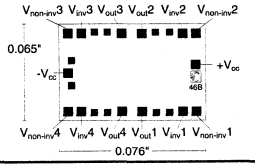


Pinout



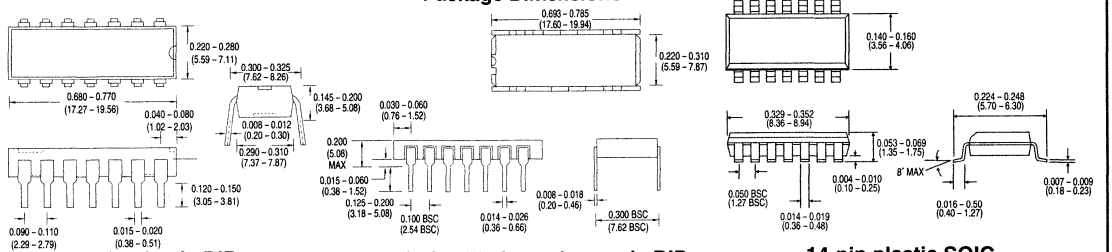
DIP and SOIC versions

Chip Topography



Height is 0.014 inches. Dimensions are typical values. NOTE: Backside connected to -Vcc. It is not necessary to electrically connect the backside to the negative supply. Contact Comlinear for complete die information.

Package Dimensions



14-pin plastic DIP | 14-pin side-brazed ceramic DIP | 14-pin plastic SOIC

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

DS414.02 (Introductory)

January 1993

INTRODUCTORY INFORMATION: specifications are based on the characteristics of a limited number of devices.

Electrical Characteristics (A_V=+6; V_{cc}=±5V; R_L = 100Ω; R_f = 500Ω)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC414AJ/AI	+25°C	–40°C	+25°C	+85°C		
Ambient Temperature	CLC414A8/AL/AM	+25°C	–55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
† –3dB bandwidth	V_{out}<2V_{pp}	90	>60	>60	>45	MHz	SSBW
	V_{out} <5V_{pp}	55	>35	>40	>35	MHz	LSBW
gain flatness[1]	V_{out} <2V_{pp}						
† peaking	DC to 15MHz	0	<0.15	<0.15	<0.15	dB	GFPL
† peaking	>15MHz	0	<0.3	<0.3	<0.3	dB	GFPH
† rolloff	DC to 30MHz	0.3	<1.0	<1.0	<1.5	dB	GFR
linear phase deviation	DC to 30MHZ	0.8	<1.2	<1.2	<1.5	°	LPD
differential gain (A_V=+2)	150Ω load, 3.58MHz	0.10	<0.15	<0.20	<0.25	%	DG1
	4.43MHz	0.12	<0.20	<0.25	<0.30	%	DG2
differential phase (A_V=+2)	150Ω load, 3.58MHz	0.12	<0.15	<0.20	<0.50	°	DP1
	4.43MHz	0.15	<0.20	<0.25	<0.60	°	DP2
crosstalk input referred	5MHz (all hostile)	60	<58	<58	<56	dB	XT
input referred	5MHz (chan. to chan.)	70	<63	<63	<61	dB	CXT
TIME DOMAIN RESPONSE							
rise and fall time	2V step	3.3	<5.0	<5.0	<6.5	ns	TRS
	5V step	4.0	<7.0	<6.0	<7.0	ns	TRL
settling time to 0.1%	2V step	16	<24	<24	<30	ns	TS1
to 0.02%	2V step	60	<80	<80	<100	ns	TS2
overshoot	2V step	5	<10	<10	<10	%	OS
slew rate		1000	>600	>600	>480	V/µs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	2V_{pp}, 5MHz	–47	<–41	<–41	<–37	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 5MHz	–55	<–47	<–47	<–45	dBc	HD3
equivalent noise input							
non-inverting voltage	>1MHz	4.2	<5.0	<5.0	<5.5	nV/√Hz	VN
inverting current	>1MHz	9.8	<11.8	<11.8	<13.0	pA/√Hz	ICN
non-inverting current	>1MHz	1.3	<1.6	<1.6	<1.8	pA/√Hz	NCN
total noise floor	>1MHz	–154	<–153	<–153	<–152	dBm_{1Hz}	SNF
total integrated noise	>1MHz to 75MHz	37	<44	<44	<48	µV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		2	<10.5	<6	<14	mV	VIO
average temperature coefficient		30	<80	—	<80	µV/°C	DVIO
*input bias current	non-inverting	1	<10	<5	<5	µA	IBN
average temperature coefficient		20	<75	—	<30	nA/°C	DIBN
*input bias current	inverting	2	<20	<6	<10	µA	IBI
average temperature coefficient		20	<140	—	<75	nA°C	DIBI
†power supply rejection ratio		50	>46	>46	>44	dB	PSRR
♠ common mode rejection ratio		50	>45	>45	>43	dB	CMRR
*supply current, all channels	no load	10	<11.5	<11.5	<11.5	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		2000	>500	>1000	>1000	kΩ	RIN
non-inverting input capacitance		1.0	<2.0	<2.0	<2.0	pF	CIN
ouput impedance	DC	0.2	<0.6	<0.3	<0.2	Ω	RO
output voltage range	R_L=100Ω	±2.8	±2.5	±2.6	±2.7	V	VO
common mode input range		±2.2	±1.4	±2.0	±2.0	V	CMIR
output current		70	30	50	50	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, however, maximum reliability is obtained if I_{out} does not exceed...	70mA
common mode input voltage	±V_{cc}
differential input voltage	±10V
maximum junction temperature	+175°C
operating temperature range	
AI/AJ:	–40°C to +85°C
A8/AL/AM:	–55°C to +125°C
storage temperature range	–65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

recommended gain range: ±1 to ±10

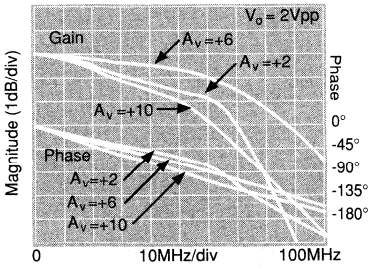
Notes:

*	AI,AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested +25°C, –55°C, +125°C.
†	A8	100% tested +25°C, sample at –55°C, +125°C.
*	AL, AM	100% wafer probed at +25°C to +25°C min/max specifications.
♠	SMD	Sample tested at +25°C, –55°C, +125°C.

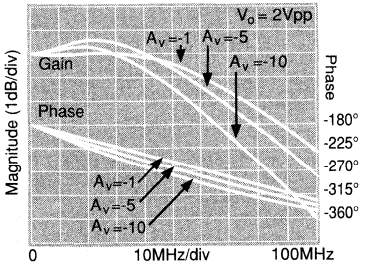
note 1: Gain flatness tests performed from 0.1MHz

Typical Performance Characteristics (T_A =+26°C, A_V =+6, V_{CC} =±5V, R_L =100Ω, R_f =500Ω)

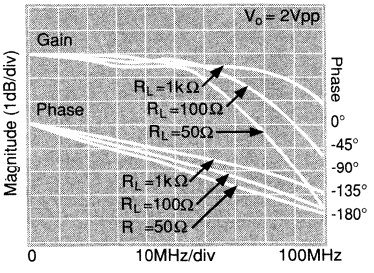
Non-Inverting Frequency Response



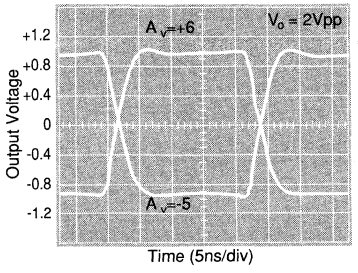
Inverting Frequency Response



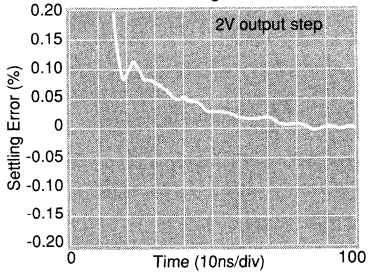
Frequency Response for Various R_Ls



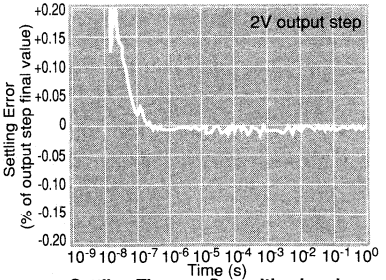
Small Signal Pulse Response



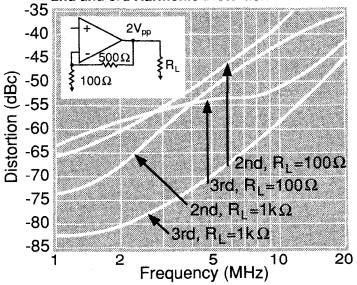
Short-Term Settling Time



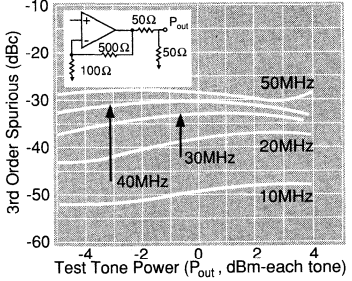
Long-Term Settling Time



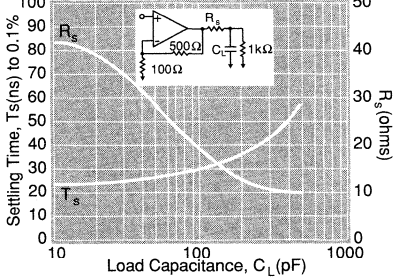
2nd and 3rd Harmonic Distortion



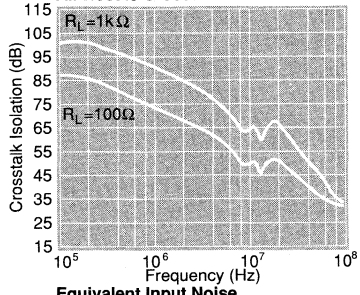
2-Tone, 3rd Order Spurious Levels



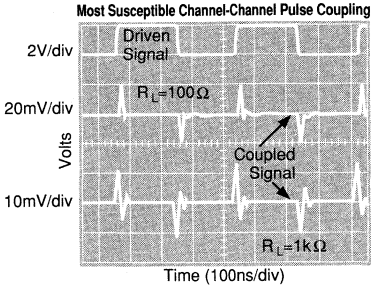
Settling Time vs. Capacitive Load



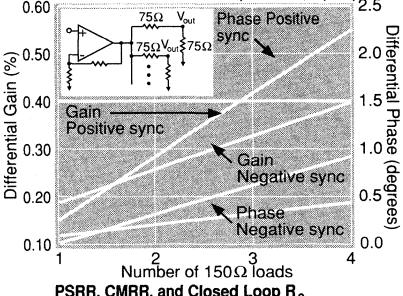
All-Hostile Crosstalk Isolation



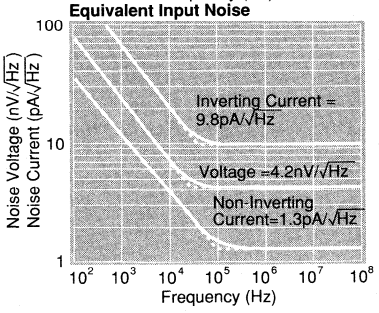
Most Susceptible Channel-Channel Pulse Coupling



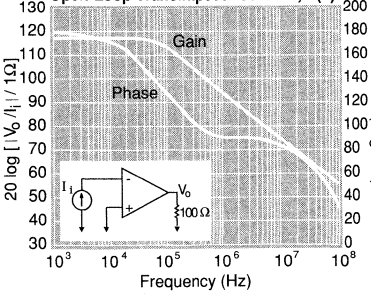
Differential Gain and Phase (4.43 MHz, A_V=+2)



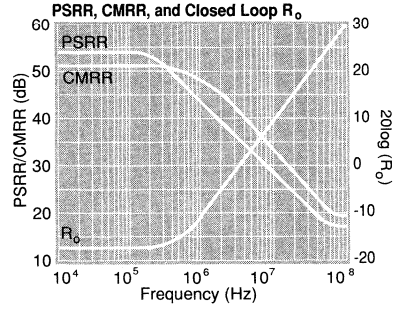
Equivalent Input Noise



Open-Loop Transimpedance Gain, Z(s)



PSRR, CMRR, and Closed Loop R_o



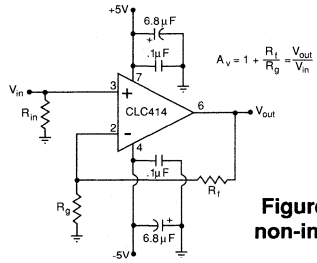
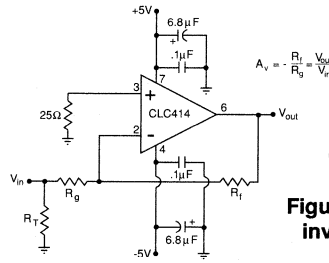


Figure 1: recommended non-inverting gain circuit



Select R_T to yield desired $R_{in} = R_T || R_g$

Figure 2: recommended inverting gain circuit

Feedback Resistor

The CLC414 achieves its exceptional AC performance while requiring very low quiescent power by using the current feedback topology and an internal slew rate enhancement circuit. The loop gain and frequency response for a current feedback op amp is predominantly set by the feedback resistor value. The CLC414 is optimized for a gain of +6 to use a 500Ω feedback resistor **(use a 1kΩ R_f for maximally flat response at a gain of +2).** Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 provides a more detailed discussion of choosing a feedback resistor. The equations found in this application note are to be considered a starting point for the determination of R_f at any gain. The value of input impedance for the CLC414 is approximately 250Ω. These equations do not account for parasitic capacitance at the inverting input nor across R_f. The plot found below entitled "Recommended R_f vs. Gain" offers values of R_f which will optimize the frequency response of the CLC414 over its ±1 to ±10 gain range. Unlike voltage feedback, current feedback op amps require a non-zero R_f for unity gain followers.

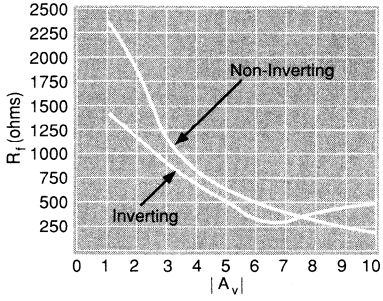


Figure 3: recommended R_f vs. gain

Unused Amplifiers

It is recommended that any unused amplifiers in the quad package be connected as unity gain followers (R_f=500Ω) with the non-inverting input tied to ground through a 50Ω resistor.

Slew Rate and Harmonic Distortion

Please see the application information for the CLC406.

Differential Gain and Phase

Differential gain and phase performance specifications are common to composite video distribution applications. These specifications refer to the change in small signal gain and phase of the color subcarrier frequency (4.43MHz for PAL composite video) as the amplifier output is swept over a range of DC voltages. Application Note OA-08 provides an additional discussion of differential gain and phase measurements.

Non-inverting Source Impedance

For best operation, the DC source impedance looking out of the non-inverting input should be less than 3kΩ but greater than 20Ω. Parasitic self oscillations may occur in the input transistors if the DC source impedance is out of this range. This impedance also acts as the gain for the non-inverting input bias and noise currents and therefore can become troublesome for high values of DC source impedance. The inverting configuration of Figure 2 shows a 25Ω resistor to ground on the non-inverting input which insures stability but does not provide bias current cancellation. The input bias currents are unrelated for a current feedback amplifier which eliminates the need for source impedance matching to achieve bias current cancellation.

DC Accuracy and Noise Calculation

Please refer to the application information for the CLC406.

Crosstalk

In any multi-channel integrated circuit there is an undesirable tendency for the signal in one channel to couple with and reproduce itself in the output of another channel. This effect is referred to as crosstalk. Crosstalk is expressed as channel separation or channel isolation which indicates the magnitude of this undesirable effect. This effect is measured by driving one or more channels and observing the output of the other undriven channel(s). The CLC414 plot page offers two different graphs detailing the effect of crosstalk over frequency. One plot entitled "All-Hostile Crosstalk Isolation" graphs all-hostile input-referred crosstalk. All-hostile crosstalk refers to the condition where three channels are driven simultaneously while observing the output of the undriven fourth channel. Input-referred implies that crosstalk is directly affected by gain and therefore a higher gain increases the crosstalk effect by a factor equal to that gain setting. The plot entitled "Most Susceptible Channel-to-Channel Pulse Coupling" describes the effect of crosstalk when one channel is driven with a $2V_{pp}$ pulse while the output of the most effected channel is observed.

Printed Circuit Layout

As with any high speed component, a careful attention to the board layout is necessary for optimum performance. Of particular importance is the careful control of parasitic capacitances on the output pin. As the output impedance plot shows, the closed loop output for the CLC414 eventually becomes inductive as the loop gain rolls off with increasing frequency. Direct capacitive loading on the output pin can quickly lead to peaking in the frequency response, overshoot in the pulse response, ringing or even sustained oscillations. The "Settling Time vs. Capacitive Load" plot should be used as a starting point for the selection of a series output resistor when a capacitive load must be driven. A quad amplifier will require careful attention to signal routing in order to minimize the effects of crosstalk. Signal coupling through the power supplies can be reduced with bypass capacitors placed close to the device supply pins.

Evaluation Board

Evaluation PC boards (part number 730024 for through-hole and 730031 for SOIC) for the CLC414 are available.

Comlinear Corporation

Quad, Wideband Monolithic Op Amp

CLC415

APPLICATIONS:
- composite video distribution amps
- HDTV amplifiers
- RGB-video amplifiers
- CCD signal processing
- active filters
- instrumentation diff amps
- channelized EW

FEATURES (typical):
- 160MHz small-signal bandwidth
- 5mA quiescent current per amplifier
- 70dB channel isolation @ 5MHz
- 0.03%/0.03° differential gain/phase
- 12ns settling to 0.1%
- 1500V/µs slew rate
- 2.0ns rise and fall time ($2V_{pp}$)
- 70mA output current per amplifier

DESCRIPTION:

The CLC415 is a wideband, quad, monolithic operational amplifier designed for intermediate-gain applications where power and cost per channel are of primary concern. Benefitting from Comlinear's current feedback architecture, the CLC415 offers a gain range of ±1 to ±10 while providing stable, oscillation-free operation without external compensation, even at unity gain.

Operating from ±5V supplies, the CLC415 consumes only 50mW of power per channel, yet maintains a 160MHz small-signal bandwidth and a 1500V/µs slew rate. High density applications requiring an integrated solution will enjoy the CLC415's 70dB channel isolation (input referred @ 5MHz).

With its exceptional differential gain and phase, typically 0.03% and 0.03° @ 3.58MHz, the CLC415 is designed to meet the performance and cost per channel requirements of high volume composite video applications. The CLC415's large-signal bandwidth, high slew rate and high drive capability are features well suited for RGB-video applications.

The CLC415 is a quad version of the high speed CLC406 while the CLC414 is a lower power quad version of the same. Both of these quads afford the designer lower power consumption and lower cost per channel with the additional benefit of requiring less board space per amplifier.

Constructed using an advanced, complementary bipolar process and Comlinear's proven current feedback architectures, the CLC415 is available in several versions to meet a variety of requirements.

CLC415AJP	-40°C to +85°C	14-pin plastic DIP
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CLC415ALC	-55°C to +125°C	dice
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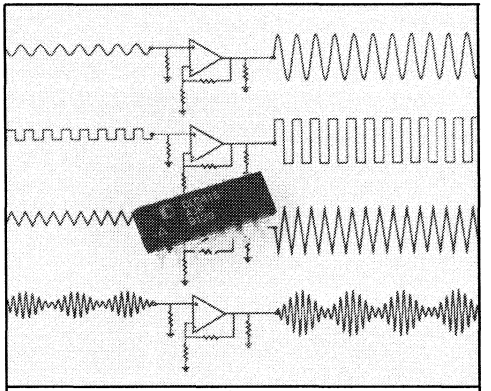
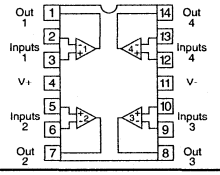
Contact factory for other packages. DESC SMD number 5962-93055.

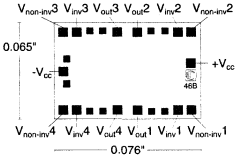


Pinout



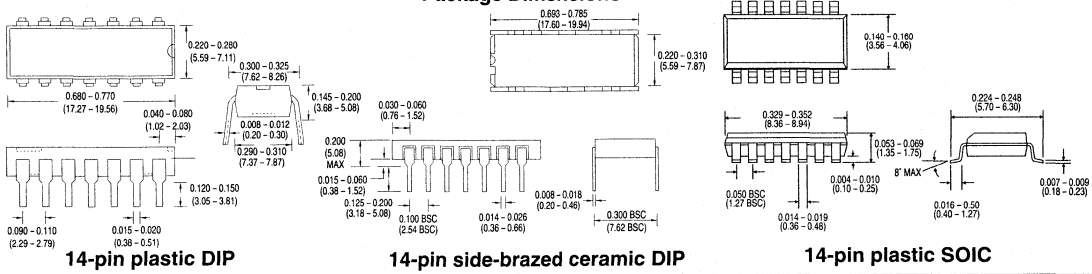
DIP and SOIC versions

Chip Topography



Height is 0.014 inches. Dimensions are typical values. NOTE: Backside connected to -Vcc. It is not necessary to electrically connect the backside to the negative supply. Contact Comlinear for complete die information.

Package Dimensions



14-pin plastic DIP | 14-pin side-brazed ceramic DIP | 14-pin plastic SOIC

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

INTRODUCTORY INFORMATION: specifications are based on the characteristics of a limited number of devices.

Electrical Characteristics (A_V=+6; V_{cc}=±5V; R_L = 100Ω; R_f = 500Ω)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC415AJ/AI	+25°C	–40°C	+25°C	+85°C		
Ambient Temperature	CLC415A8/AL/AM	+25°C	–55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
† –3dB bandwidth	V_{out}<2V_{pp}	160	>120	>120	>90	MHz	SSBW
	V_{out} <5V_{pp}	120	>85	>90	>80	MHz	LSBW
gain flatness[1]	V_{out} <2V_{pp}						
† peaking	DC to 25MHz	0	<0.2	<0.2	<0.2	dB	GFPL
† peaking	>25MHz	0	<0.5	<0.5	<0.5	dB	GFPH
† rolloff	DC to 50MHz	0.2	<0.7	<0.7	<1.1	dB	GFR
linear phase deviation	DC to 75MHZ	0.5	<1.0	<1.0	<1.3	°	LPD
differential gain (A_V=+2)	150Ω load, 3.58MHz	0.03	<0.08	<0.08	<0.08	%	DG1
	4.43MHz	0.03	<0.10	<0.10	<0.10	%	DG2
differential phase (A_V=+2)	150Ω load, 3.58MHz	0.03	<0.08	<0.08	<0.08	°	DP1
	4.43MHz	0.03	<0.10	<0.10	<0.10	°	DP2
crosstalk input referred	5MHz (all hostile)	65	<60	<60	<59	dB	XT
input referred	5MHz (chan. to chan.)	70	<63	<63	<62	dB	CXT
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.0	<3.0	<3.0	<4.0	ns	TRS
	5V step	3.0	<4.0	<3.6	<4.5	ns	TRL
settling time to 0.1%	2V step	12	<18	<18	<22	ns	TS
overshoot	2V step	8	<12	<12	<12	%	OS
slew rate		1500	>1200	>1200	>1000	V/µs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	2V_{pp}, 20MHz	–44	<–38	<–38	<–34	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 20MHz	–54	<–46	<–46	<–42	dBc	HD3
equivalent noise input							
non-inverting voltage	>1MHz	3.0	<3.6	<3.6	<4.0	nV/√Hz	VN
inverting current	>1MHz	11.5	<14	<14	<16	pA/√Hz	ICN
non-inverting current	>1MHz	2.0	<2.6	<2.6	<3.0	pA/√Hz	NCN
total noise floor	>1MHz	–157	<–155	<–155	<–154	dBm_{1Hz}	SNF
total integrated noise	>1MHz to 100MHz	37	<44	<44	<48	µV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		2	<9	<5	<10	mV	VIO
average temperature coefficient		20	<50	—	<50	µV/°C	DVIO
*input bias current	non-inverting	5	<25	<13	<13	µA	IBN
average temperature coefficient		30	<150	—	<50	nA/°C	DIBN
*input bias current	inverting	3	<18	<10	<15	µA	IBI
average temperature coefficient		20	<100	—	<50	nA°C	DIBI
†power supply rejection ratio		55	>47	>47	>45	dB	PSRR
common mode rejection ratio		50	>45	>45	>43	dB	CMRR
*supply current, all channels	no load	20	<27	<26	<24	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		1300	>300	>600	>600	kΩ	RIN
non-inverting input capacitance		1.0	<2.0	<2.0	<2.0	pF	CIN
ouput impedance	DC	0.2	<0.6	<0.3	<0.2	Ω	RO
output voltage range	R_L=100Ω	±2.6	±2.3	±2.5	±2.5	V	VO
common mode input range		±2.2	±1.4	±2.0	±2.0	V	CMIR
output current		70	50	50	50	mA	IO

Absolute Maximum Ratings

V_{cc} ±7V

I_{out} output is short circuit protected to ground, however, maximum reliability is obtained if I_{out} does not exceed... 70mA

common mode input voltage ±V_{cc}
differential input voltage ±10V
maximum junction temperature +175°C
operating temperature range
AJ/AI: –40°C to +85°C
A8/AL/AM: –55°C to +125°C
storage temperature range –65°C to +150°C
lead temperature (soldering 10 sec) +300°C

Miscellaneous Ratings

recommended gain range: ±1 to ±10

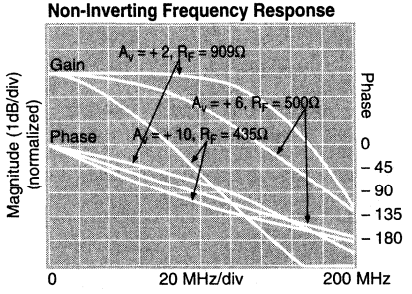
Notes:

* AI, AJ 100% tested at +25°C, sample at +85°C.
† AJ Sample tested at +25°C.
† AI 100% tested at +25°C.
* A8 100% tested +25°C, –55°C, +125°C.
† A8 100% tested +25°C, sample at –55°C, +125°C.
* AL, AM 100% wafer probed at +25°C to +25°C min/max specifications.

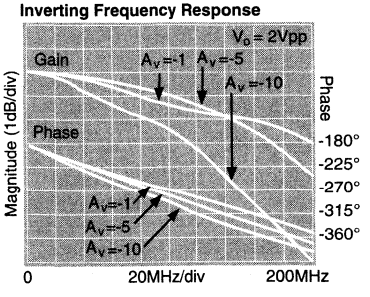
note 1: Gain flatness tests performed from 0.1 MHz

Typical Performance Characteristics (T_A =+25°C, A_V =+6, V_{CC} =±5V, R_L =100Ω, R_f =500Ω)

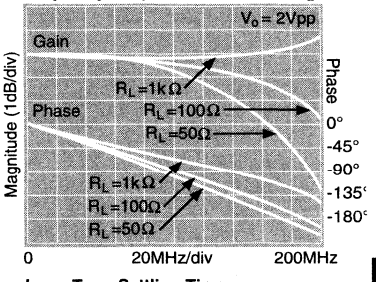
Non-Inverting Frequency Response



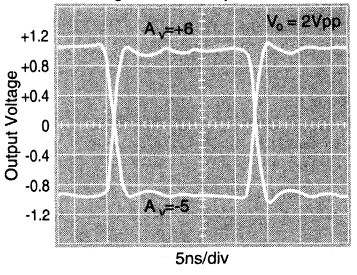
Inverting Frequency Response



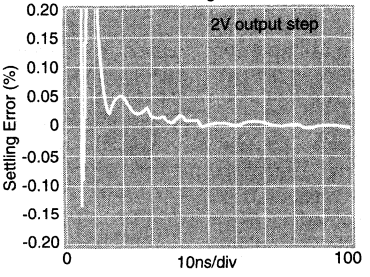
Frequency Response for Various R_Ls



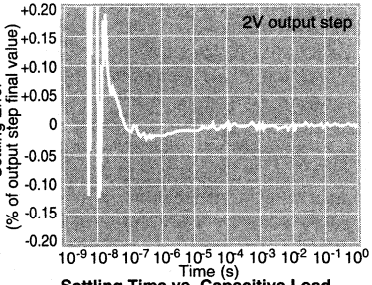
Small Signal Pulse Response



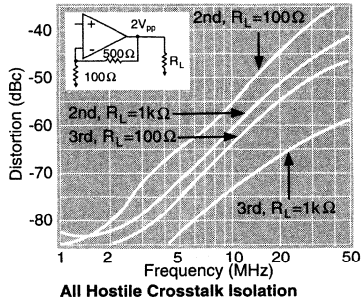
Short-Term Settling Time



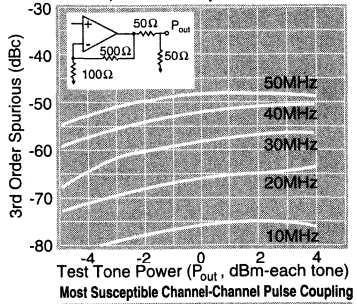
Long-Term Settling Time



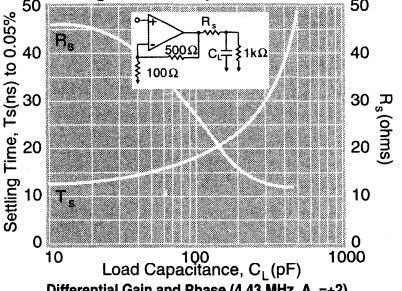
2nd and 3rd Harmonic Distortion



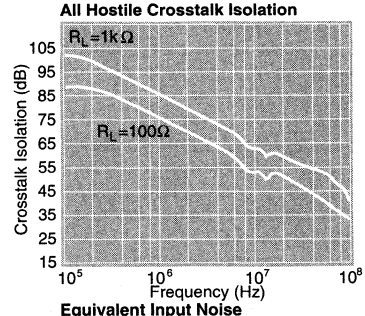
2-Tone, 3rd Order Spurious Levels



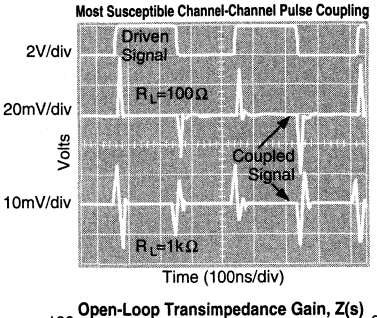
Settling Time vs. Capacitive Load



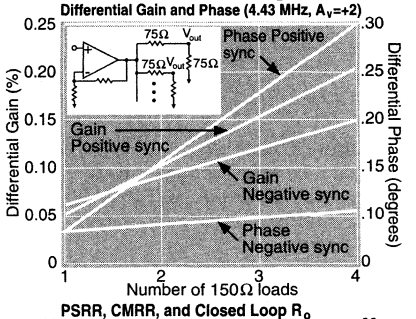
All Hostile Crosstalk Isolation



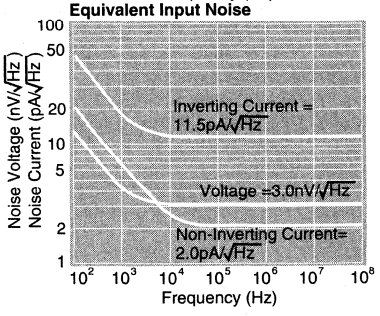
Most Susceptible Channel-Channel Pulse Coupling



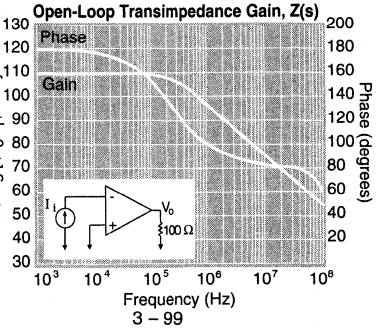
Differential Gain and Phase (4.43 MHz, A_V=+2)



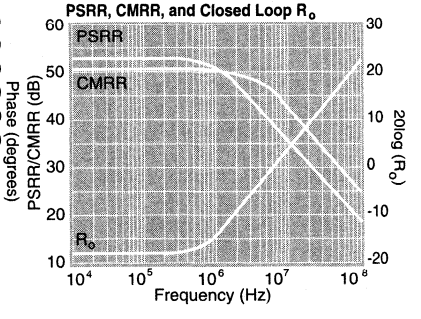
Equivalent Input Noise



Open-Loop Transimpedance Gain, Z(s)



PSRR, CMRR, and Closed Loop R_o



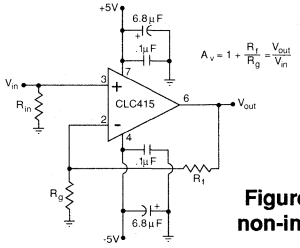
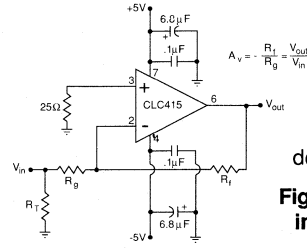


Figure 1: recommended non-inverting gain circuit



Select R_T to yield desired $R_{in} = R_T \| R_g$

Figure 2: recommended inverting gain circuit

Feedback Resistor

The CLC415 achieves its exceptional AC performance while requiring very low quiescent power by using the current feedback topology and an internal slew rate enhancement circuit. The loop gain and frequency response for a current feedback op amp is predominantly set by the feedback resistor value. The CLC415 is optimized for a gain of +6 to use a 500Ω feedback resistor **(use a 900Ω R_f for maximally flat response at a gain of +2).** Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth.

Application Note OA-13 provides a more detailed discussion of choosing a feedback resistor. The equations found in this application note are to be considered a starting point for the determination of R_f at any gain. The value of input impedance for the CLC415 is approximately 60Ω. These equations do not account for parasitic capacitance at the inverting input nor across R_f. The plot found below entitled "Recommended R_f vs. Gain" offers values of R_f which will optimize the frequency response of the CLC415 over its ±1 to ±10 gain range. Unlike voltage feedback, current feedback op amps require a non-zero R_f for unity gain followers.

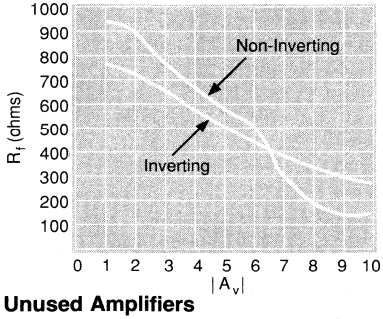


Figure 3: recommended R_f vs. gain

Unused Amplifiers

It is recommended that any unused amplifiers in the quad package be connected as unity gain followers ($R_f = 500\Omega$) with the non-inverting input tied to ground through a 50Ω resistor.

Slew Rate and Harmonic Distortion

Please see the application information for the CLC406.

Differential Gain and Phase

Differential gain and phase performance specifications are common to composite video distribution applications. These specifications refer to the change in small signal gain and phase of the color subcarrier frequency (4.43MHz for PAL composite video) as the amplifier output is swept over a range of DC voltages. Application Note OA-08 provides an additional discussion of differential gain and phase measurements.

Non-inverting Source Impedance

For best operation, the DC source impedance looking out of the non-inverting input should be less than 3kΩ but greater than 20Ω. Parasitic self oscillations may occur in the input transistors if the DC source impedance is out of this range. This impedance also acts as the gain for the non-inverting input bias and noise currents and therefore can become troublesome for high values of DC source impedance. The inverting configuration of Figure 2 shows a 25Ω resistor to ground on the non-inverting input which insures stability but does not provide bias current cancellation. The input bias currents are unrelated for a current feedback amplifier which eliminates the need for source impedance matching to achieve bias current cancellation.

DC Accuracy and Noise

Please refer to the application information section of the CLC406 for a discussion of output offset voltage and spot noise calculation.

Crosstalk

In any multi-channel integrated circuit there is an undesirable tendency for the signal in one channel to couple with and reproduce itself in the output of another channel. This effect is referred to as crosstalk. Crosstalk is expressed as channel separation or channel isolation which indicates the magnitude of this undesirable effect. This effect is measured by driving one or more channels and observing the output of the other undriven channel(s). The CLC415 plot page offers two different graphs detailing the effect of crosstalk over frequency. One plot entitled "All-Hostile Crosstalk Isolation" graphs all-hostile, input-referred crosstalk. All-hostile crosstalk refers to the condition where three channels are driven simultaneously while observing the output of the undriven fourth channel. Input-referred implies that crosstalk is directly affected by gain and therefore a higher gain increases the crosstalk effect by a factor equal to that gain setting. The plot entitled "Most Susceptible Channel-to-Channel Pulse Coupling" describes the effect of crosstalk when one channel is driven with a $2V_{pp}$ pulse while the output of the most effected channel is observed.

Printed Circuit Layout

As with any high speed component, a careful attention to the board layout is necessary for optimum performance. Of particular importance is the careful control of parasitic capacitances on the output pin. As the output impedance plot shows, the closed loop output for the CLC415 eventually becomes inductive as the loop gain rolls off with increasing frequency. Direct capacitive loading on the output pin can quickly lead to peaking in the frequency response, overshoot in the pulse response, ringing or even sustained oscillations. The "Settling Time vs. Capacitive Load" plot should be used as a starting point for the selection of a series output resistor when a capacitive load must be driven. A quad amplifier will require careful attention to signal routing in order to minimize the effects of crosstalk. Signal coupling through the power supplies can be reduced with bypass capacitors placed close to the device supply pins.

Evaluation Board

Evaluation PC boards (part number 730024 for through-hole and 730031 for SOIC) for the CLC415 are available.

Comlinear Corporation

High-Speed, Voltage Feedback Op-Amp

CLC420

APPLICATIONS:
- active filters/integrators
- differential amplifiers
- pin diode receivers
- log amplifiers
- D/A converters
- photo multiplier amplifiers

FEATURES (typical):
- 300MHz small signal bandwidth
- 1100 V/µs slew rate
- unity gain stability
- 0.01% settling in 18ns
- CLC420B: 0.5mV input offset voltage, 4µV/°C
- 0.2µA input offset current
- 2pA$\sqrt{Hz}$ current noise
- recommended gain range ±1 to ±10

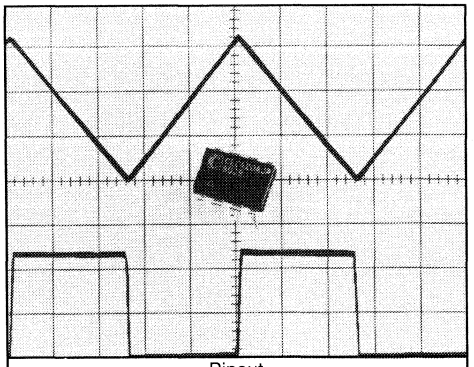
The CLC420 is an operational amplifier designed for applications requiring matched inputs, integration or transimpedance amplification. Utilizing voltage feedback architecture, the CLC420 offers a 300MHz bandwidth, a 1100V/µs slew rate and a 4mA supply current (power consumption of 40mW, ±5V supplies). Additional benefits of the CLC420B are a 0.5mV input offset voltage and a 4µV/°C temperature coefficient.

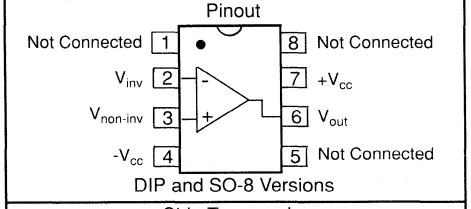
Applications such as differential amplifiers will benefit from 70dB common mode rejection ratio and an input offset current of 0.2µA. With its unity-gain stability, 2pA/$\sqrt{Hz}$ current noise and 3µA of input bias current, the CLC420 is designed to meet the needs of filter applications and log amplifiers. The low input offset current and current noise, combined with a settling time of 18ns to 0.01% make the CLC420 ideal for D/A converters, pin diode receivers and photo multipliers amplifiers. All applications will find 70dB power supply rejection ratio attractive.

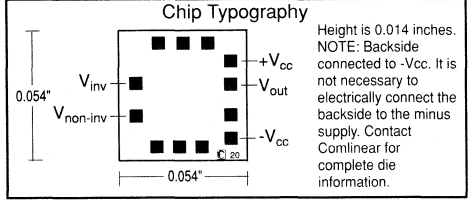
The CLC420 is available in several versions to meet a variety of requirements.

CLC420AJP/BJP	-40°C to +85°C	8-pin plastic DIP
CLC420AJE/BJE	-40°C to +85°C	8-pin plastic SOIC
CLC420AID/BID	-40°C to +85°C	8-pin side-brazed DIP
CLC420A8D/B8D	-55°C to +125°C	8-pin side-brazed DIP, MIL-STD-883, Level B
CLC420ALC	-55°C to +125°C	dice
CLC420AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

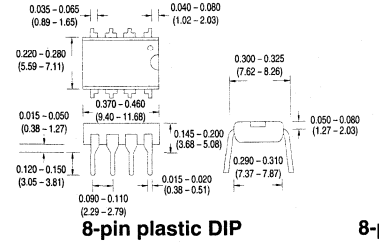
Contact factory for other packages. DESC SMD number, 5962-91758.



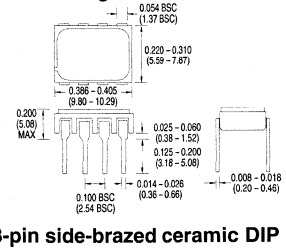




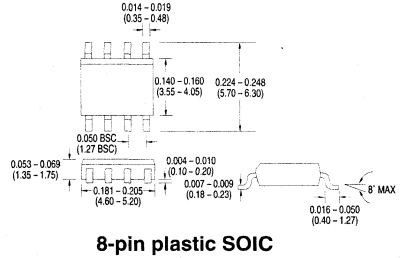
Package Dimensions



8-pin plastic DIP



8-pin side-brazed ceramic DIP



8-pin plastic SOIC

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics (A_V=+1, V_{CC}=±5.0V, R_L = 100Ω, R_f=0Ω, unless specified)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC420A8/B8/AL/AM	+25°C	-55°C	+25°C	+125°C		
Ambient Temperature	CLC420AJ/BJ/AI/BI	+25°C	-40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{OUT}<0.4V_{pp}	300	>200	>200	>130	MHz	SSBW
	V_{OUT}<5V_{pp}	40	>20	>25	>20	MHz	LSBW
†A_V=-1, R_f=500Ω	V_{OUT}<0.4V_{pp}	100	>65	>65	>45	MHz	SSBWI
A_V=-1, R_f=500Ω	V_{OUT}<5V_{pp}	60	>30	>35	>30	MHz	LSBWI
gain flatness	V_{OUT}<0.4V_{pp}						
peaking	0.1MHz to 100MHz	0	<1	<0.6	<0.6	dB	GFPL
peaking	>100MHz	0	<5	<3	<3	dB	GFPH
rolloff	0.1MHz to 100MHz	0.2	<1	<1	<2	dB	GFR
†rolloff, A_V=-1, R_f=500Ω	0.1MHz to 30MHz	0.2	<1.4	<1.4	<1.6	dB	GFRI
linear phase deviation	0.1MHz to 100MHz	0.9	<1.8	<1.8	<2.5	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	0.4V step	1.2	< 2	< 2	< 3	ns	TRS
	5V step	14	< 25	< 20	< 20	ns	TRL
rise and fall time, A_V = -1, R_f =500Ω	0.4V step	3.5	< 5.5	< 5.5	< 7.8	ns	TRSI
	5V step	6	< 10	< 9.5	< 10	ns	TRLI
settling time to ±0.1%	2V step	12	< 18	< 18	< 18	ns	TSS
±0.01%	2V step	18	< 25	< 25	< 25	ns	TSP
overshoot	0.4V step	8	< 35	< 25	< 25	%	OS
slew rate	5V step	1100	> 600	> 750	> 600	V/µs	SR
slew rate, A_V = -1, R_f = 500 Ω	5V step	750	> 430	> 500	> 430	V/µs	SRI
DISTORTION AND NOISE RESPONSE							
2ND harmonic distortion	2V_{PP}, 20MHz	-50	<-40	<-40	<-40	dBc	HD2
3RD harmonic distortion	2V_{PP}, 20MHz	-53	<-45	<-45	<-40	dBc	HD3
†2ND harmonic distortion, A_V=-1,	2V_{PP}, 20MHz, R_f=500Ω	-51	<-40	<-40	<-40	dBc	HD2
†3RD harmonic distortion, A_V=-1,	2V_{PP}, 20MHz, R_f=500Ω	-51	<-40	<-40	<-35	dBc	HD3
input referred noise							
voltage	1MHz to 200MHz	4.2	< 5.3	< 5.3	<6	nV/√Hz	VN
current	1MHz to 200MHz	2	< 2.9	< 2.6	<2.3	pA/√Hz	ICN
STATIC DC PERFORMANCE							
***Input offset voltage**	**(A version)**	**1**	**<3.2**	**<2**	**<3.5**	**mV**	**VIO**
average temperature coefficient		**8**	**<15**	**—**	**<15**	**µV/°C**	**DVIO**
***input offset voltage**	**(B version)**	**0.5**	**<1.6**	**<0.8**	**<1.8**	**mV**	**VIOB**
average temperature coefficient		**4**	**<10**	**—**	**<10**	**µV/°C**	**DVIOB**
*input bias current		3	< 20	<10	< 10	µA	IB
average temperature coefficient		45	<120	—	<60	nA/°C	DIB
*input offset current		0.2	< 2.6	<1	< 2	µA	IIO
average temperature coefficient		2	< 20	—	< 10	nA/°C	DIIO
*open loop gain		65	> 52	> 56	> 56	dB	AOL
†power supply rejection ratio		70	> 55	> 60	> 60	dB	PSRR
♠ common mode rejection ratio		80	> 60	> 65	> 65	dB	CMRR
*supply current	no load, quiescent	4	< 5	< 5	< 5	mA	ICC
MISCELLANEOUS PERFORMANCE							
differential mode input	resistance	2	>0.5	>1	>1	MΩ	RIND
	capacitance	1	<2	<2	<2	pF	CIND
common mode input	resistance	1	>0.25	>0.5	>0.5	MΩ	RINC
	capacitance	1	<2	<2	<2	pF	CINC
output impedance	at DC	0.02	<0.3	<0.2	<0.2	Ω	RO
output voltage range	no load	±3.6	±2.8	±3	±3	V	VO
*output voltage range	RL=100Ω	±2.9	±2.5	±2.5	±2.5	V	VOL
common mode input range		±3.2	±2.5	±2.8	±2.8	V	CMIR
output current	(AJ/BJ/AI/BI/AL/AM)	±70	±30	±50	±50	mA	IO
output current	(A8/B8)	±70	±30	±35	±35	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out}	
(is short circuit protected to ground, maximum reliability maintained if I_{out} does not exceed 70mA, except A8D, B8D which should not exceed 35mA over the military temperature range)	
common mode input voltage	±V_{cc}
differential input voltage	10V
junction temperature	+175°
operating temperature range	
AI/AJ/BI/BJ:	-40°C to +85°C
A8/B8/AL/AM:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec

Miscellaneous Ratings

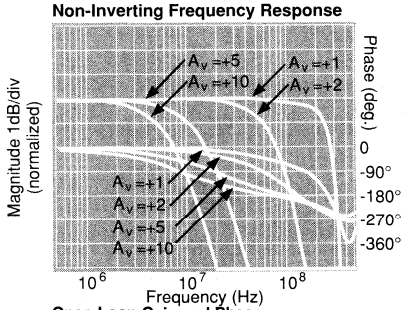
recommended gain range: ±1 to ±10

Notes:

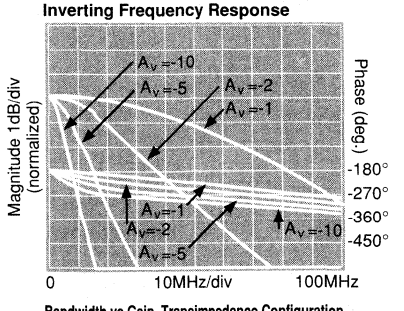
*	AI, AJ, BI, BJ	100% tested at +25°C, sample at +85°C.
†	AJ, BJ	Sample tested at +25°C.
†	AI, BI	100% tested at +25°C.
*	A8, B8	100% tested at +25°C, -55°C, +125°C.
†	A8, B8	100% tested at +25°C, sample at -55°C, +125°C.
♠	SMD	Sample tested at +25°C, – 55°C, +125°C.
*	AL, AM	100% wafer probed at +25°C to +25°C min/max specifications.

Typical Performance Characteristics (A_V=+1, V_{CC}=±5.0V, R_L = 100Ω, R_f=0Ω, unless specified)

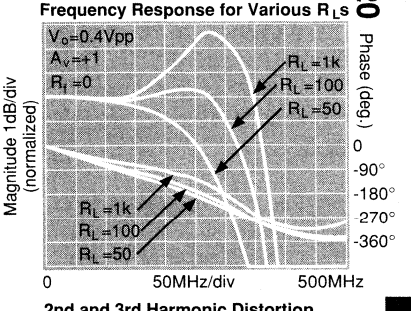
Non-Inverting Frequency Response



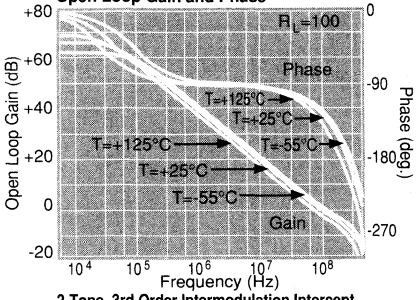
Inverting Frequency Response



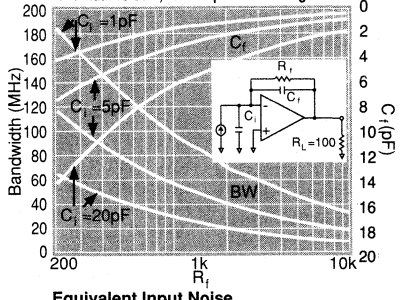
Frequency Response for Various R_Ls



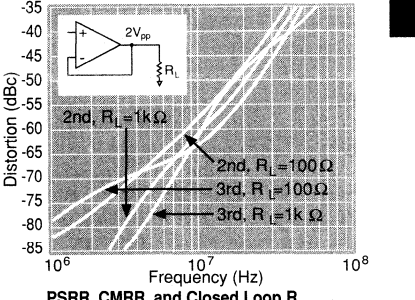
Open Loop Gain and Phase



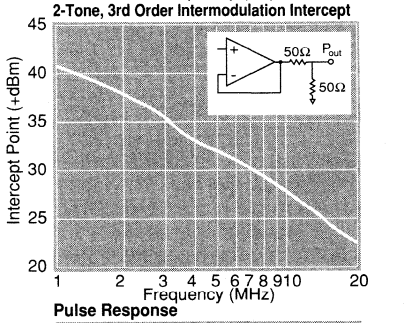
Bandwidth vs Gain, Transimpedance Configuration



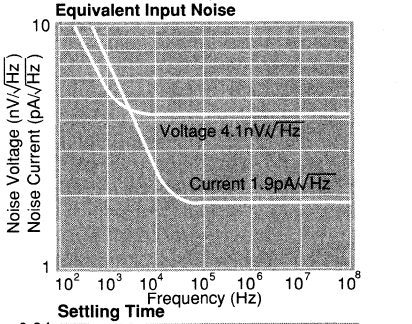
2nd and 3rd Harmonic Distortion



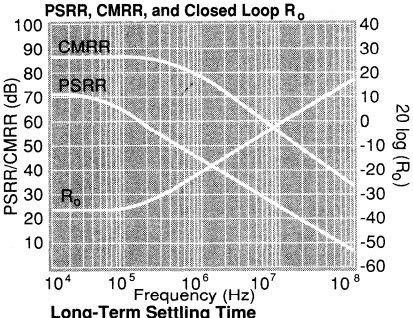
2-Tone, 3rd Order Intermodulation Intercept



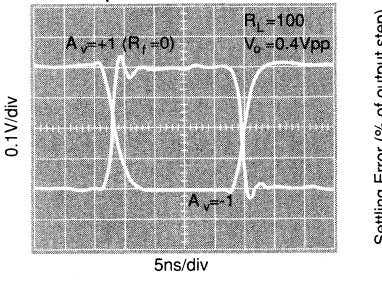
Equivalent Input Noise



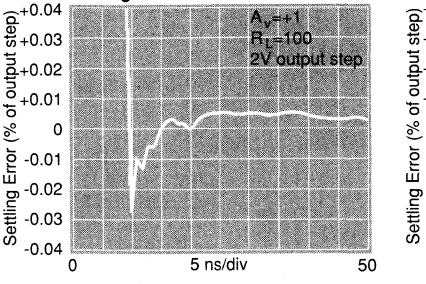
PSRR, CMRR, and Closed Loop R_o



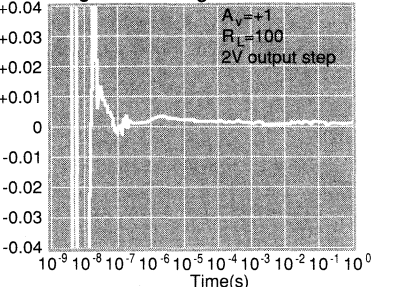
Pulse Response



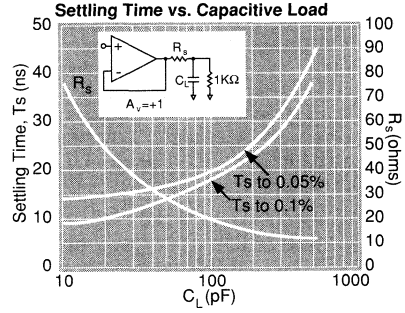
Settling Time



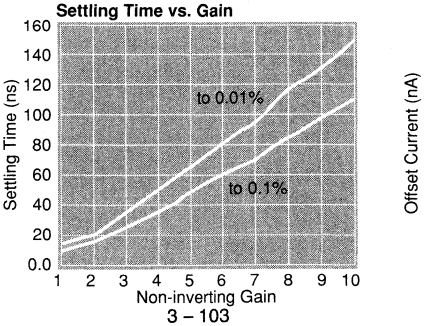
Long-Term Settling Time



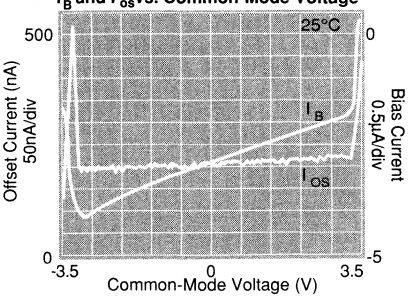
Settling Time vs. Capacitive Load



Settling Time vs. Gain



I_B and I_{os} vs. Common-Mode Voltage



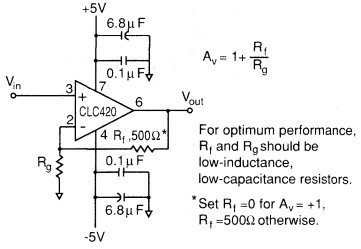


Figure 1: recommended non-inverting gain circuit

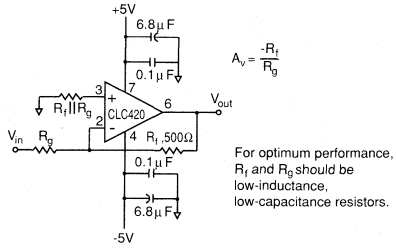


Figure 2: recommended inverting gain circuit

Description

The CLC420 is a high-speed, slew-boosted, voltage-feedback amplifier with unity-gain stability. These features along with matched inputs, low input bias and noise currents, and excellent CMRR render the CLC420 very attractive for active filters, differential amplifiers, log amplifiers, and transimpedance amplifiers.

DC accuracy

Unlike current-feedback amplifiers, voltage-feedback amplifiers have matched inputs. This means that the non-inverting and inverting input bias currents are well matched and track over temperature, etc. As a result, by matching the resistance looking out of the two inputs, these errors can be reduced to a small offset current term.

Gain bandwidth product

Since the CLC420 is a voltage-feedback op-amp, closed-loop bandwidth is approximately equal to the gain-bandwidth product (typically 100MHz) divided by the noise gain of the circuit (for noise gains greater than 5). At lower noise gains, higher-order amplifier poles contribute to higher closed-loop bandwidth. At low gains use the frequency response performance plots given in the data sheet.

Another point to remember is that the closed-loop bandwidth is determined by the noise gain, not the signal gain of the circuit. Noise gain is the reciprocal of the attenuation in the feedback network enclosing the op amp. For example, a CLC420 setup as a non-inverting amplifier with a closed-loop gain of +1 (a noise gain of 1) has a 300MHz bandwidth. When used as an inverting amplifier with a gain of -1 (a noise gain of 2), the bandwidth is less, typically only 100MHz.

Full-power bandwidth, and slew-rate

The CLC420 combines exceptional full-power bandwidths (40MHz, V_O=5Vpp, A_V=+1) and slew rates (1100V/µs, A_V=+1) with low (40mW) power consumption. These attractive results are achieved by using slew-boosting circuitry to keep the slew rates high while consuming very little power.

In non-slew boosted amplifiers, full-power bandwidth can be easily determined from slew-rate measurements, but in slew-boosted amplfiers, such as the CLC420, you can't. For this reason we provide data for both.

Slew rate is also different for inverting and non-inverting configurations. This occurs because common-mode signal voltages are present in non-inverting circuits but absent in inverting circuits. Once again data is provided for both.

Transimpedance amplifier circuits

Low inverting, input current noise (2pA/$\sqrt{Hz}$) makes the CLC420 ideal for high-sensitivity transimpedance amplifier circuits for applications such as pin-diode optical receivers, and detectors in receiver IFs. However, feedback resistors 4kΩ or greater are required if feedback resistor noise current is going to be less than the input current noise contribution of the op-amp.

With feedback resistors this large, shunt capacitance on the inverting input of the op-amp (from the pin-diode, etc.) will unacceptably degrade phase margin causing frequency response peaking or oscillations. A small-valued capacitor shunting the feedback resistor solves this problem (Note:This approach does not work for a current-feedback op-amp configured for transimpedance applications). To determine the value of this capacitor, refer to the "Transimpedance BW vs. R_f and C_i" plot.

For example, let's assume an optical transimpedance receiver is being developed. Total capacitance from the inverting input to ground, including the photodiode and strays is 5pF. A 5kΩ feedback resistor value has been determined to provide best dynamic range based on the responsivity of the photodiode and the range of incident optical powers, etc. From the "Transimpedance BW vs. R_f and C_i" plot, using C_i = 5pF it is determined from the two curves labeled C_i = 5pF, that C_f = 1.5pF provides optimal compensation (no more than 0.5dB frequency response peaking) and a -3dB bandwidth of approximately 27MHz.

Printed circuit layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the output and inverting input: Node connections should be small with minimal coupling to the ground plane.

Parasitic or load capacitance directly on the output (pin 6) will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before this capacitance, if present, effectively decouples this effect. The graphs on the preceding page, "Settling Time vs. C_L", illustrate the required resistor value and resulting performance vs. capacitance.

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC420 are available.

Comlinear Corporation

High-Gain, Voltage Feedback Op Amp

CLC422

APPLICATIONS:
- differential amplifier
- IF amplifier
- high-gain ampilfier
- high-precision applications
- instrumentation amplifier
- low voltage-noise amplifier

FEATURES (typical):
- 200MHz, – 3dB bandwidth (Av = + 40V/V)
- 2300V/μs slew rate
- 2.4nV/√Hz input voltage noise
- 0.8mV input offset voltage
- 4.5pA/√Hz input current noise
- 88dB common-mode rejection
- recommended gain range: ± 30 to ± 200V/V

DESCRIPTION

The CLC422 is a very high-speed operational amplifier employing a traditional voltage-feedback architecture and Comlinear's slew enhancement circuitry. Providing a 200MHz, −3dB bandwidth (Av= +40) and a 2300V/μs slew rate, the CLC422 is designed for applications requiring the amplification of very small, high-frequency signals. Since the CLC422 is not slew limited, there is little degradation in performance between small and large signal operation. At a non-inverting gain of 40, the CLC422 maintains a 200MHz, −3dB bandwidth for both 0.5Vpp and 5.0Vpp output voltages.

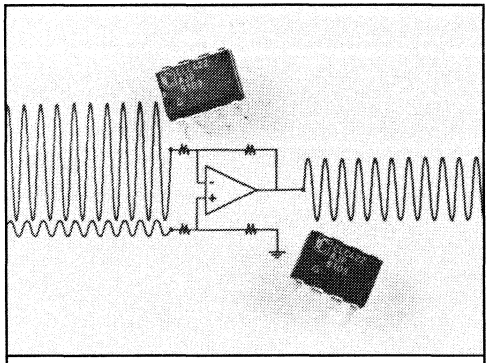
The CLC422 delivers precise performance with its excellent DC characteristics, such as a 0.8mV input offset voltage, 0.5μA input offset current and a 15μA input bias current. AC dynamic performance includes a rise/fall time of 2ns for both 0.5Vpp and 5.0Vpp output steps. Overshoot is typically 1% and settling time to 0.2% is 17ns.

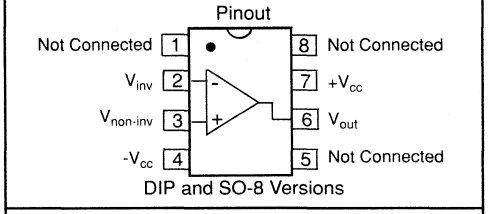
The CLC422 is the ideal amplifier to extract very small, high-frequency signals from a noisy environment due to its high common mode rejection, extremely low input-voltage noise and high gain range. All these characteristics contribute to an excellent signal-to-noise ratio.

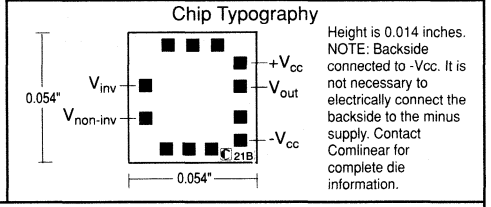
The high-gain CLC422 complements the unity-gain stable CLC420, both of which offer very high speeds using a traditional voltage-feedback architecture. The CLC422 is available in several versions to meet a variety of requirements.

CLC422AJP	– 40°C to + 85°C	8-pin plastic DIP
CLC422AJE	– 40°C to + 85°C	8-pin plastic SOIC
CLC422AIB	– 40°C to + 85°C	8-pin hermetic CERDIP
CLC422A8B	– 55°C to + 125°C	8-pin hermetic CERDIP, MIL-STD-883, Level B
CLC422ALC	– 55°C to + 125°C	dice
CLC422AMC	– 55°C to + 125°C	dice qualified to Method 5008, MIL-STD-883, Level B

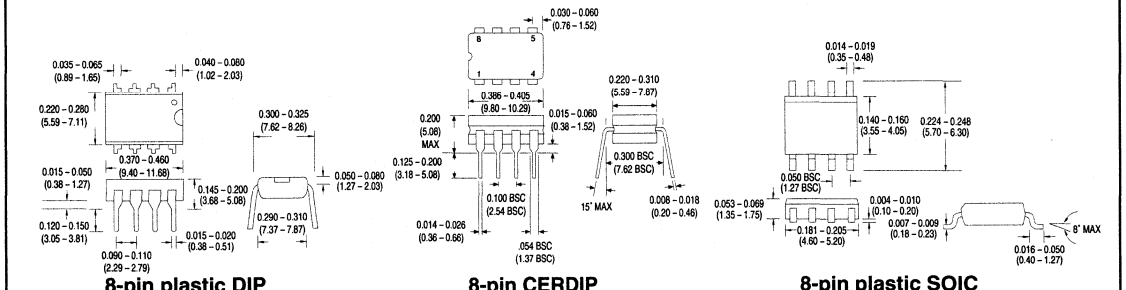
Contact factory for other packages. DESC SMD number, 5962-91666.







Package Dimensions



INTRODUCTORY INFORMATION: Specifications are based on the characterization of a limited number of devices.

Electrical Characteristics ($A_V = +40$; $\pm V_{cc} = \pm 5.0V$; $R_L = 100\Omega$; $R_f = 1500\Omega$; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC422AJ/AI	+25°C	−40°C	+25°C	+85°C		
Ambient Temperature	CLC422 A8/AM/AL	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
†−3dB bandwidth	$V_{out}<0.5V_{pp}$	200	>130	>130	>100	MHz	SSBW
	$V_{out}<5V_{pp}$	200	>130	>130	>100	MHz	LSBW
gain flatness	$V_{out}<0.5V_{pp}$						
† peaking	0.1MHz to 70MHz	0	<0.6	<0.6	<0.6	dB	GFPL
† peaking	70MHz to 200MHz	0	<3	<3	<3	dB	GFPH
† rolloff	0.1MHz to 35MHz	0.2	<1	<1	<1.2	dB	GFR
linear phase deviation	0.1 MHz to 70MHz	1	<2	<2	<2	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	2	<5	<5	<6	ns	TRS
	5V step	2	<5	<5	<6	ns	TRL
settling time to ±0.2%	2V step	17	<25	<25	<25	ns	TSS
overshoot	0.5V step	1	<15	<15	<15	%	OS
slew rate	5V step	2300	>1600	>1600	>1400	V/μs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	$2V_{pp}$, 20MHz	−40	<−30	<−33	<−33	dBc	HD2
†3rd harmonic distortion	$2V_{pp}$, 20MHz	−55	<−43	<−45	<−45	dBc	HD3
input noise							
voltage	1MHz to 200MHz	2.4	<3	<3	<3.4	nV/√Hz	VN
current	1MHz to 200MHz	4.5	<6.8	<6	<6	pA/√Hz	ICN
STATIC DC PERFORMANCE							
*input offset voltage		0.8	<2.8	<2	<3	mV	VIO
average temperature coefficient		2	<10	—	<10	μV/°C	DVIO
*input bias current		15	<65	<45	<45	μA	IB
average temperature coefficient		75	<200	—	<100	nA/°C	DIB
input offset current		0.5	<3.6	<2	<3	μA	IIO
average temperature coefficient		4	<20	—	<10	nA/°C	DIIO
*open loop gain		75	>64	>66	>66	dB	AOL
†power supply rejection ratio		78	>64	>66	>66	dB	PSRR
♠common mode rejection ratio		88	>66	>70	>66	dB	CMRR
*supply current	no load, quiescent	17	<20	<20	<24	mA	ICC
MISCELLANEOUS PERFORMANCE							
differential mode input	resistance	60	>15	>30	>30	kΩ	RIND
	capacitance	1	<2	<2	<2	pF	CIND
common mode input	resistance	700	>280	>350	>350	kΩ	RINC
	capacitance	1	<2	<2	<2	pF	CINC
output impedance	DC	0.05	<0.3	<0.2	<0.2	Ω	RO
output voltage range	no load	±3.8	±3.3	±3.5	±3.5	V	VO
output voltage range	$R_L = 100\Omega$	±3.6	±2.5	±3.1	±3.1	V	VOL
common mode input range		±3	±2.6	±2.6	±2.6	V	CMIR
output current	−40°C to 85°C	±70	±30	±50	±50	mA	IO
	−55°C to 125°C	±70	±25	±50	±50	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	$\pm V_{cc}$
differential input voltage	10V
junction temperature	+175°C
operating temperature range	
AI/AJ:	−40°C to +85°C
A8/AM/AL:	−55°C to +125°C
storage temperature range	−65°C to +150°C
lead solder duration (+300°C)	10 sec

Miscellaneous Ratings

recommended gain range ±30 to ±200V/V

NOTES:

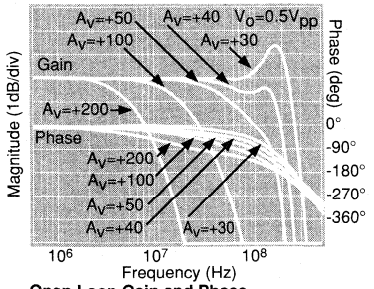
*	AI, AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested at +25°C, −55°C, +125°C.
†	A8	100% tested at +25°C, sample −55°C, +125°C.
*	AL, AM	100% wafer probe tested at +25°C to +25°C min/max specifications.
♠	SMD	Sample tested at +25°C, −55°C, +125°C.

Comlinear reserves the right to change specifications without notice.

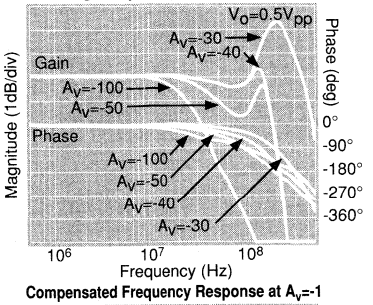
Typical Performance Characteristics

(T_A = +25 °C; A_V=+40; $\pm V_{CC}$= ±5.0V; R_L=100Ω; R_f=1500Ω)

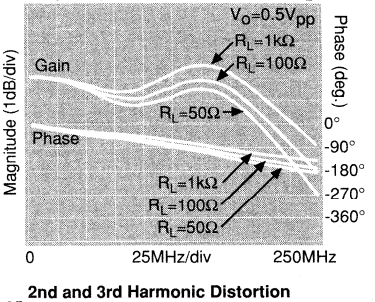
Non-Inverting Frequency Response



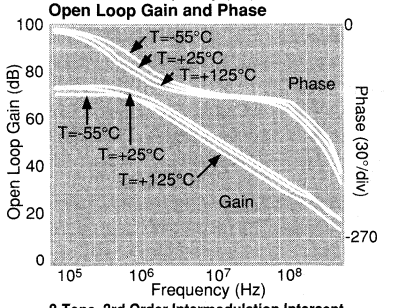
Inverting Frequency Response



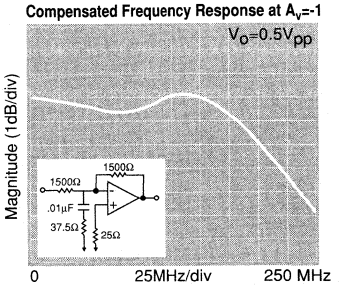
Frequency Response for Various R_Ls



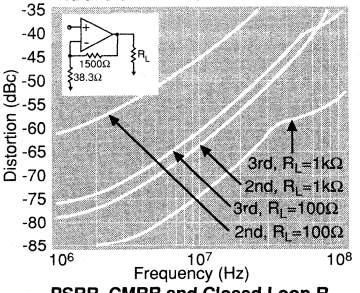
Open Loop Gain and Phase



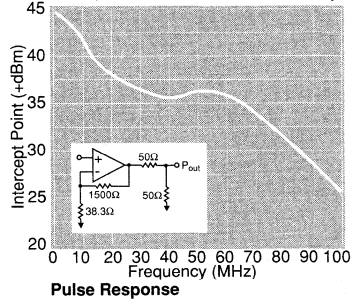
Compensated Frequency Response at A_v=-1



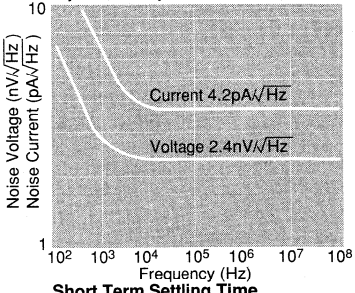
2nd and 3rd Harmonic Distortion



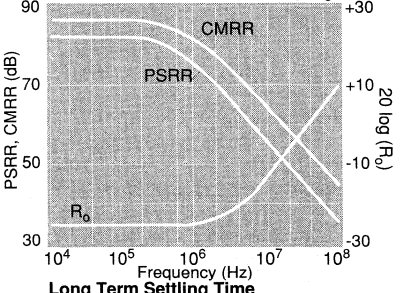
2-Tone, 3rd Order Intermodulation Intercept



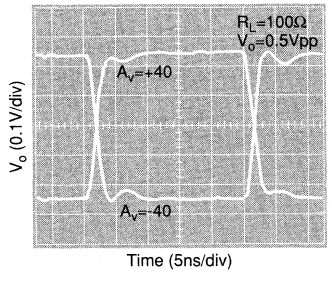
Equivalent Input Noise



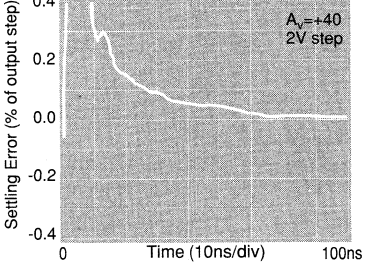
PSRR, CMRR and Closed Loop R_o



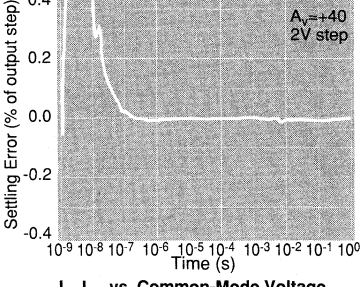
Pulse Response



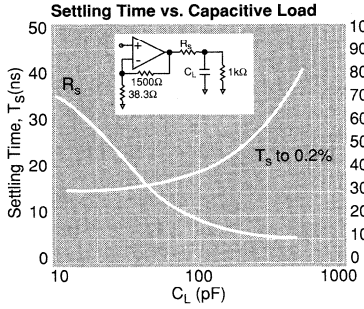
Short Term Settling Time



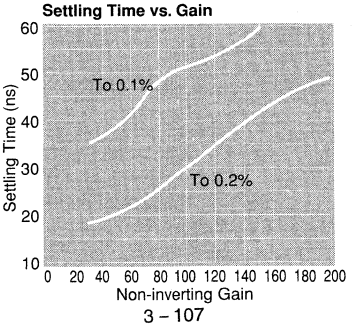
Long Term Settling Time



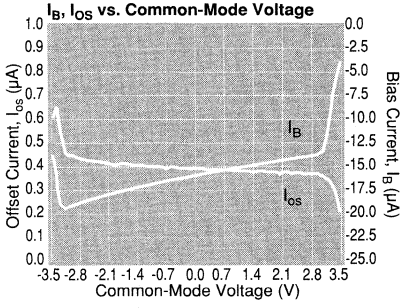
Settling Time vs. Capacitive Load

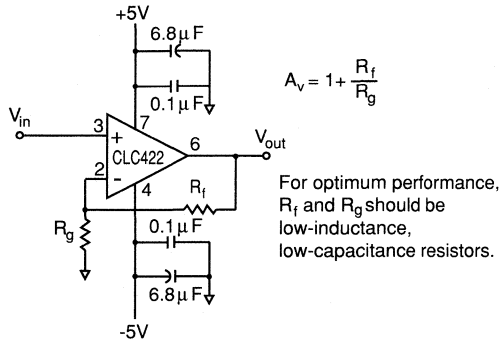


Settling Time vs. Gain

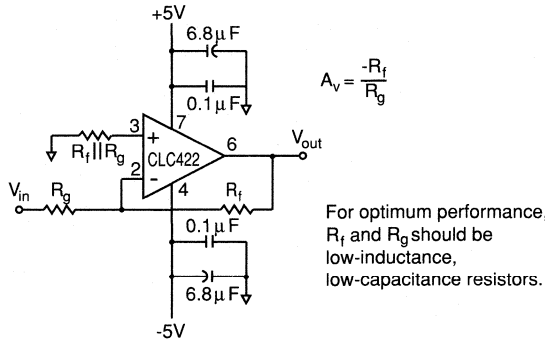


I_B, I_{OS} vs. Common-Mode Voltage





For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.



For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

Description
The CLC422 is a high-speed, slew-boosted, voltage-feedback amplifier designed for operation at gains of thirty or more. These features along with matched inputs, low input bias and noise currents, and excellent CMRR render the CLC422 very attractive for high-gain differential and instrumentation amplifiers, IF amplifiers, and applications requiring exceptional gain-bandwidth product.

DC accuracy
Unlike current-feedback amplifiers, voltage-feedback amplifiers have matched inputs. This means that the non-inverting and inverting input bias currents are well matched and track over temperature, etc. As a result, by matching the resistance looking out of the two inputs, these errors can be reduced to a small offset current term.

Gain bandwidth product
Since the CLC422 is a voltage-feedback op amp, closed-loop bandwidth is approximately equal to the gain-bandwidth product (typically 2GHz) divided by the noise gain (the reciprocal of the attenuation of the feedback network enclosing the op amp) of the circuit for noise gains greater than 100. At lower noise gains, higher-order amplifier poles contribute to higher closed-loop bandwidth. At lower gains use the frequency response performance plots given in the data sheet.

Full-power bandwidth, and slew-rate
Since the CLC422's slew-boosting circuitry prevents slew rate limiting, the full-power bandwidth is identical to the small-signal bandwidth. This device also sets a new standard for gain-bandwidth product in a monolithic voltage-feedback op amp (2GHz) while consuming a modest 170mW from ±5 volt supplies.

Low-gain voltage stages and transimpedance amplifiers
As a general rule, a CLC422 should only be used at gains greater than ±30. For lower gain stages and/or transimpedance amplifiers, other members of Comlinear's family of current and voltage-feedback amplifiers can provide superior performance.

However, in a few instances a CLC422 may provide somewhat better bandwidth or lower distortion at low frequencies (below 10MHz) than other amplifiers operating at comparable gains. To stabilize a CLC422 to gains lower than ±30 requires strict attention to distributed capacitances, layouts, and a variety of other details. Compensating at low gains adds extra components and requires more effort on the part of the design engineer. It is not recommended except for those well versed in RF layout and compensation of high frequency amplifiers. Techniques and tested performance of low gain compensation may be found in application note OA-17 for the CLC422. This is available from Comlinear.

Printed circuit layout
As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the output and inverting input: node connections should be small with minimal coupling to the ground plane.

Parasitic or load capacitance directly on the output (pin 6) will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before this capacitance, if present, effectively decouples this effect. The graphs on the preceding page, "Settling Time vs. Capacitive Load", illustrate the required resistor value and resulting performance vs. capacitance.

Evaluation Board
Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC422 are available.

Comlinear Corporation

Ultra Low Noise Wideband Op Amp

Preliminary **CLC425**

APPLICATIONS:

- instrumentation sense amplifiers
- ultrasound pre-amps
- magnetic tape & disk pre-amps
- photo-diode transimpedance amplifiers
- wide band active filters
- low noise figure RF amplifiers
- professional audio systems
- low-noise loop filters for PLLs

FEATURES (typical):

- 1.7GHz gain-bandwidth product
- 1.05nV/√Hz input voltage noise
- 1.6pA/√Hz input current noise
- 100μV input offset voltage, 2μV/°C drift
- 350V/μs slew rate
- 15mA to 5mA adjustable supply current
- gain range ±10 to ±1,000V/V
- evaluation board and simulation macromodel

DESCRIPTION

The CLC425 combines a wide bandwidth (**1.7GHz GBW**) with very low input noise (**1.05nV/√Hz, 1.6pA/√Hz**) and low dc errors (**100μV vos, 2μV/°C drift**) to provide a very precise, wide dynamic-range op amp offering closed-loop gains of ≥10.

Singularly suited for very wideband high-gain operation, the CLC425 employs a traditional voltage-feedback topology providing all the benefits of balanced inputs, such as low offsets and drifts, as well as a 96dB open-loop gain, a 100dB CMRR and a 95dB PSRR.

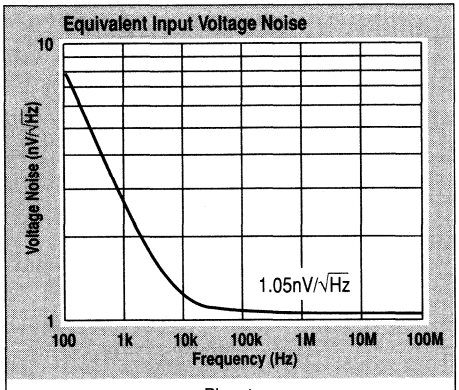
The CLC425 also offers great flexibility with its externally adjustable supply current, allowing designers to easily choose the optimum set of power, bandwidth, noise and distortion performance. Operating from ±5V power supplies, the CLC425 defaults to a 15mA quiescent current, or by adding one external resistor, the supply current can be adjusted to less than 5mA.

The CLC425's combination of ultra-low noise, wide gain-bandwidth, high slew rate and low dc errors will enable applications in areas such as medical diagnostic ultrasound, magnetic tape & disk storage, communications and opto-electronics to achieve maximum high-frequency signal-to-noise ratios.

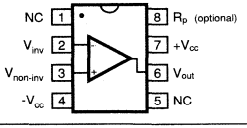
The CLC425 is available in the following versions.

CLC425AJP	-40°C to +85°C	8-pin PDIP
CLC425AJE	-40°C to +85°C	8-pin SOIC
CLC425AIB	-40°C to +85°C	8-pin CerDIP
CLC425A8B	-55°C to +125°C	8-pin CerDIP, MIL-STD-883 Level B
CLC425A8L-2	-55°C to +125°C	20-pin LCC, MIL-STD-883 Level B
CLC425ALC	-55°C to +125°C	dice
CLC425AMC	-55°C to +125°C	dice, MIL-STD-883 Level B

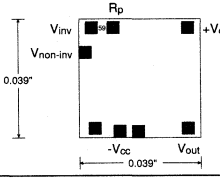
Contact factory for other packages and DESC SMD number.



Pinout

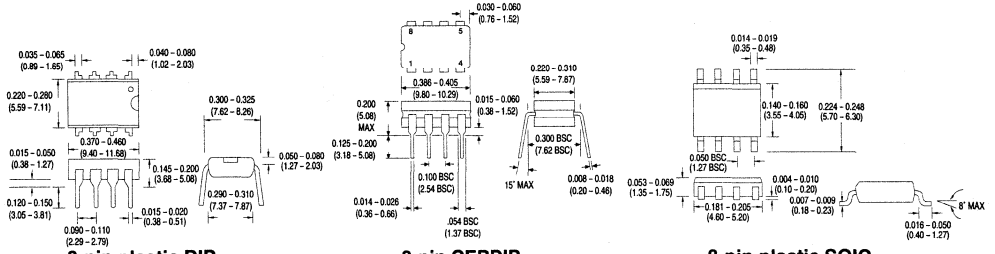


Chip Topography



Thickness is 0.014in. Note: Backside connected to $-V_{cc}$. It is not necessary to electrically connect the backside to the negative power supply. Contact factory for more information.

Package Dimensions



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CLC425 Electrical Characteristics (V_{cc} = ±5V; A_v = +20; R_f =499Ω; R_g = 26.1Ω; R_L = 100Ω; unless noted)

PARAMETERS	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC425 AJ/AI	+25°C	-40°C	+25°C	+85°C		
Ambient Temperature	CLC425 A8/AM/AL	+25°C	-55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
gain bandwidth product	V_{out} < 0.4V_{pp}	1.7				GHz	GBW
†-3dB bandwidth	V_{out} < 0.4V_{pp}	85	TBD	TBD	TBD	MHz	SSBW
	V_{out} < 5.0V_{pp}	TBD	TBD	TBD	TBD	MHz	LSBW
gain flatness	V_{out} < 0.4V_{pp}						
† peaking	DC to 30MHz	0.3	TBD	TBD	TBD	dB	GFP
† rolloff	DC to 30MHz	0.1	TBD	TBD	TBD	dB	GFR
linear phase deviation	DC to 30MHz	TBD	TBD	TBD	TBD	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	0.4V step	4.1	TBD	TBD	TBD	ns	TRS
settling time to 0.1%	2V step	22	TBD	TBD	TBD	ns	TSS
overshoot	0.4V step	5	TBD	TBD	TBD	%	OS
slew rate	2V step	350	TBD	TBD	TBD	V/µs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	1V_{pp}, 10MHz	- 50	TBD	TBD	TBD	dBc	HD2
†3rd harmonic distortion	1V_{pp}, 10MHz	- 80	TBD	TBD	TBD	dBc	HD3
3rd order intermodulation intercept	10MHz	35				dBm	IMD
1/f input voltage noise corner		500				Hz	1/F
equivalent noise input							
voltage	TBD to 100MHz	1.05	TBD	TBD	TBD	nV/√Hz	VN
current	TBD to 100MHz	1.6	TBD	TBD	TBD	pA/√Hz	ICN
noise floor	TBD to 100MHz	- 165	TBD	TBD	TBD	dBm_{1Hz}	SNF
integrated noise	TBD to 100MHz	12	TBD	TBD	TBD	µV	INV
STATIC DC PERFORMANCE							
open-loop gain	DC	96	77	86	86	dB	AOL
*input offset voltage		± 100	± 1000	± 800	± 1000	µV	VIO
average drift		± 2	8	—	4	µV/°C	DVIO
*input bias current		12	34	20	20	µA	IB
average drift		- 100	- 250	—	- 120	nA/°C	DIB
input offset current		± 0.2	3.4	2.0	2.0	µA	IIO
average drift		± 3	± 50	—	± 25	nA/°C	DIIO
†power supply rejection ratio	DC	95	82	88	88	dB	PSRR
♠common mode rejection ratio	DC	100	88	92	92	dB	CMRR
*supply current	R_L= ∞	15	18	16	16	mA	ICC
MISCELLANEOUS PERFORMANCE							
input resistance	common-mode	2	0.6	1.6	1.6	MΩ	RINC
	differential-mode	6	1	3	3	kΩ	RIND
input capacitance	common-mode	2.5	3	3	3	pF	CINC
output resistance	closed loop	5	50	10	10	mΩ	ROUT
output voltage range	R_L= ∞	± 3.8	± 3.5	± 3.7	± 3.7	V	VO
	R_L=100Ω	± 3.4	± 2.8	± 3.2	± 3.2	V	VOL
input voltage range	common mode	± 3.8	± 3.4	± 3.5	± 3.5	V	CMIR
output current	source -55°C/-40°C	90	60/70	70	70	mA	IOP
	sink -55°C/-40°C	90	40/55	55	55	mA	ION

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} short circuit protected to ground, however maximum reliabiliy is obtained if I_{out} does not exceed...	150mA
common-mode input voltage	±V_{cc}
differential input current diode protected	±25mA
maximum junction temperature	+175°C
operating temperature range	
AJ/AI	-40°C to +85°C
A8/ AM/AL:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

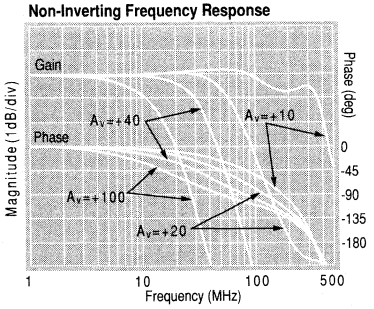
Recommended gain range ±10 to ±1,000V/V

Notes:

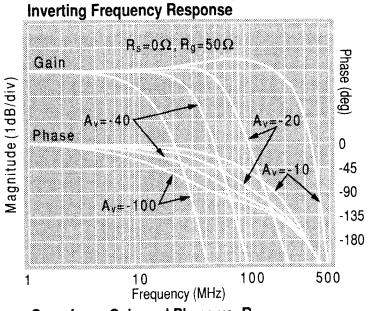
* AJ,AI : 100% tested at +25°C, sample at +85°C.
† AJ : Sample tested at +25°C.
† AI : 100% tested at +25°C.
* A8 : 100% tested at +25°C, -55°C, +125°C.
† A8 : 100% tested at +25°C, sample at -55°C, +125°C
* AL, AM : 100% wafer probed +25°C to +25°C min/max specs.
♠ SMD : Sample tested at +25°C, -55°C and +125°C.

CLC425 Typical Performance (T_A=25°C, V_{cc}=±5V, R_p=26.1Ω, R_L=499Ω, R_f=100Ω, unless noted)

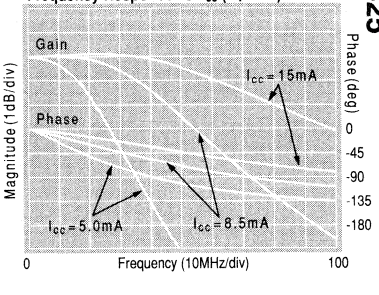
Non-Inverting Frequency Response



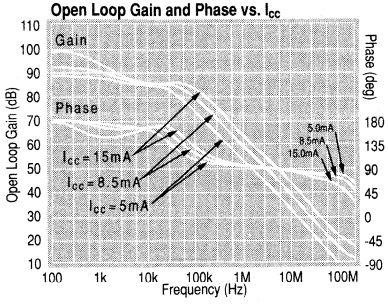
Inverting Frequency Response



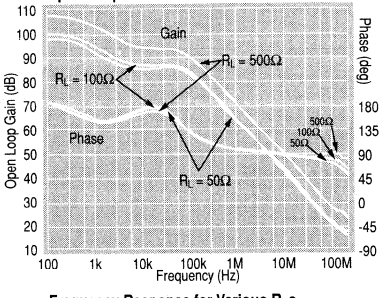
Frequency Response vs. I_{cc} (A_V=+20)



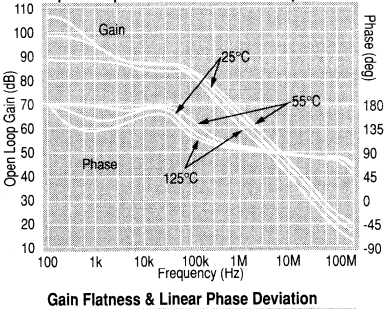
Open Loop Gain and Phase vs. I_{cc}



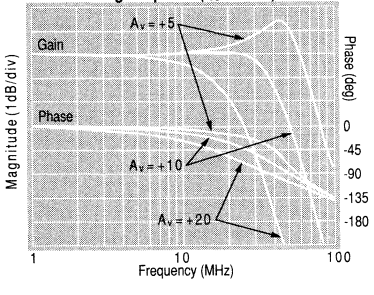
Open Loop Gain and Phase vs. R_L



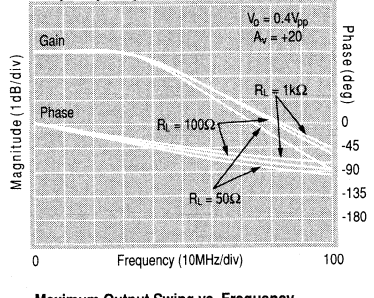
Open Loop Gain and Phase vs. Temp



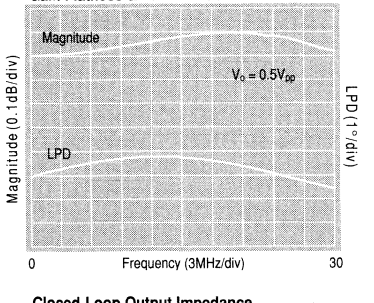
Non-Inverting Response (I_{CC}=5.0mA)



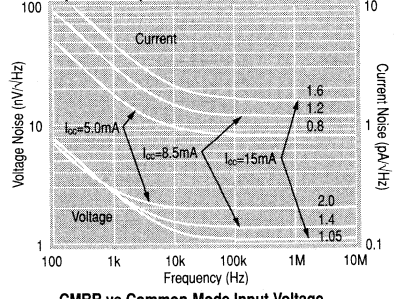
Frequency Response for Various R_Ls



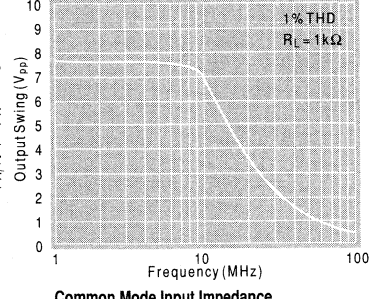
Gain Flatness & Linear Phase Deviation



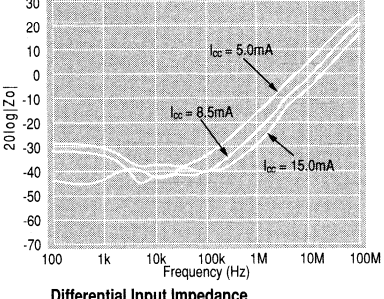
Equivalent Input Noise



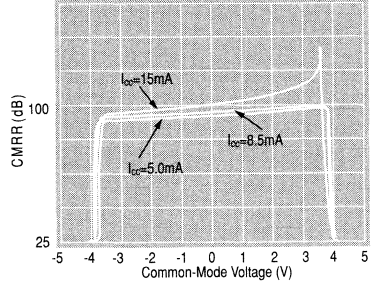
Maximum Output Swing vs. Frequency



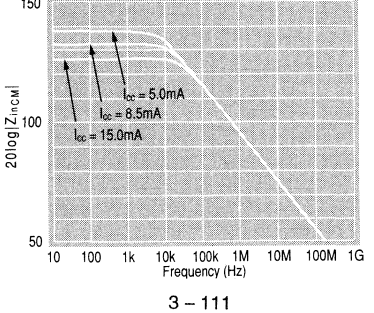
Closed-Loop Output Impedance



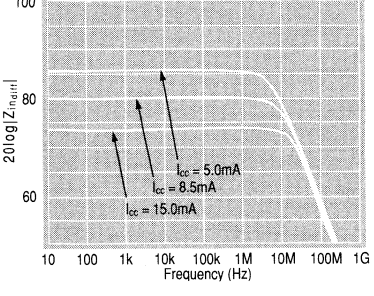
CMRR vs Common-Mode Input Voltage



Common Mode Input Impedance

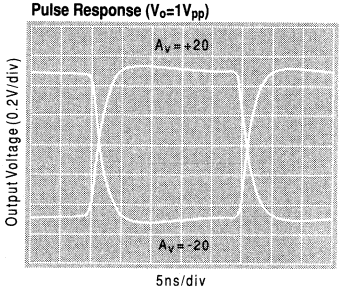


Differential Input Impedance

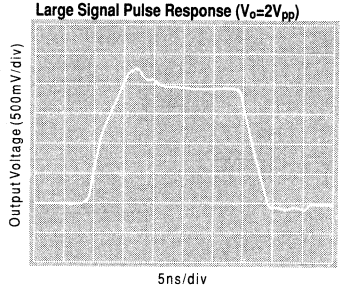


CLC425 Typical Performance (T_A=25°C, V_{cc}=±5V, R_g=26.1Ω, R_f=499Ω, R_L=100Ω, unless noted)

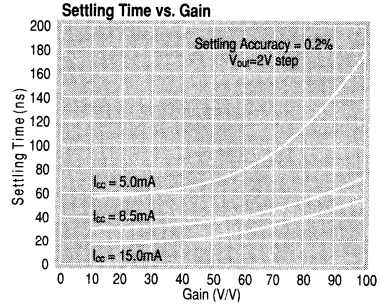
Pulse Response (V_O=1V_{pp})



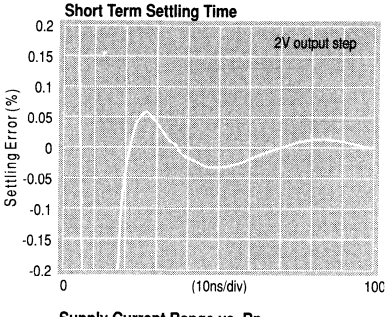
Large Signal Pulse Response (V_O=2V_{pp})



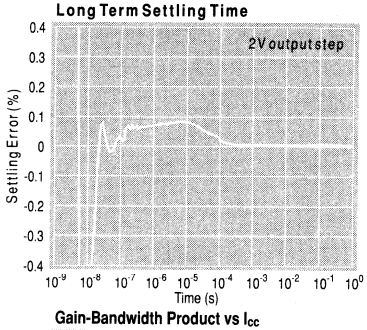
Settling Time vs. Gain



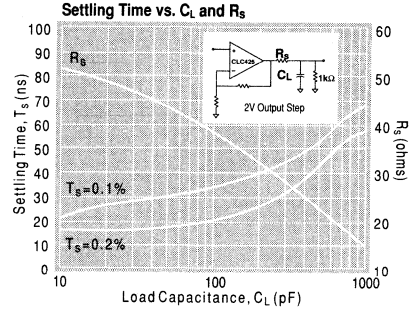
Short Term Settling Time



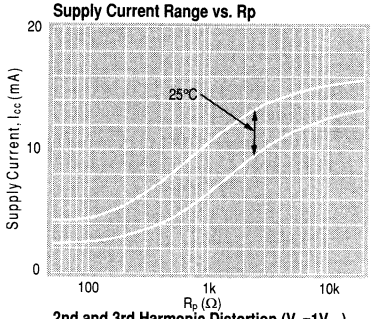
Long Term Settling Time



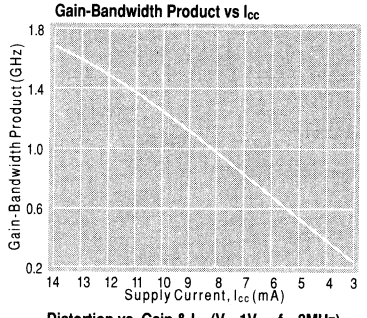
Settling Time vs. C_L and R_S



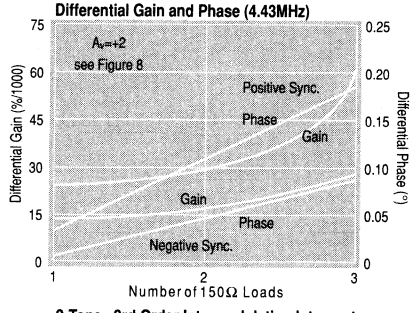
Supply Current Range vs. Rp



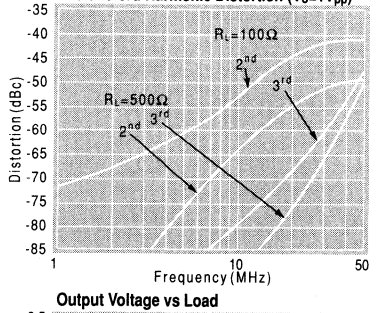
Gain-Bandwidth Product vs I_{cc}



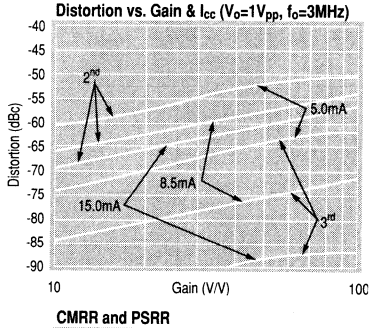
Differential Gain and Phase (4.43MHz)



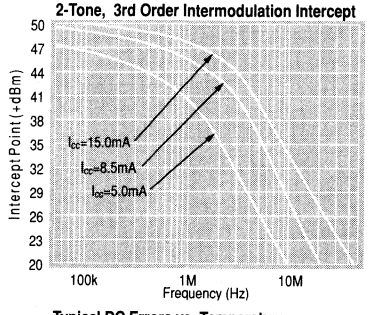
2nd and 3rd Harmonic Distortion (V_O=1V_{pp})



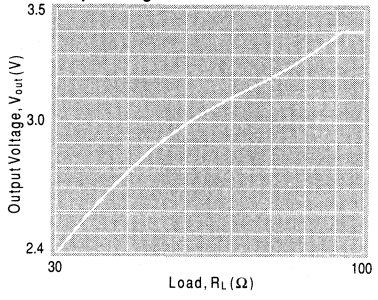
Distortion vs. Gain & I_{cc} (V_O=1V_{pp}, f_O=3MHz)



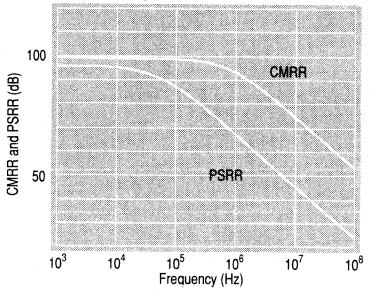
2-Tone, 3rd Order Intermodulation Intercept



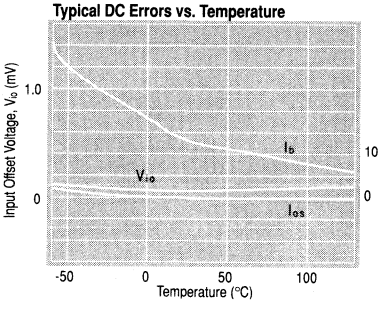
Output Voltage vs Load



CMRR and PSRR



Typical DC Errors vs. Temperature



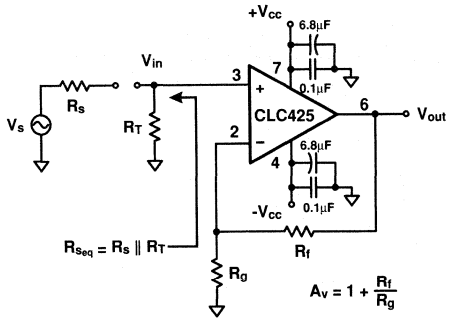


Figure 1: Non-inverting Amplifier Configuration

Introduction

The CLC425 is a very wide gain-bandwidth, ultra-low noise voltage feedback operational amplifier which enables application areas such as medical diagnostic ultrasound, magnetic tape & disk storage and fiber-optics to achieve maximum high-frequency signal-to-noise ratios. The set of characteristic plots located in the "Typical Performance" section illustrates many of the performance trade-offs. The following discussion will enable the proper selection of external components in order to achieve optimum device performance.

Bias Current Cancellation

In order to cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain-setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in Figure 1. Combining this constraint with the non-inverting gain equation also seen in Figure 1, allows both R_f and R_g to be determined explicitly from the following equations: $R_f=A_vR_{seq}$ and $R_g=R_f/(A_v-1)$. When driven from a 0Ω source, such as that from the output of an op amp, the non-inverting input of the CLC425 should be isolated with at least a 25Ω series resistor.

As seen in Figure 2, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input ($R_f||(R_g+R_s)$). R_b is recommended to be no less than 25Ω for best CLC425 performance. The additional noise contribution of R_b can be minimized through the use of a shunt capacitor.

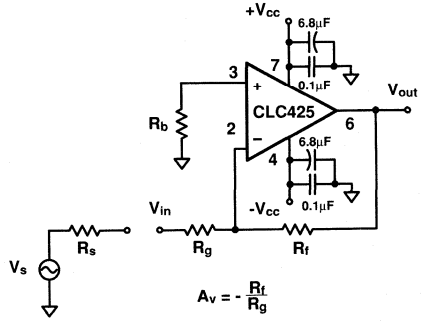
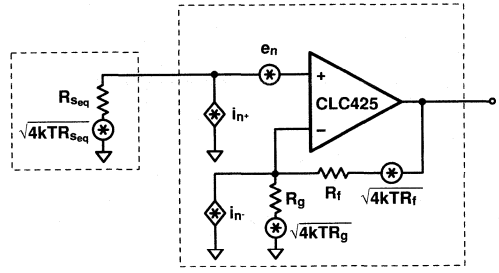


Figure 2: Inverting Amplifier Configuration

Total Input Noise vs. Source Resistance

In order to determine maximum signal-to-noise ratios from the CLC425, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary.

Figure 3 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n=i_{n+}=i_{n-}$) sources, there also exists thermal voltage noise ($e_t=\sqrt{4kTR}$) associated with each of the external resistors. Equation 1 provides the general form for total equivalent input voltage noise density (e_{ni}). Equation 2 is a simplification of Equation 1 that assumes $R_f||R_g = R_{seq}$ for



$$4kT = 16.4e-21 \; Joules \; @ \; 25°C$$

Figure 3: Non-inverting Amplifer Noise Model

$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+}R_{s_{eq}}\right)^2 + 4kTR_{s_{eq}} + \left(i_{n-}\left(R_f \,||\, R_g\right)\right)^2 + 4kT\left(R_f \,||\, R_g\right)}$$

Equation 1: General Noise Equation

bias current cancellation. Figure 4 illustrates the equivalent noise model using this assumption. Figure 5 is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing voltage noise sources of Equation 2 shown. This plot gives the expected e_{ni} for a given R_{seq} which assumes $R_f||R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is $e_{ni}*A_v$.

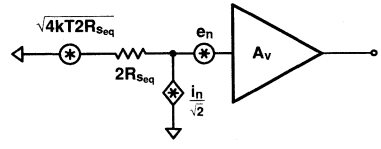


Figure 4: Noise Model with $R_f||R_g = R_{seq}$

$$e_{ni} = \sqrt{e_n^2 + 2\left(i_n R_{s_{eq}}\right)^2 + 4kT\left(2R_{s_{eq}}\right)}$$

Equation 2: Noise Equation with $R_f||R_g = R_{seq}$

As seen in Figure 5, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 33.5Ω. Between 33.5Ω and 6.43kΩ, e_{ni} is dominated by the thermal noise ($e_t=\sqrt{4kTR_{seq}}$) of the external resistors. Above 6.43kΩ, e_{ni} is dominated by the amplifier's current noise ($\sqrt{2}i_nR_{seq}$). The point at which the CLC425's voltage noise and current noise contribute equally occurs for R_{seq}=464Ω (i.e. $e_n/\sqrt{2}i_n$). As an example, configured with a gain of +20V/V giving a -3dB of 90MHz and driven from an R_{seq}=25Ω, the CLC425 produces a total equivalent input noise voltage ($e_{ni}*\sqrt{1.57*90MHz}$) of 16.5μV_{rms}.

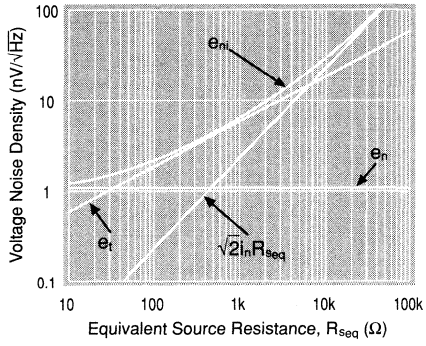


Figure 5: Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then $R_f||R_g$ does not need to equal R_{seq}. In this case, according to Equation 1, $R_f||R_g$ should be as low as possible in order to minimize noise. Results similar to Equation 1 are obtained for the inverting configuration of Figure 2 if R_{seq} is replaced by R_b and R_g is replaced by R_g+R_s. With these substitutions, Equation 1 will yield an e_{ni} refered to the non-inverting input. Refering e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains.

Noise Figure

Noise Figure (NF) can be defined as the ratio of the total output noise power (e_{no}) to that portion of output noise power caused by the source resistance (e_t*A_v) and is so expressed in Equation 3. This definition assumes an unterminated source and that the parallel combination of R_f and R_g is chosen to equal to R_s for bias current cancellation. The curve labeled "Unterminated" in Figure 6 is a plot of NF vs. R_s and for a 50Ω source the CLC425's NF is 5.26dB.

$$NF = 10\log\left(\frac{e_n^2 + 2(i_nR_s)^2 + 4kT(2R_s)}{4kTR_s}\right)$$

Equation 3: Noise Figure Equation for Unterminated Source

Adding a matching termination resistor (R_T, Figure 1) to the CLC425's input will result in a higher measured Noise Figure as seen by the curve labeled "Terminated". Noise Figure can also be defined as the ratio of the source's SNR to the amplifier's SNR. Therefore, even though the thermal

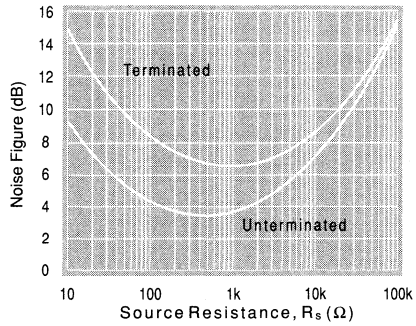


Figure 6: Noise Figure vs. Source Resistance

noise power contribution of all the external resistors is diminished by ½ (i.e. $R_f||R_g = R_s||R_T = ½R_s$), the addition of the matching termination resistor as a part of the amplifier also cuts the input signal amplitude by ½ such that the amplifier's SNR is reduced and the resulting Noise Figure is higher as shown in the plot. From the curve labeled "Terminated", the CLC425 configured with a 50Ω matching termination resistor (R_T) driven from the same 50Ω (R_s) source used above, yields a NF of 9.72dB. As seen from the two curves, the difference is negligible with very high source resistances where the current noise of the amplifier becomes the dominant factor. For more information regarding Noise Figure, see OA-11.

Supply Current Adjustment

The CLC425's supply current can be externally adjusted downward from its nominal value by adding an optional resistor (R_p) between pin 8 and the negative supply as shown in Figure 7. Several of the plots found within the plot pages demonstrate the CLC425's behavior at different supply currents. The plot labeled "I_{cc} vs. R_p" provides the means for selecting R_p and shows the result of standard IC process variation which is bounded by the 25°C curve.

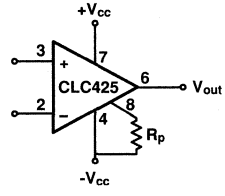


Figure 7: External Supply Current Adjustment

Non-Inverting Gains Less Than 10V/V

Using the CLC425 at lower non-inverting gains requires external compensation such as the shunt compensation as shown in Figure 8. The quiescent supply current must also be reduced to 5mA with R_p for stability. The compensation capacitors are chosen to reduce frequency response peaking to less than 1dB. The plot in the "Typical Performance" section labeled "Differential Gain and Phase" shows the video performance of the CLC425 with this compensation circuitry.

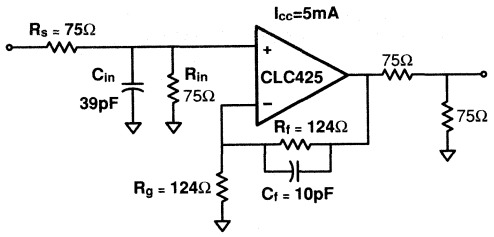


Figure 8: External Shunt Compensation

Inverting Gains Less Than 10V/V

The lag compensation of Figure 9 will achieve stability for lower gains. Placing the network between the two input terminals does not affect the closed-loop nor noise gain, but is best used for the invering configuration because of its affect on the non-inverting input impedance.

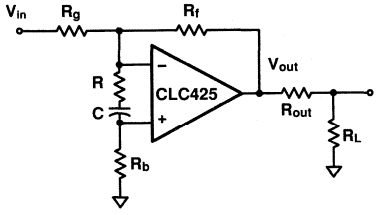


Figure 9: External Lag Compensation

Single-Supply Operation

The CLC425 can be operated with single power supply as shown iin Figure 10. Both the input and output are capacitively coupled to set the dc operating point.

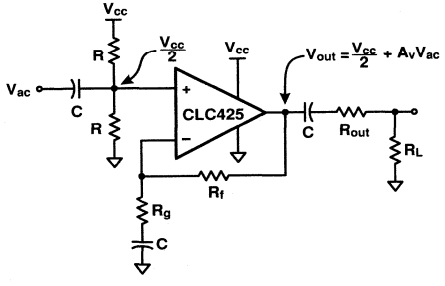


Figure 10: Single Supply Operation

Low Noise Transimpedance Amplifier

The circuit of Figure 11 implements a low-noise transimpedance amplifier commonly used with photodiodes. The transimpedance gain is set by R_f. The simulated frequency response is shown in Figure 12 and shows the influence C_f has over gain flatness. Equation 4 provides the total input current noise density (i_{ni}) equation for the basic transimpedance configuration and is plotted against feedback resistance (R_f) showing all contributing noise sources in Figure 13. This plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_f). The total equivalent output voltage noise density (e_{no}) is $i_{ni}*R_f$.

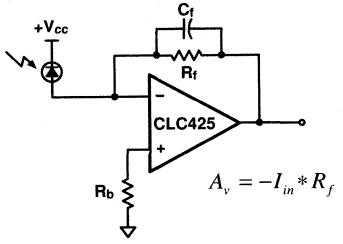


Figure 11: Transimpedance Amplifier Configuration

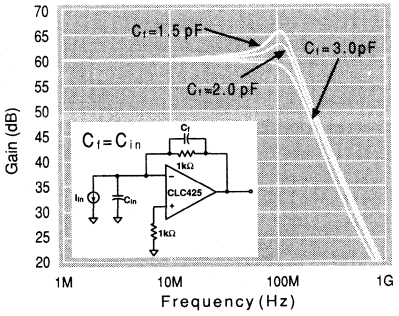


Figure 12: Transimpedance Amplifier Frequency Response

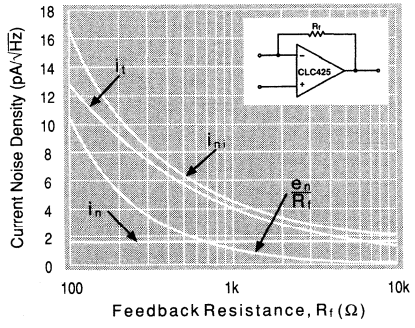


Figure 13: Current Noise Density vs. Feedback Resistance

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}}$$

Equation 4: Total Equivalent Input Refered Current Noise Density

Very Low Noise Figure Amplifier

The circuit of Figure 14 implements a very low Noise Figure amplifier using a step-up transformer combined with a CLC425 and a CLC404. The circuit is configured with a gain of 35.6dB. The circuit achieves measured Noise Figures of less than 2.5dB in the 10-40MHz region. 3rd order intercepts exceed +30dBm for frequencies less than 40MHz and gain flatness of 0.5dB is measured in the 1-50MHz pass bands. Application Note OA-14 provides greater detail on these low Noise Figure techniques.

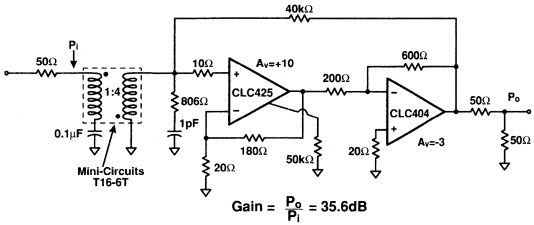
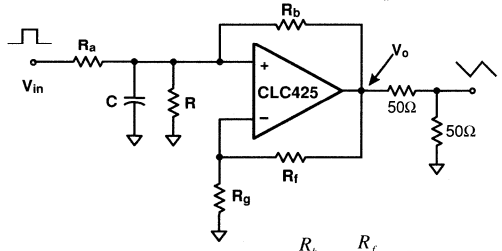


Figure 14: Very Low Noise Figure Amplifier

Low Noise Integrator

The CLC425 implements a deBoo integrator shown in Figure 15. Integration linearity is maintained through positive feedback. The CLC425's low input offset voltage and matched inputs allowing bias current cancellation provide for very precise integration. Stability is maintained through the constraint on the circuit elements.

$$V_o \cong V_{in}\frac{K_o}{sR_aC}; \qquad K_o = 1+\frac{R_f}{R_g}$$



$$\frac{R_b}{R_a \| R} \geq \frac{R_f}{R_g}, \quad R >> R_a$$

Figure 15: Low Noise Integrator

High-Gain Sallen-Key Active Filters

The CLC425 is well suited for high-gain Sallen-Key type of active filters. Figure 16 shows the 2nd order Sallen-Key low pass filter topology. Using component predistortion methods as discussed in OA-21 enables the proper selection of components for these high-frequency filters.

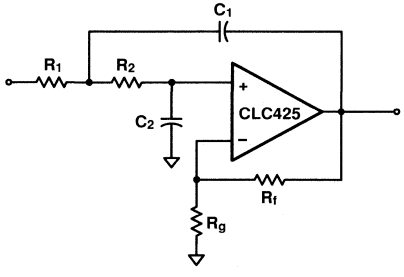
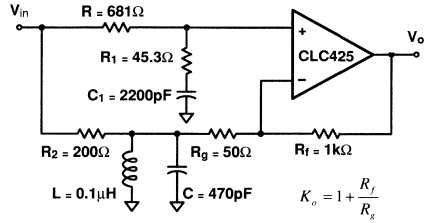


Figure 16: Sallen-Key Active Filter Topology

Low Noise Magnetic Media Equalizer

The CLC425 implements a high-performance low-noise equalizer for such applications as magnetic tape channels as shown in Figure 17. The circuit combines an integrator with a bandpass filter to produce the low-noise equalization. The circuit's simulated frequency response is illustrated in Figure 18.



$$\frac{V_o}{V_{in}} = K_o\left(\frac{sC_1R_1+1}{sC_1(R_1+R)+1} - \left(\frac{R_f}{R_f+R_g}\right)\frac{sLR_g}{s^2LCR_2R_g + sL(R_2+R_g)+R_2R_g}\right)$$

Figure 17: Low Noise Magnetic Media Equalizer

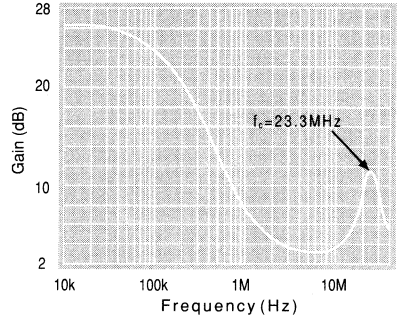


Figure 18: Equalizer Frequency Response

Low-Noise Phase-Locked Loop Filter

The CLC425 is extremely useful as a Phase-Locked Loop filter in such applications as frequency synthesizers and data synchronizers. The circuit of Figure 19 implements one possible PLL filter with the CLC425.

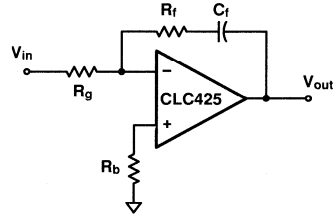


Figure 19: Phased-Locked Loop Filter

Decreasing the Input Noise Voltage

The input noise voltage of the CLC425 can be reduced from its already low $1.05nV/\sqrt{Hz}$ by slightly increasing the supply current. Using a 50kΩ resistor to ground on pin 8, as shown in the circuit of Figure 14, will increase the quiescent current to ≈17mA and reduce the input noise voltage to < $0.95nV/\sqrt{Hz}$.

Printed Circuit Board Layout

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillation, see OA-15 for more information. Comlinear suggests the 730013 Evaluation Board both as a guide for high-frequency layout and as an aid in device testing and characterization.

Comlinear Corporation

Quad, Wideband Monolithic Op Amp

CLC430

APPLICATIONS:
- video distribution
- multiple-line driver
- analog bus driver
- video signal multiplexing
- DAC output buffer
- CCD amplifer

FEATURES (typical):
- 55MHz small-signal bandwidth ($4V_{pp}$)
- 2000 V/µs slew rate
- ± 5V to ± 15V supplies
- 100ns disable to high-impedance output
- 85mA continuous output current
- 0.02%/0.04° differential gain/phase
- high common mode input voltage

DESCRIPTION:

The CLC 430 is a high-speed, monolithic operational amplifier employing Comlinear's proprietary current feedback architecture. Equipped with a very fast disable/enable feature, the CLC430 is designed specifically for video switching and distribution systems. The CLC430's high-speed operation includes a 55MHz small signal bandwidth (4Vpp) and a 2000V/µs slew rate while requiring only 11mA quiescent current. Since the CLC430 is designed to operate over a wide range of supply voltages, there is little degradation in performance between ±5V and ±15V operation.

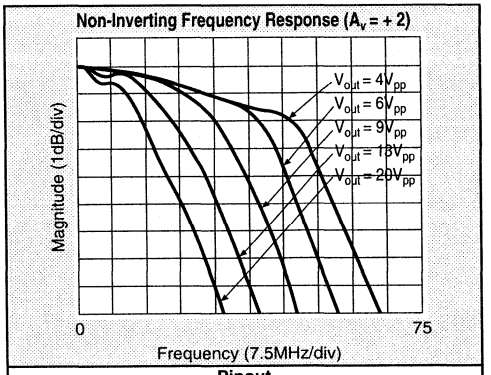
The CLC430 is designed to drive video speed signals through multiple 75Ω or 50Ω channels while maintaining excellent differential gain and phase performance. The disable/enable feature allows the CLC430 to be used in video switching and multiplexing applications with its quick turn-off (100ns) and turn-on (200ns). Switched into disable mode, the CLC430 provides a high impedance output while drawing only 1.5mA supply current. Multiplexing video signals onto an analog bus can easily be achieved by combining parallel CLC430s to form a common output. And since "break before make" is guaranteed, the disable pins of the paralleled combination can be driven with the same signal source.

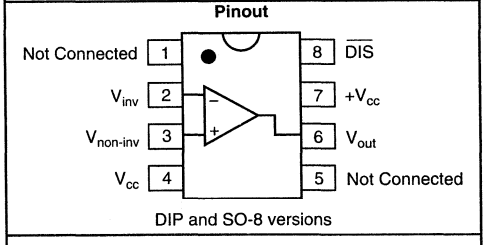
Applications with large DC components, such as CCD amplifiers will enjoy the CLC430's high common mode input range and wide signal swing.

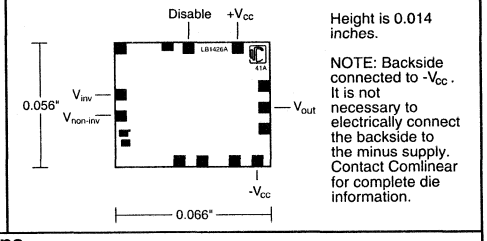
The CLC430 is available in several versions to meet a variety of requirements.

CLC430AJP	−40°C to +85°C	8-pin plastic DIP
CLC430AJE	−40°C to +85°C	8-pin plastic SOIC
CLC430AIB	−40°C to +85°C	8-pin hermetic CERDIP
CLC430A8B	−55°C to +125°C	8-pin hermetic CERDIP MIL-STD-883, Level B
CLC430ALC	−55°C to +125°C	dice
CLC430AMC	−55°C to +125°C	dice qualified to Method 5008, MIL- STD-883, Level B

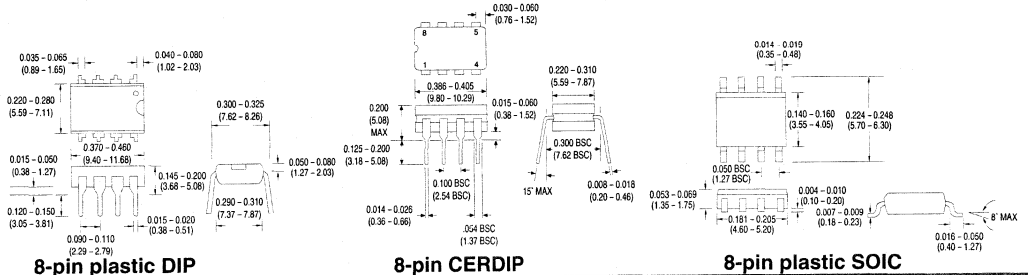
Contact factory for other packages. DESC SMD number 5962-92030.







Package Dimensions



Electrical Characteristics (A_V=+2; $\pm V_{cc}$=±15V; R_L = 100Ω; R_f = 750Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC430AJ/AI	+25°C	−40°C	+25°C	+85°C		
Ambient Temperature	CLC430A8/AM/AL	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN PERFORMANCE							
† −3dB bandwidth	V_{out} <4V_{pp}(note 1)	55	30	30	25	MHz	SSBW
	V_{out} <10V_{pp}	27	20	20	16	MHz	LSBW
gain flatness[2]	V_{out} <4V_{pp}(note 1)						
† peaking	DC to 10MHz	0.2	0.5	0.5	0.6	dB	GFPL
† peaking	DC to 10MHz	0.2	0.5	0.5	0.6	dB	GFPH
† rolloff	DC to 20MHz	0.5	1.5	1.5	1.8	dB	GFR
linear phase deviation	DC to 20MHZ	0.3	1.8	1.8	2.3	°	LPD
diff. gain pos/neg sync	4.43MHz,150Ω load	0.02	0.07/0.04	0.07/0.04	0.10/0.05	%	DG
diff. phase pos/neg sync	4.43MHz,150Ω load	0.04	0.20/0.07	0.20/0.07	0.25/0.15	°	DP
TIME DOMAIN RESPONSE							
rise and fall time	10V step	10	16	14	16	ns	TRL
settling time to 0.05%	2V step	35	50	50	60	ns	TS
overshoot	2V step, 1ns rise/fall	0	8	5	8	%	OS
slew rate	V_{out} = ±10V	2000	1400	1500	1400	V/µs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	2V_{pp}, 10MHz	40	34	34	34	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 10MHz	53	43	46	46	dBc	HD3
equivalent noise input							
voltage	>1MHz	3	3.5	3.5	4.0	nV/√Hz	VN
inverting current	>1MHz	15	21	18	21	pA/√Hz	ICI
non-inverting current	>1MHz	4	7	6	7	pA/√Hz	ICN
noise floor	>1MHz	−151	−148	−148	−148	dBm_{1Hz}	SNF
integrated input noise	1MHz to 100MHz	63	90	90	90	µV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		±2	±11	±7.5	±11	mV	VIO
average temperature coefficient		±25	+50	—	+50	µV/°C	DVIO
*input bias current	non-inverting	±3	±22	±14	+10	µA	IBN
average temperature coefficient		±10	±160	—	±80	nA/°C	DIBN
*input bias current	inverting	±3	±18	±14	±12	µA	IBI
average temperature coefficient		±10	±100	—	±50	nA°C	DIBI
•power supply rejection ratio		62	53	56	53	dB	PSRR
♠common mode rejection ratio		62	52	54	52	dB	CMRR
*supply current	no load	11	15	12	12	mA	ICC
supply current	disabled	1.5	2.5	2.0	2.5	mA	ICCD
SWITCHING PERFORMANCE (break before make is guaranteed)							
turn on time		200	300	300	350	ns	TON
turn off time		100	200	200	200	ns	TOFF
off isolation	10MHz	59	56	56	56	dB	ISO
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		8000	1500	3000	5000	kΩ	RIN
non-inverting input capacitance		0.5	1.0	1.0	1.0	pF	CIN
output voltage range	R_L=100Ω	±8	±6	±6	±4	V	VOL
output voltage range	no load	±13	±12	±12	±12	V	VO
common mode input range		±11	±10	±10	±10	V	CMIR
output current		±85	±60	±60	±45	mA	IO

Absolute Maximum Ratings

V_{cc}	±18V
I_{out} output is short circuit protected to ground, however, maximum reliability is obtained if I_{out} does not exceed...	125mA
common mode input voltage	$\pm V_{cc}$
differential input voltage	±15V
maximum junction temperature	+175°C
operating temperature range	
AJ/AI:	−40°C to +85°C
A8/AL/AM:	−55°C to +125°C
storage temperature range	−65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

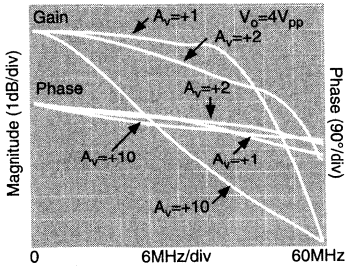
recommended gain range: ±1 to ±10

Notes:

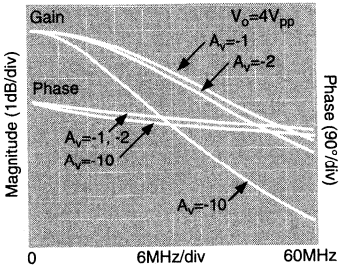
*	AI, AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested +25°C, −55°C, +125°C.
†	A8	100% tested +25°C, sample at −55°C, +125°C.
*	AL, AM	100% wafer probed at +25°C to +25°C min/max specifications.
♠	SMD	Sample tested at +25°C, −55°C, +125°C.
note 1:		Specification is guaranteed for V_{out} = 4V_{pp} but is tested with V_{out} = 0.63 V_{pp}.
note 2:		Gain flatness test performed from 0.1MHz.

Typical Performance Characteristics (T_A = 25° C, A_V = +2, $\pm V_{CC}$ = ±15V, R_L=100Ω, R_f = 750 Ω)

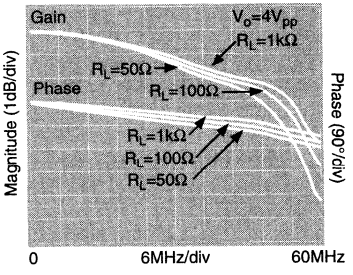
Non-Inverting Frequency Response



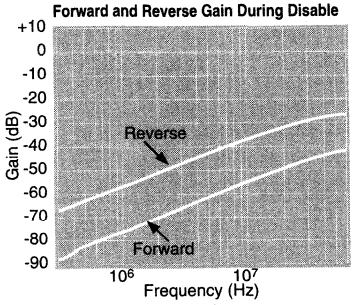
Inverting Frequency Response



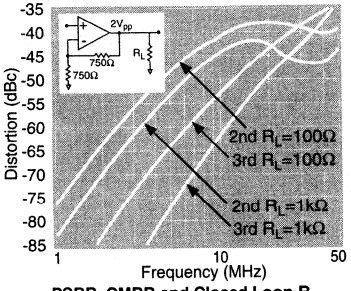
Frequency Response vs.Load



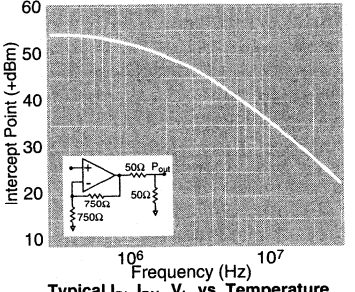
Forward and Reverse Gain During Disable



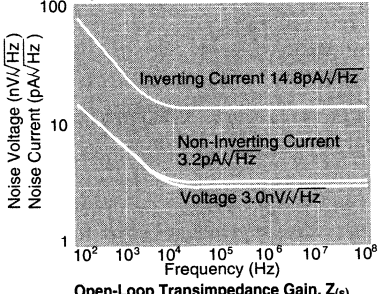
2nd and 3rd Harmonic Distortion



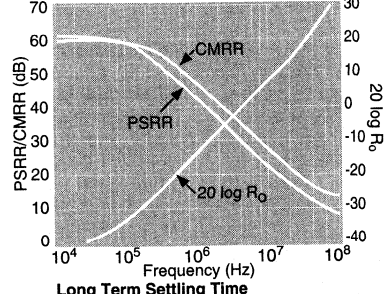
2-Tone, 3rd Order Intermodulation Intercept



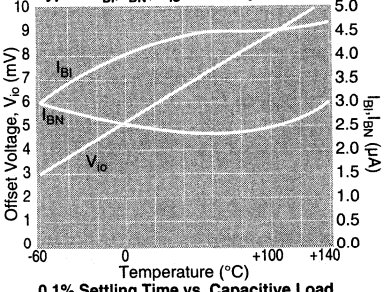
Equivalent Input Noise



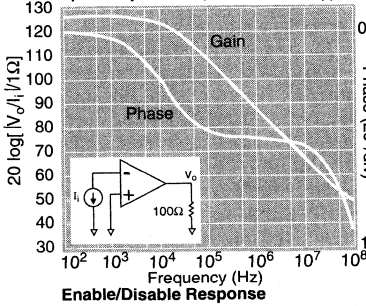
PSRR, CMRR and Closed Loop R_O



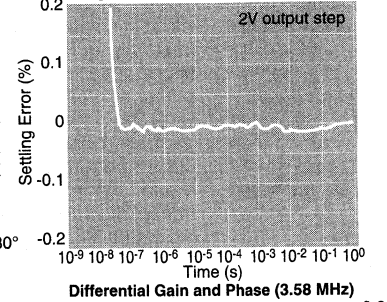
Typical I_{BI}, I_{BN}, V_{io} vs. Temperature



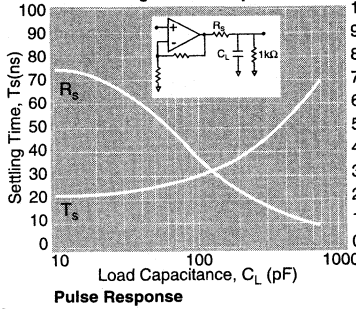
Open-Loop Transimpedance Gain, $Z_{(s)}$



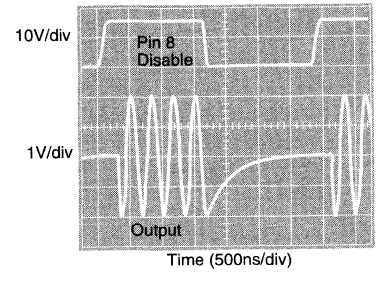
Long Term Settling Time



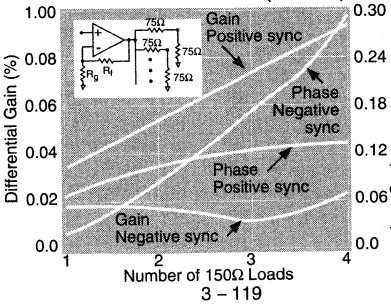
0.1% Settling Time vs. Capacitive Load



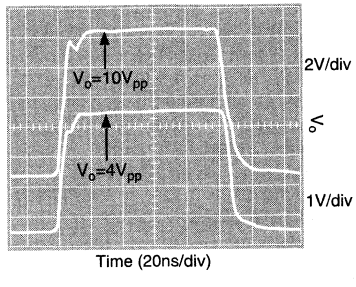
Enable/Disable Response



Differential Gain and Phase (3.58 MHz)



Pulse Response



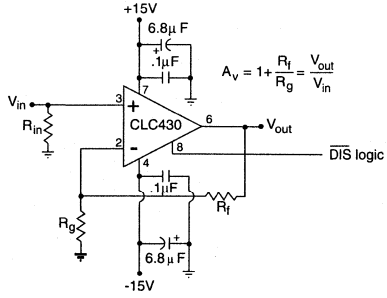


Figure 1: recommended non-inverting gain circuit

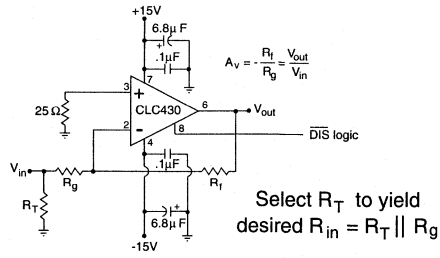


Figure 2: recommended inverting gain circuit

Enable/Disable Operation

The CLC430 has a disable feature which allows several CLC430 outputs to be multiplexed on an analog output bus. When disabled, the CLC430 output and inverting input become a high impedance, and the amplifier quiescent power is reduced. The device is guaranteed to be disabled when the DIS line, pin 8, is grounded. An internal 10kΩ pull-up resistor ensures the amplifier is enabled when pin 8 is left floating or connected to the positive supply. Current, not voltage, determines the enabled state of the CLC430. Logic swings of 0V to + V_{CC} are required by the CLC430 disable pin. Open-collector TTL, or CMOS supplied from the same positive supply will effectively drive the disable feature of the CLC430.

Break-before-make operation is desirable to prevent large transient currents between amplifier outputs connected to the same output bus. The turn-on vs. turn-off time of the CLC430 guarantees two amplifiers will not be enabled simultaneously when driven from the same decoder circuit. Refer to Figure 3A on the CLC410 datasheet for a typical multiplexing circuit.

Feedback Resistor

The loop gain and frequency response for a current feedback amplifier is determined predominantly by the, feedback resistor, R_f. The datasheet electrical characteristics and typical performance plots, unless stated otherwise, specify a 750Ω R_f, a gain of +2, and ±15V supplies. Frequency response at different gains and supply voltages can be optimized by using a different value for R_f. Generally, lowering R_f, will peak the frequency response and extend the bandwith, while increasing its value will roll off the response. For unity-gain voltage follower circuits a non-zero R_f must be used with current feedback amplifiers such as the CLC430.

Application note OA-13 gives a detailed explanation of choosing R_f. The equations in the application note are to be considered as a starting point for the selection of R_f,and do not include the effects of parasitic capacitance at the inverting input, output, nor across the feedback resistor. The value for the inverting input impedance (R_i in OA-13) for the CLC430 is 60Ω when supplied from ±15V, a little higher at lower supply voltages. the following plot entitled "Recommended R_f, vs. Gain" is to be used to choose a value of R_f which will optimize the frequency response of the CLC430 over its entire recommended gain range. For ±5V operation a 675Ω feedback resistor at a gain of ±2 gives best response.

Figure 3

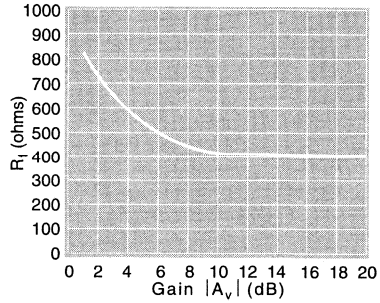


Figure 3: recommend R_f vs. Gain

Differential Gain and Phase

The differential gain and phase of the CLC430 driving one video load (R_L=150Ω) is specified and guaranteed on the Electrical Characteristics table. A Typical Performance plot shows differential gain and phase with the part driving from one to four video loads. The technique used for measuring differential gain and phase is described in detail in application note OA-08.

Printed Circuit Layout

As with any high-speed amplifier, careful attention to circuit board layout is necessary for best performance. Of particular importance is the control of parasitic capacitance at the output and inverting input pins. Protoboards, sockets, and wirewrap construction must not be used due to the excessive parasitic capacitance and inductance resulting from such circuit construction techniques. A good low-impedance ground plane, and high-frequency power supply bypassing immediately adjacent to the device pins are critical to realizing full performance. The key to successful circuit operation is to be aware of frequencies at which the amplifier has power gain, not simply the frequency of the input signal. A discussion circuit design and construction guidelines applicable to the CLC430 can be found in application note OA-1 5.

Evaluation Board

Evaluation boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC430 are available. This board can be used for fast, trouble-free evaluation and characterization of the CLC430, and as a template for engineers designing their own printed circuit boards. Applications schematics for this board can be found in the product accessories section of the Comlinear databook.

Comlinear Corporation

High-Speed Output Clamping Op Amp

CLC501

APPLICATIONS:

- residue amplifier in high-accuracy, subranging A/D systems
- high-speed communications
- output clamping applications
- pulse amplitude modulation systems

FEATURES (typical):

- output clamping (V_{high} and V_{low})
- 1ns recovery from clamping/overdrive
- 0.05% settling in 12ns
- characterized and guaranteed at $A_v = +32$
- low power, 180mW

DESCRIPTION:

The CLC501 is a high-speed current-feedback op amp with the unique feature of output voltage clamping. This feature allows both the maximum positive (V_{high}) and negative (V_{low}) output voltage levels to be established. This is useful in a number of applications in which "downstream" circuitry must be protected from overdriving input signals. Not only can this prevent damage to downstream circuitry, but can also reduce time delays since saturation is avoided. The CLC501's very fast 1ns overload/clamping recovery time is useful in applications in which information-containing signals follow overdriving signals.

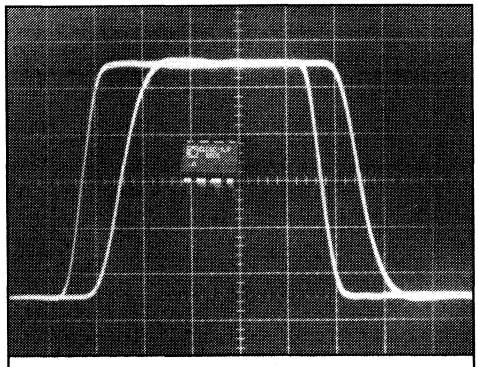
Engineers designing high-resolution, subranging A/D systems have long sought an amplifier capable of meeting the demanding requirements of the residue amplifier function. Amplifiers providing the residue function must not only settle quickly, but recover from overdrive quickly, protect the second stage A/D, and provide high fidelity at relatively high gain settings. The CLC501, which excels in these areas, is the ideal design solution in this onerous application. To further support this application, the CLC501 is both characterized and tested at a gain setting of +32—the most common gain setting for residue amplifier applications.

The CLC501's other features provide a quick, high-performance design solution. Since the CLC501's current feedback design requires no external compensation, designers need not spend their time designing compensation networks. The small 8-pin package and low, 180mW power consumption make the CLC501 ideal in numerous applications having small power and size budgets.

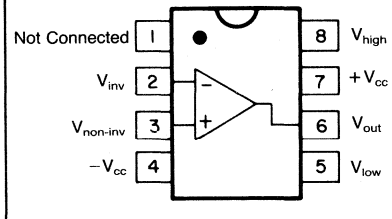
The CLC501 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC501AJP	−40°C to +85°C	8-pin plastic DIP
CLC501AJE	−40°C to +85°C	8-pin plastic SOIC
CLC501AID	−40°C to +85°C	8-pin hermetic sidebrazed ceramic DIP
CLC501A8D	−55°C to +125°C	8-pin hermetic sidebrazed ceramic dip, MIL-STD-883, Level B

Contact factory for other packages. DESC SMD number is 5962-89974.

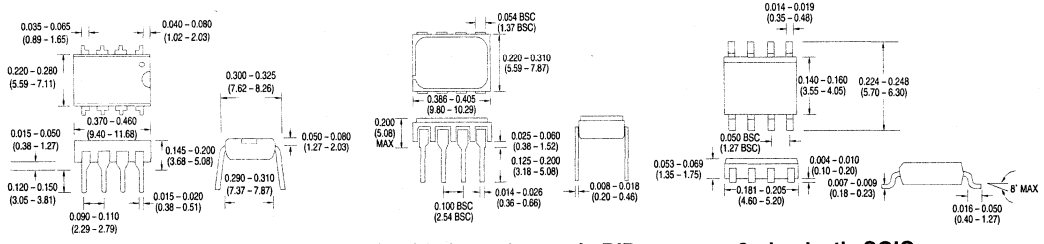


Pinout



DIP and SO-8 Versions

Package Dimensions



8-pin plastic DIP **8-pin side-brazed ceramic DIP** **8-pin plastic SOIC**

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics ($R_L = 100\Omega$, $V_{cc} = \pm 5V$, $A_v = +32$, $R_f = 1.5k\Omega$, $V_H = +3V$, $V_L = -3V$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC501AJ/AI	+25°C	−40°C	+25°C	+85°C		
Ambient Temperature	CLC501A8	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN PERFORMANCE							
†−3dB bandwidth	$V_{out}<5V_{pp}$	75	>60	>60	>45	MHz	SSBW
−3dB bandwidth	$@A_v = +20, V_{out}<2V_{pp}$	110	>85	>85	>55	MHz	SS20
gain flatness	$V_{out}<5V_{pp}$						
† peaking[1]	<15MHz	0	<0.1	<0.1	<0.1	dB	GFPL
† peaking	>15MHz	0	<0.2	<0.2	<0.2	dB	GFPH
† rolloff[1]	<30MHz	0.2	<1.0	<1.0	<1.3	dB	GFR
linear phase deviation	DC to 30MHz	0.2	<1.0	<1.0	<1.0	°	LPD
TIME DOMAIN PERFORMANCE							
rise and fall time	2V step	4.7	<5.8	<5.8	<7.8	ns	TRS
	5V step	5.5	<6.5	<6.5	<8.0	ns	TRL
settling time to ±0.05%	2V step	12	<18	<18	<24	ns	TSP
overshoot	2V step	0	<5	<5	<5	%	OS
slew rate		1200	>800	>800	>700	V/μs	SR
DISTORTION AND NOISE PERFORMANCE							
†2nd harmonic distortion	$2V_{pp}$, 20MHz	−45	<−30	<−33	<−30	dBc	HD2
†3rd harmonic distortion	$2V_{pp}$, 20MHz	−60	<−45	<−50	<−50	dBc	HD3
equivalent input noise[2]							
noise floor	>1MHz	−158	<−156	<−156	<−155	dBm(1Hz)	SNF
integrated noise	1MHz to 100MHz	28	<35	<35	<40	μV	INV
CLAMP PERFORMANCE							
overshoot in clamp	32x overdrive	5	—	<15	—	%	OVC
overload recovery from clamp	32x overdrive	1	<3	<3	<3	ns	TSO
V_{io} drift after recovery		150	<200	<200	<200	μV	CDR
*clamp accuracy	>2x overdrive	0.1	<0.2	<0.2	<0.2	V	VOC
input bias current on V_H, V_L		20	<100	<50	<50	μA	ICL
− 3dB bandwidth	V_L, V_H = 2Vpp	50	—	—	—	MHz	CBW
useful clamping range	V_H or V_L		< ±3.0	< ±3.3	< ±3.3	V	CMC
STATIC, DC PERFORMANCE							
*input offset voltage		1.5	<4.6	<3.0	<5.0	mV	VIO
average temperature coefficient		10	<20	—	<20	μV/°C	DVIO
*input bias current	non-inverting	10	<37	<25	<35	μA	IBN
average temperature coefficient		100	<150	—	<100	nA/°C	DIBN
*input bias current	inverting	10	<46	<30	<40	μA	IBI
average temperature coefficient		100	<200	—	<100	nA/°C	DIBI
†power supply rejection ratio		70	>55	>60	>60	dB	PSRR
♠common mode rejection ratio		70	>55	>60	>60	dB	CMRR
*supply current	no load	18	<25	<24	<24	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	150	>50	>100	>100	kΩ	RIN
	capacitance	4	<7	<7	<7	pF	CIN
output impedance	at DC	0.2	<0.3	<0.3	<0.3	Ω	RO
common mode input range		3.0	>2.0	>2.5	>2.5	V	CMIR
output voltage range	no load	±3.5V	> ±3.0	> ±3.2	> ±3.2	V	VO
output current	−40°C to +85°C	±70	> ±35	> ±50	> ±50	mA	IO
	−55°C to +125°C	±70	> ±30	> ±50	> ±50	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	$\pm V_{cc}$
junction temperature	+ 175°C
operating temperature range	
AI/AJ:	− 40°C to + 85°C
A8:	− 55°C to + 125°C
storage temperature range	− 65°C to + 150°C
lead solder duration (+ 300°C)	10 sec

Miscellaneous Ratings

recommended gain range: + 7 to + 50, − 1 to − 50

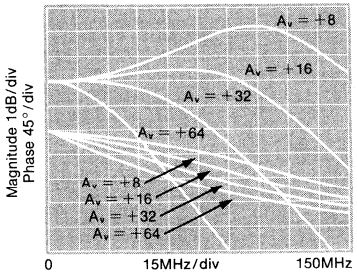
NOTES:

*	AI, AJ	100% tested at + 25°C, sample at + 85°C.
†	AJ	Sample tested at + 25°C.
†	AI	100% tested at + 25°C.
*	A8	100% tested at + 25°C, − 55°C, + 125°C.
†	A8	100% tested at + 25°C, sample − 55°C, + 125°C.
♠	SMD	Sample tested at + 25°C, − 55°C, + 125°C.

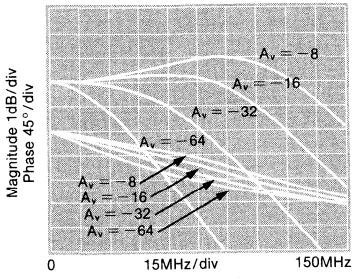
note 1: Gain flatness tests performed from 0.1MHz.

Typical Performance Characteristics ($T_A = 25°C$, $A_v = +32$, $V_{cc} = \pm 5V$, $R_L = 100\Omega$, $R_f = 1.5k\Omega$, $V_H = +3V$, $V_L = -3V$)

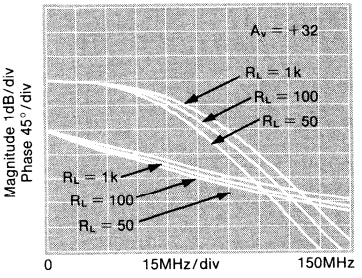
Non-Inverting Frequency Response



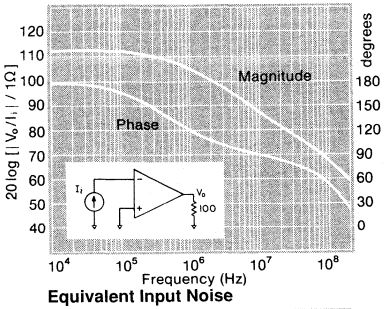
Inverting Frequency Response



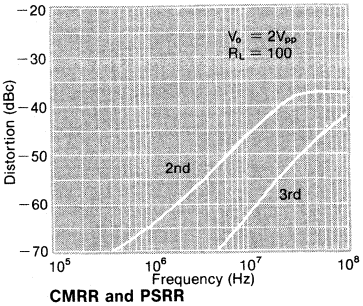
Frequency Response for Various R_Ls



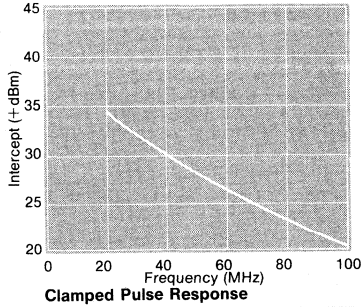
Open-Loop Transimpedance Gain, Z(s)



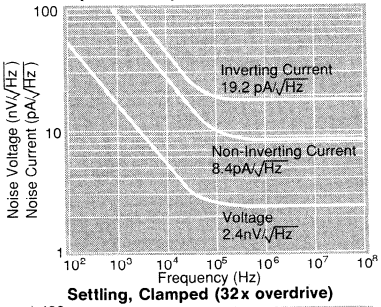
2nd and 3rd Harmonic Distortion



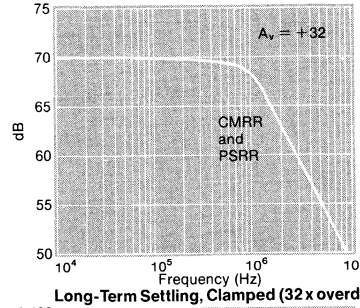
2-Tone, 3rd Order Intermodulation Intercept



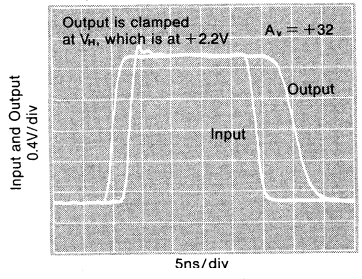
Equivalent Input Noise



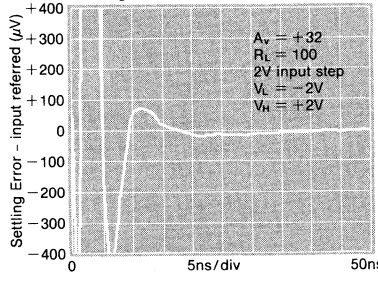
CMRR and PSRR



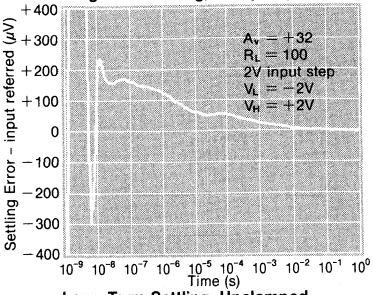
Clamped Pulse Response



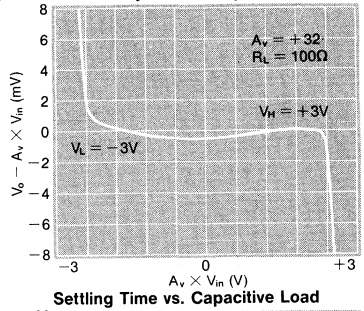
Settling, Clamped (32 x overdrive)



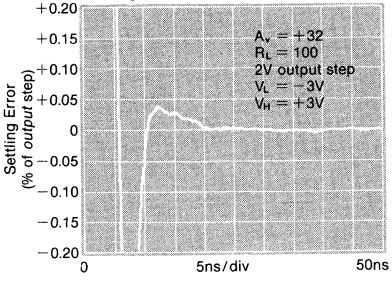
Long-Term Settling, Clamped (32 x overdrive)



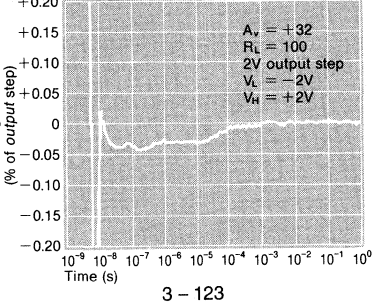
Nonlinearity Near Clamp Voltage



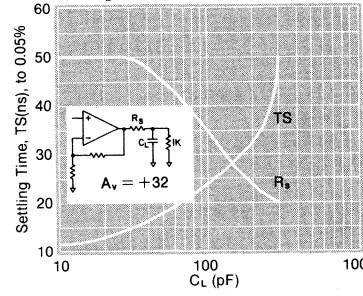
Settling, Unclamped



Long-Term Settling, Unclamped



Settling Time vs. Capacitive Load



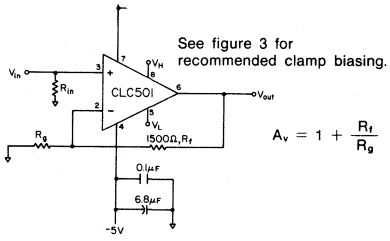


Figure 1:
recommended non-inverting gain circuit

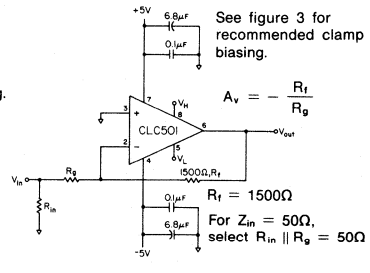


Figure 2:
recommended inverting gain circuit

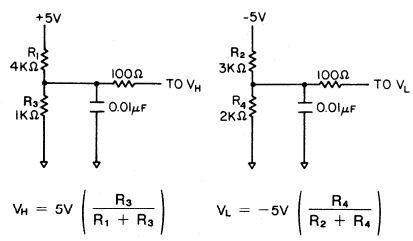


Figure 3: recommended clamp biasing for clamp levels of +1V and −2V

Clamp Operation

The maximum positive or negative excursion of the output voltage is determined by voltages applied to the clamping pins, V_H and V_L. V_H determines the positive clamping level; V_L determines the negative level. For example, if V_H is set at +2V and V_L is set at −0.5V the output voltage is restricted within this −0.5V to +2V range. When the output voltage tries to exceed this level, the amplifier goes into "clamp mode" and the output voltage limits at the clamp voltage.

Clamp Accuracy and Amplifier Linearity

Ideally, the clamped output voltage and the clamp voltage should be identical. In practice, however, there are two sources of clamp inaccuracy: the inherent clamp accuracy (which is shown in the specification page) and resistor divider action of open-loop output resistance of 10Ω and the load resistor. Or, in equation form,

$$V_{out,\ clamp} = (V_{H\ or\ L} \pm 200mV)\ \frac{R_L}{R_L + 10\Omega.}$$

When setting the clamp voltages, the designer should also recognize that within about 200mV of the clamp voltage, amplifier linearity begins to deteriorate. (See plot on previous page.)

Biasing V_H and V_L

Each of the clamping pins is buffered internally so simple resistive voltage divider circuits work well in providing the clamp voltages (see Figure 3). The 100Ω isolating resistor ensures stability when the clamp pin is connected to V_{cc} or when the clamp pin is driven by an external signal source; in other situations, such as the one described in Figure 3, the isolating resistor is not necessary.

V_H should be biased more positively than V_L. V_H may be biased below 0V; however, with this biasing, the output voltage will actually clamp at 0V unless a simple pull down circuit is added to the op amp output. (When clamped against V_H, the output cannot sink current.) An analogous situation and design solution exists for V_L when it is biased above 0V, but in this case, a pull up circuit is used to *source* current when the amplifier is clamped against V_L.

The clamps, which have a bandwidth of about 50MHz, may be driven by a high-frequency signal source. This allows the clamping level to be modulated, which is useful in many applications such as pulse amplitude modulation. The source resistance of the signal source should be less than 500Ω to ensure stability.

Clamp-Mode Dynamics

As can be seen in the clamped pulse response plot on the previous page, clamping is virtually instantaneous. Note, however, that there can be a small amount of overshoot, as indicated on the specification page. The output voltage stays at the clamp voltage level as long as the product of the input voltage and the gain setting exceeds the clamp voltage. When the input voltage decreases, it will eventually reach a point where it is no longer trying to drive the output voltage above the clamp voltage. When this occurs, there is typically a 1ns "overload recovery from clamp," which is the time it takes for the op amp to resume linear operation. The normal op amp parameters, such as the rise time, apply when the op amp is in linear operation.

When the op amp is in clamp mode for more than about 100ns, a small thermal tail can be detected in the settling performance. This tail, which has a maximum value of 200μV referred to the input, is proportional to the amount of time spent in clamp mode. In most applications, this will have only a minor effect. For example, in a system with a 100ns overdrive occurring with a duty cycle of 10%, the input-referred tail is 20μV which is only 0.001% of a 2V signal.

DC Accuracy and Noise

Since the two inputs for the CLC501 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In Equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin resistance.

$$\text{Output Offset } V_o = \pm IBN \times R_s\ (1 + R_f/R_g) \pm VIO\ (1 + R_f/R_g) \pm IBI \times R_f \qquad \text{Eq. (3)}$$

PSRR and CMRR

The PSRR and CMRR performance plots on the previous page show performance for a circuit set at a gain of +32 and a source resistance of 0Ω. In current feedback op amps, common mode and power supply variations manifest themselves in changes in the op amp's bias currents (IBI for the inverting input and IBN for the non-inverting input) and in the offset voltage (VIO). At DC, these values are:

CMRR:	PSRR:
$\frac{\Delta VIO}{\Delta V_{cm}} = 130\mu V/V$	$\frac{\Delta VIO}{\Delta V_{cc}} = 180\mu V/V$
$\frac{\Delta IBN}{\Delta V_{cm}} = 6\mu A/V$	$\frac{\Delta IBN}{\Delta V_{cc}} = 3\mu A/V$
$\frac{\Delta IBI}{\Delta V_{cm}} = 2\mu A/V$	$\frac{\Delta IBI}{\Delta V_{cc}} = 3\mu A/V$

The total effect, as referenced to the input, is given by the following:

$$PSRR: = -20\ \log\left[\frac{\Delta VIO}{\Delta V_{cc}} + \frac{\Delta IBN}{\Delta V_{cc}} R_s + \frac{\Delta IBI}{\Delta V_{cc}} R_{eq}\right]$$

$$CMRR = -20\ \log\left[\frac{\Delta VIO}{\Delta V_{cm}} + \frac{\Delta IBN}{\Delta V_{cm}} R_s + \frac{\Delta IBI}{\Delta V_{cm}} R_{eq}\right]$$

Where R_s is the equivalent resistance seen by the non-inverting input and R_{eq} is the equivalent resistance of R_g in parallel with R_f.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC501 are available.

Comlinear Corporation

Clamping, Low-Gain Op Amp with Fast 14-bit Settling

CLC502

APPLICATIONS:

- output clamping applications
- high-accuracy A/D systems (12-14 bits)
- high-accuracy D/A converters
- pulse amplitude modulation systems

FEATURES:

- output clamping with fast recovery
- 0.0025% settling in 25ns (32ns max.)
- low power, 170mW
- low distortion, −50dBc at 20MHz

DESCRIPTION:

The CLC502 is an operational amplifier designed for low-gain applications requiring output voltage clamping. This feature allows the designer to set maximum positive and negative output voltage levels for the amplifier – thus allowing the CLC502 to protect downstream circuitry, such as delicate converter systems, from destructive transients or signals which would otherwise cause saturation. The overload recovery time of only 8ns permits systems to resume operation quickly after overdrive.

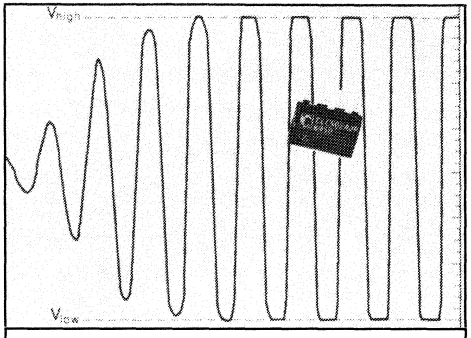
High-accuracy systems will also benefit from the CLC502's fast, accurate settling. Settling to 0.0025% in 25ns (32ns guaranteed over temperature), the CLC502 is ideal as the input amplifier in high-accuracy (12 bits and above) A/D systems. Unlike most other high-speed op amps, the CLC502 is free of settling tails. And, as the settling plots show, settling to 0.01% accuracy is an even faster 18ns typical.

The CLC502 is also useful in other applications which require low-gain amplification (± 1 to ± 8) and the clamping or overload recovery features. For example, even low-resolution imaging circuits, which often have to cope with overloading signal levels, can benefit from clamping and overload recovery.

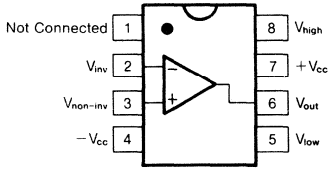
The CLC502 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC502AJP	−40°C to +85°C	8-pin plastic DIP
CLC502AJE	−40°C to +85°C	8-pin plastic SOIC
CLC502AID	−40°C to +85°C	8-pin hermetic side-brazed ceramic DIP
CLC502A8D	−55°C to +125°C	8-pin hermetic side-brazed ceramic DIP, MIL-STD-883, Level B

Contact factory for other packages. DESC SMD number, 5962-91743.

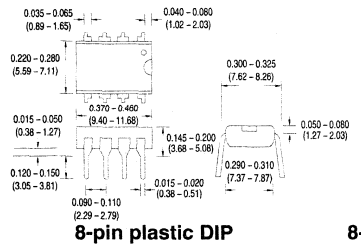


PINOUT

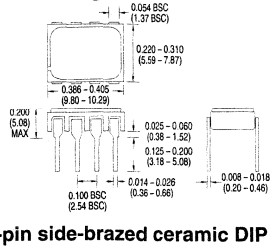


DIP and SO-8 versions

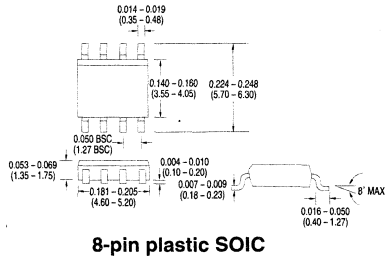
Package Dimensions



8-pin plastic DIP



8-pin side-brazed ceramic DIP



8-pin plastic SOIC

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

DS502.03 January 1993

Electrical Characteristics ($R_L = 100\Omega$, $V_{cc} = \pm 5V$, $A_v = +2$, $R_f = 250\Omega$, $V_h = +3V$, $V_l = -3V$)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC502A8	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC502AJ/AI	+25°C	−40°C	+25°C	+ 85°C		
FREQUENCY DOMAIN PERFORMANCE							
†-3dB bandwidth	V_{out} <0.5V_{pp}	150	>100	>110	>100	MHz	SSBW
	V_{out} <5V_{pp}	65	>40	>40	>40	MHz	LSBW
gain flatness	V_{out} <0.5V_{pp}						
† peaking[2]	DC to 25MHz	0	<0.4	<0.3	<0.4	dB	GFPL
† peaking	>25MHz	0	<0.7	<0.5	<0.7	dB	GFPH
† rolloff[2]	DC to 50MHZ	0.5	<1.0	<1.0	<1.0	dB	GFR
linear phase deviation	DC to 50MHZ	0.4	<1.2	<1.0	<1.2	°	LPD
TIME DOMAIN PERFORMANCE							
rise and fall time	0.5V step	2.7	<3.5	<3.2	<3.5	ns	TRS
	5V step	5.0	<8	<8	<8	ns	TRL
settling time to ±0.0025%	2Vstep	25	<32	<32	<32	ns	TS14
±0.01%	2V step	18	<25	<25	<25	ns	TSP
±0.1%	2V step	10	<15	<15	<15	ns	TSS
overshoot	0.5V step	0	<10	<10	<10	%	OS
slew rate		800	>500	>500	>500	V/μs	SR
DISTORTION AND NOISE PERFORMANCE							
†2nd harmonic distortion	2V_{pp}, 20MHz	−50	<−38	<−43	<−43	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 20MHz	−60	<−53	<−53	<−53	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−157	<−155	<−155	<−155	dBm(1Hz)	SNF
integrated noise	1MHz to 150MHz	40	<49	<49	<49	μV	INV
differential gain[1]		0.01	—	—	—	%	DG
differential phase[1]		0.05	—	—	—	°	DP
CLAMP PERFORMANCE							
overshoot in clamp	2x overdrive	5	—	<10	—	%	OVC
overload recovery from clamp	2x overdrive	8	<15	<15	<15	ns	TSO
*clamp accuracy	2x overdrive	±0.2	<±0.3	<±0.3	<±0.3	V	VOC
input bias current on V_h, V_l		20	<75	<35	<35	μA	ICL
−3dB bandwidth	V_l or V_h = 2V_{pp}	50	—	—	—	MHz	CBW
clamp voltage range	V_h or V_l		<± 3.0	<± 3.3	<± 3.3	V	CMC
STATIC, DC PERFORMANCE							
* input offset voltage		0.5	<2.6	<1.6	<2.8	mV	VIO
average temperature coefficient		3	<12	—	<12	μV/°C	DVIO
* input bias current	noninverting	10	<45	<25	<35	μA	IBN
average temperature coefficient		100	<250	—	<100	nA/°C	DIBN
* input bias current	inverting	10	<50	<30	<40	μA	IBI
average temperature coefficient		100	<250	—	<100	nA/°C	DIBI
†power supply rejection ratio		68	>55	>60	>60	dB	PSRR
♠common mode rejection ratio		65	>55	>60	>60	dB	CMRR
*supply current	no load	17	<23	<23	<23	mA	ICC
MISCELLANEOUS PERFORMANCE							
noninverting input	resistance	150	>50	>85	>85	kΩ	RIN
	capacitance	3.5	<5.5	<5.5	<5.5	pF	CIN
output impedance	at DC	0.1	<0.2	<0.2	<0.2	Ω	RO
common mode input range		3.0	>2.0	>2.5	>2.5	V	CMIR
output voltage range	no load	±3.5V	>±3.0	>±3.2	>±3.2	V	VO
output current		±55	>±25	>±45	>±45	mA	IO

Absolute Maximum Ratings

V_{cc}	± 7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	± V_{cc}
junction temperature	+ 175°C
operating temperature range	
AI/AJ:	− 40°C to + 85°C
A8:	− 55°C to + 125°C
storage temperature range	− 65°C to + 150°C
lead solder duration (+ 300°C)	10 sec

Miscellaneous Ratings

recommended gain range: ± 1 to ± 8

NOTES:

*	AI, AJ	100% tested at + 25°C, sample at +85°C.
†	AJ	Sample tested at + 25°C.
†	AI	100% tested at + 25°C.
*	A8	100% tested at + 25°C, − 55°C, + 125°C.
†	A8	100% tested at + 25°C, sample − 55°C, + 125°C.
♠	SMD	Sample tested at + 25°C, − 55°C, +125°C.

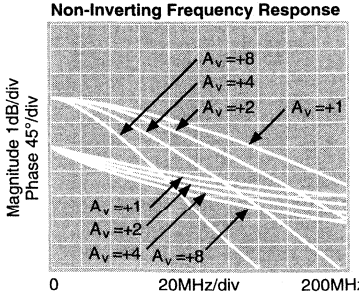
note 1: Differential gain and phase measured at A_v = +2V, R = 250Ω.

note 2: Gain flatness tests begin at 0.1MHz.

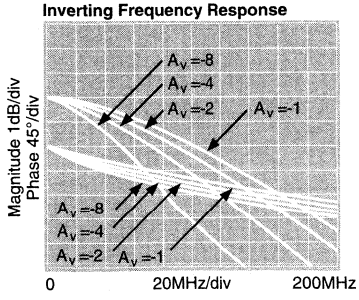
R_L = 150Ω, 1V_{pp} equivalent video signal, 0-100 IRE, 40 IRE$_{pp}$, 0 IRE = 0 volts, at 75Ω load and 3.58 MHz.

Typical Performance Characteristics (T_A =+25°C, A_V =+2, V_{CC} =±5V, R_L =100Ω, R_f =250Ω, V_H =+3V, V_L =-3V)

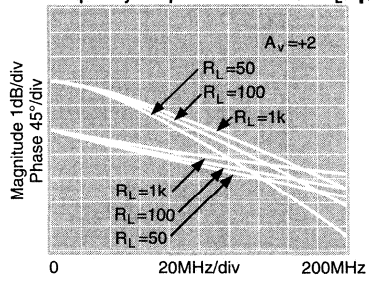
Non-Inverting Frequency Response



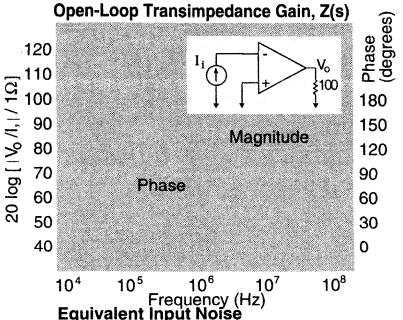
Inverting Frequency Response



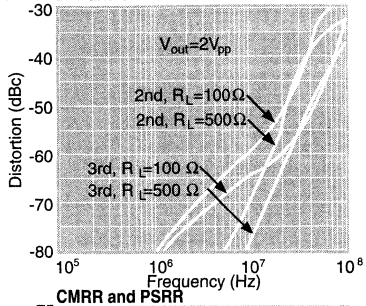
Frequency Response for Various R_Ls



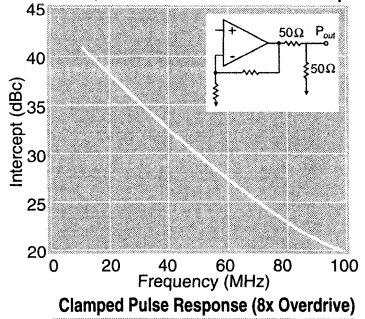
Open-Loop Transimpedance Gain, Z(s)



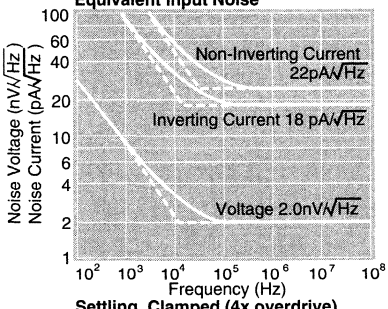
2nd and 3rd Harmonic Distortion



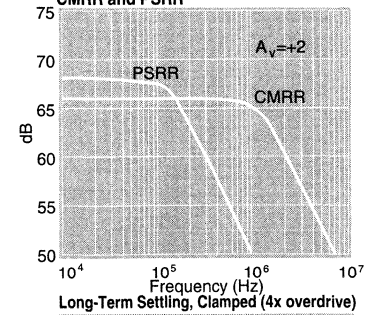
2-Tone, 3rd Order Intermodulation Intercept



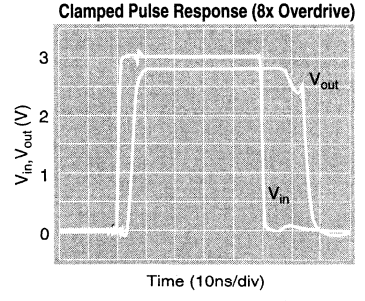
Equivalent Input Noise



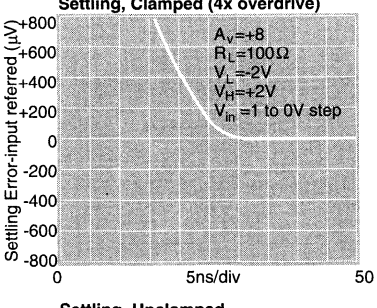
CMRR and PSRR



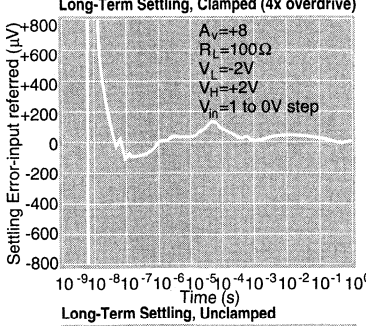
Clamped Pulse Response (8x Overdrive)



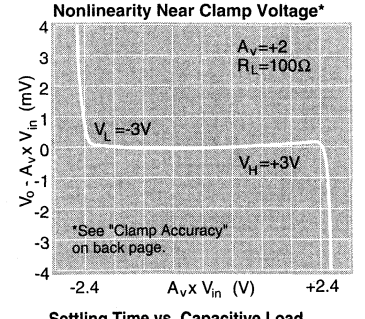
Settling, Clamped (4x overdrive)



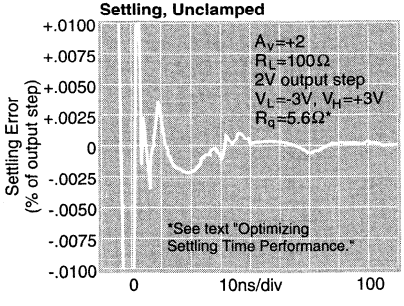
Long-Term Settling, Clamped (4x overdrive)



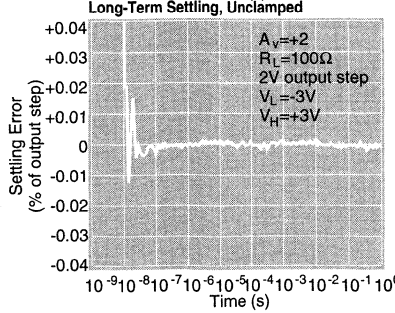
Nonlinearity Near Clamp Voltage*



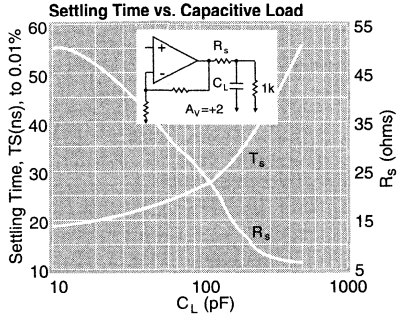
Settling, Unclamped



Long-Term Settling, Unclamped



Settling Time vs. Capacitive Load



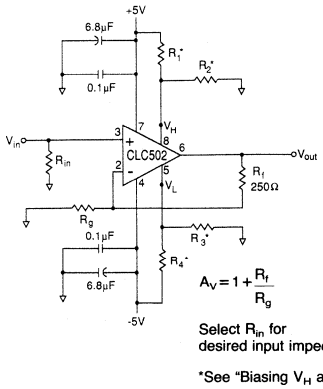


Figure 1:
recommended non-inverting gain circuit

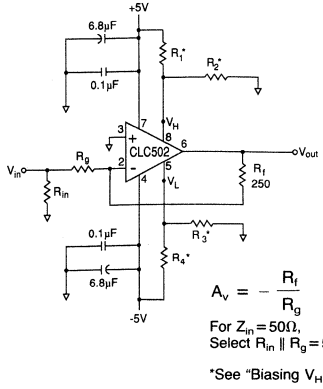


Figure 2:
recommended inverting gain circuit

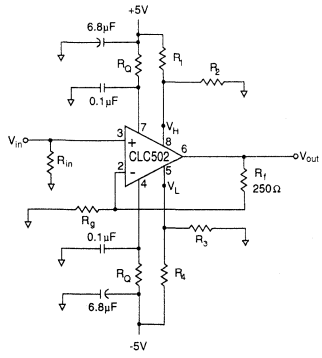


Figure 3:
location of damping resistors (R_Q)

Clamp Operation

The maximum positive or negative excursion of the output voltage is determined by voltages applied to the clamping pins, V_H and V_L. V_H determines the positive clamping level; V_L determines the negative level. For example, if V_H is set at +2V and V_L is set at −0.5V the output voltage is restricted within this −0.5V to +2V range. When the output voltage tries to exceed this level, the amplifier goes into "clamp mode" and the output voltage limits at the clamp voltage.

Clamp Accuracy and Amplifier Linearity

Ideally, the clamped output voltage and the clamp voltage should be identical. In practice, however, there are two sources of clamp inaccuracy: the inherent clamp accuracy (which is shown in the specification page) and resistor divider action of open-loop output resistance of 10Ω and the load resistor. Or, in equation form,

$$V_{out,\ clamp} = (V_{H\ or\ L} \pm 300mV)\frac{R_L}{R_L + 10\Omega.}$$

When setting the clamp voltages, the designer should also recognize that within about 200mV of the clamp voltage, amplifier linearity begins to deteriorate. (See plot on previous page.)

Biasing V_H and V_L

Each of the clamping pins is buffered internally so simple resistive voltage divider circuits work well in providing the clamp voltages. V_L and V_H can be set by choosing the divider resistors using:

$$V_H = (5V)\left(\frac{R_2}{R_1 + R_2}\right) \qquad V_L = (-5V)\left(\frac{R_3}{R_3 + R_4}\right)$$

As a general guideline, let $R_1 + R_2 \cong R_3 + R_4 \cong 5k\Omega$.

V_H should be biased more positively than V_L. V_H may be biased below 0V; however, with this biasing, the output voltage will actually clamp at 0V unless a simple pull down circuit is added to the op amp output (when clamped against V_H, the output cannot sink current). An analogous situation and design solution exists for V_L when it is biased above 0V, but in this case, a pull up circuit is used to *source* current when the amplifier is clamped against V_L.

The clamp voltage range rating is that for normal operation. Problems in overdriven linearity may occur if the clamps are set outside this range so this is not suggested under any conditions. If the clamping capability is not required, the CLC402 (low-gain op amp with fast 14-bit settling) may be the more appropriate part.

The clamps, which have a bandwidth of about 50MHz, may be driven by a high-frequency signal source. This allows the clamping level to be modulated, which is useful in many applications such as pulse amplitude modulation. The source resistance of the signal source should be less than 500Ω to ensure stability.

Clamp-Mode Dynamics

As can be seen in the clamped pulse response plot on the previous page, clamping is virtually instantaneous. Note, however, that there can be a small amount of overshoot, as indicated on the specification page. The output voltage stays at the clamp voltage level as long as the product of the input voltage and the gain setting exceeds the clamp voltage. When the input voltage decreases, it will eventually reach a point where it is no longer trying to drive the output voltage above the clamp voltage. When this occurs, there is typically a 5-10ns "overload recovery from clamp," which is the time it takes for the op amp to resume linear operation. The normal op amp parameters, such as the rise time, apply when the op amp is in linear operation.

Optimizing Settling Time Performance

To obtain the best possible settling time performance for the CLC502, some additional design criteria must be considered, particularly when driving loads of less than 500Ω. When driving a 100Ω load, a step of a few volts on the output will create a large step of current in the power supplies. In some cases, this step will cause a small ringing on the power supply due to the bypass capacitor (.1μF) oscillating with the inductance in the power supply trace. The critical trace is the power supply trace between the two capacitors (a trace inductance of 20nH will be enough to degrade settling time performance). The frequency of the ring can be determined by

$$f = \frac{1}{2\pi\sqrt{C \cdot L_{Trace}}}$$

and any reduction in this frequency will improve performance due to better power supply rejection at lower frequencies. To obtain the best performance, a small resistor, R_Q, may be added in the trace to dampen the circuit (See Figure 3). An R_Q of 5-10Ω will result in excellent settling performance and will have only minor impact on other performance characteristics. No provision for R_Q has been made on the evaluation board available from Comlinear as part #730013. It can, however, be easily added by cutting a trace and adding a 5-10Ω resistor, as shown in Figure 3, for both supplies.

DC Accuracy and Noise

Since the two inputs for the CLC502 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. The two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting source resistance ineffective.

In Equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin source resistance.

$$\text{Output Offset } V_O = \pm IBN \times R_S(1 + R_f/R_g) \pm VIO\ (1 + R_f/R_g) \pm IBI \times R_f \qquad \text{Eq. (3)}$$

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

The device is also very sensitive to parasitic capacitance on the output pin. The plots include a suggested series R_s to de-couple this effect. Evaluation boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC502 are available.

Comlinear Corporation

High-Speed, Programmable-Supply Current, Monolithic Op Amp

CLC505

APPLICATIONS:

- low-power/battery applications
- remote site instrumentation
- mobile communications gear
- video switching matrix
- phased-array radar

DESCRIPTION:

The CLC505 is a monolithic, high-speed op amp with a unique combination of high performance, low power consumption, and flexibility of operation. With a 10 to 1 range of supply current programmability (not preset currents, but rather a continuous range "programmed" with a single external resistor, R_p), this amplifier can be used in a wide variety of high-performance applications. Performance (typical) at any supply current is exceptional:

parameter	Supply Current (I_{cc}) 1mA	3.4mA	9mA	Units
-3dB bandwidth	50	100	150	MHz
settling time	35	14	12	nsec
slew rate	800	1200	1700	V/μsec
output current	7	25	45	mA

Even at 10mW power consumption, the CLC505 provides performance far beyond other monolithic op amps, many of which consume nearly 100 times as much power.

The CLC505's combination of high performance, low power consumption, and large signal performance makes the CLC505 ideal for many demanding applications in which power consumption must be minimized. Examples include a variety of remote site equipment such as battery-powered test instrumentation and communications gear. Power is also critical in applications requiring many channels, such as video switching matrices, ATE, and phased-array radar systems.

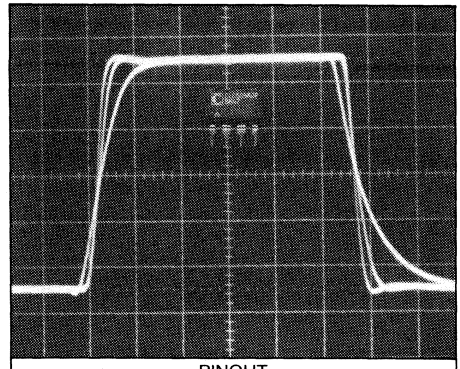
The CLC505 has been designed for ease of use and has been specified for design confidence and predictability. **The following pages include three complete data sheets, one for operation at 1mA supply current, one at 3.4mA, and one at 9mA. Specifications are guaranteed and tested at all three supply currents.** The CLC505 is also available in several versions specified by the three-letter suffix:

CLC 505AJP	-40°C to +85°C	8-pin plastic DIP
CLC505AJE	-40°C to +85°C	8-pin plastic SOIC
CLC505AID	-40°C to +85°C	8-pin side-brazed ceramic DIP
CLC505A8D	-55°C to +125°C	8-pin hermetic side-brazed ceramic DIP, MIL-STD-883, Level B
CLC505ALC	-55°C to +125°C	dice
CLC505AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD 883, Level B

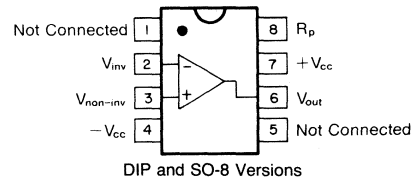
Contact factory for other packages. DESC SMD number, 5962-90993.

FEATURES (typical):

- 10mW power consumption with 50MHz BW
- single-resistor programming of supply current
- 3.4mA I_{cc} provides 100MHz bandwidth and 14ns settling (0.05%)
- fast disable capability
- 0.04% differential gain at I_{cc} = 3.4mA
- 0.06° differential phase at I_{cc} = 3.4mA

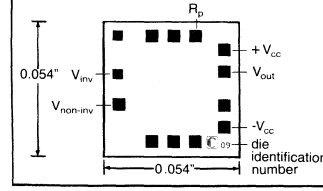


PINOUT



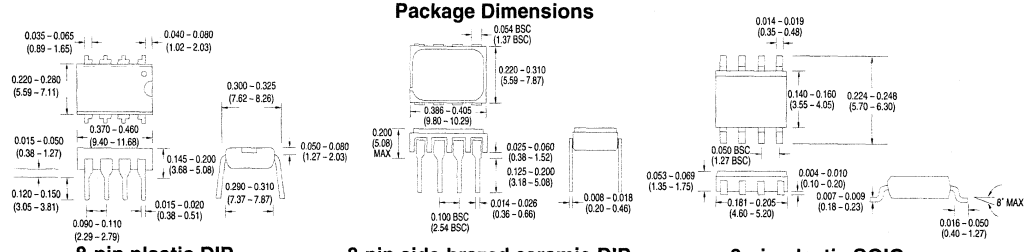
DIP and SO-8 Versions

Chip Topography



Height is 0.014 inches.
NOTE: Backside connected to $-V_{cc}$. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



8-pin plastic DIP **8-pin side-brazed ceramic DIP** **8-pin plastic SOIC**

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics (A_V = +6, V_{CC} = ±5.0V, R_f = 1000Ω, C_p = 100pF)

		SUPPLY CURRENT I_{CC} (TYP) = 9mA R_P = 33kΩ, R_L = 250Ω					
PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC505A8/AL/AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC505AJ/AI	+25°C	−40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
†-3dB bandwidth	Vout<$2V_{pp}$	150	>115	>115	>100	MHz	SSBW
-3dB large signal	Vout<$5V_{pp}$	135	>95	>95	>80	MHz	LSBW
gain flatness	Vout<$2V_{pp}$						
† peaking[4]	<25/20/10MHz**	0	<0.4	<0.3	<0.4	dB	GFPL
† peaking	>25/20/10MHz**	0	<0.6	<0.5	<0.6	dB	GFPH
† rolloff[4]	<50/40/20MHz**	0.2	<1.0	<1.0	<1.3	dB	GFR
linear phase deviation	DC to 50/40/20MHz**	0.6	<1.0	<1.0	<1.2	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.3	<3.0	<3.0	<3.5	ns	TRS
	5V step	2.6	<3.7	<3.7	<4.4	ns	TRL
settling time to 0.1/0.05/0.05%**	2V step	12	<16	<16	<16	ns	TSP
overshoot	2V step	5	<15	<12	<15	%	OS
slew rate (for A_V +2)[2]		1700	>1000	>1200	>1200	V/μs	SR
DISTORTION AND NOISE RESPONSE							
† 2nd harmonic distortion	$2V_{pp}$, 20/10/5MHz**	−50	<−40	<−45	<−45	dBc	HD2
† 3rd harmonic distortion	$2V_{pp}$, 20/10/5MHz**	−65	<−55	<−55	<−55	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−156	<−154	<−154	<−153	dBm(1Hz)	SNF
integrated noise	1MHz to 200/200/100MHz**	50	<65	<65	<70	μV	INV
differential gain[3]		0.04	—	—	—	%	DG
differential phase[3]		0.06	—	—	—	°	DP
STATIC, DC PERFORMANCE							
§* input offset voltage		2	<±12.8	<±8.0	<±14	mV	VIO
average temperature coefficient		30	<±50	—	<±50	μV/°C	DVIO
§* input bias current	non-inverting	8	<±36	<±18	<±18	μA	IBN
average temperature coefficient		80	<±225	—	<±100	nA/°C	DIBN
§* input bias current	inverting	10	<±60	<±38	<±40	μA	IBI
average temperature coefficient		80	<±275	—	<±125	nA/°C	DIBI
† power supply rejection ratio		50	>45	>48	>45	dB	PSRR
♠ common mode rejection ratio		50	>45	>48	>45	dB	CMRR
§* supply current	**no load, quiescent**	**9**	**<11**	**<11**	**<12**	**mA**	**ICC**
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	1200	>400	>800	>1600	kohm	RIN
	capacitance	1	<2	<2	<2	pF	CIN
output impedance	at DC	0.2	<1.2	<0.3	<0.2	ohm	RO
output voltage range	no load	±3.3	>±2.8	>±3.0	>±3.0	V	VO
common mode input range	for rated performance	±2.2	>±1.5	>±1.8	>±2.0	V	CMIR
output current	−40°C to +85°C	±45	>±20	>±36	>±36	mA	IO
	−55°C to +125°C	±45	>±18	>±36	>±36	mA	IO

Absolute Maximum Ratings

V_{CC}	±7V
I_{out} is short circuit protected to ground, maximum reliability maintained if I_{out} does not exceed (except A8 should not exceed 35mA over military temperature range.)	70mA
common mode input voltage	$\pm V_{CC}$
differential input voltage	10V
junction temperature range	+175°C
operating temperature range	
AI/AJ:	−40°C to + 85°C
A8/AM/AL:	−55°C to + 125°C
storage temperature range	−65°C to + 150°C
lead solder duration (+300°C)	10 sec

Miscellaneous Ratings

Recommended gain range: +2 to +21, -1 to -20

NOTES:

*	AI,AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested at +25°C, −55°C, +125°C.
†	A8	100% tested at +25°C, sample −55°C, +125°C.
*	AL, AM	100% wafer probe tested at +25°C to +25°C. min/max specifications.
♠	SMD	Sample tested at +25°C, -55°C, +125°C.

note 1: Not applicable due to output current limitations.
note 2: See text on the back page of the data sheet
note 3: Differential gain and phase is characterized with a $1V_{pp}$ equivalent video signal, 0-100 IRE, 40 IRE_{pp}, and 0IRE = 0V at the load resistor and 3.58 MHz.
note 4: Gain flatness tests performed from 0.1 MHz.

Electrical Characteristics (A_V = +6, $\pm V_{CC}$ = ±5.0V, R_L = 1000Ω, C_p = 100pF)

SUPPLY CURRENT I_{CC} (TYP) = 3.4mA R_p = 100kΩ, R_L = 500Ω				SUPPLY CURRENT I_{CC} (TYP) = 1mA R_p = 300kΩ, R_L = 1000Ω					
TYP	MAX & MIN RATINGS			TYP	MAX & MIN RATINGS			UNITS	SYMBOL
+25°C	−55°C	+25°C	+125°C	+25°C	−55°C	+25°C	+125°C		
+25°C	−40°C	+25°C	+85°C	+25°C	−40°C	+25°C	+85°C		
100	>80	>80	>65	50	>30	>35	>30	MHz	SSBW
80	>50	>50	>40	33	—[1]	>20	>18	MHz	LSBW
0	<0.3	<0.2	<0.3	0	<0.2	<0.1	<0.2	dB	GFPL
0	<0.5	<0.4	<0.5	0	<0.3	<0.2	<0.3	dB	GFPH
0.2	<1.0	<1.0	<1.3	0.5	<1.0	<1.0	<1.3	dB	GFR
0.5	<1.0	<1.0	<1.2	0.3	<0.8	<0.8	<1.0	°	LPD
3.5	<4.4	<4.4	<5.4	7	<12	<10	<12	ns	TRS
4.4	<7.0	<7.0	<8.8	9	—[1]	<18	<20	ns	TRL
14	<22	<22	<22	35	<70	<60	<60	ns	TSP
2	<12	<10	<12	0	<8	<5	<8	%	OS
1200	>700	>800	>800	800	>500	>600	>600	V/μs	SR
−55	<−40	<−45	<−45	−55	<−40	<−45	<−45	dBc	HD2
−65	<−55	<−55	<−55	−65	<−55	<−55	<−55	dBc	HD3
−155	<−153	<−153	<−152	−152	<−150	<−150	<−149	dBm(1Hz)	SNF
56	<70	<70	<80	55	<70	<70	<80	μV	INV
0.04	—	—	—	0.1	—	—	—	%	DG
0.06	—	—	—	0.1	—	—	—	°	DP
3	<±11.8	<±7.0	<±13	3	<±13.0	<±7.0	<±14.5	mV	VIO
40	<±60	—	<±60	50	<±75	—	<±75	μV/°C	DVIO
2	<±12	<±6	<±6	1	<±5.0	<±2.5	<±2.5	μA	IBN
30	<±75	—	<±50	10	<±32	—	<±30	nA/°C	DIBN
4	<±22	<±14	<±15	2	<±7.0	<±4.0	<±5.0	μA	IBI
40	<±100	—	<±60	20	<±38	—	<±35	nA/°C	DIBI
50	>45	>48	>45	50	>45	>48	>45	dB	PSRR
50	>45	>48	>45	50	>45	>48	>45	dB	CMRR
3.4	**<3.8**	**<3.8**	**<4.2**	**1.0**	**<1.4**	**<1.3**	**<1.4**	**mA**	**ICC**
3000	>1000	>2000	>4000	7500	>2500	>5000	>10000	kohm	RIN
1	<2	<2	<2	1	<2	<2	<2	pF	CIN
0.2	<1.6	<0.5	<0.2	0.5	<3.0	<1.0	<0.5	ohm	RO
±3.3	>±2.8	>±3.0	>±3.0	±3.3	>±2.5	>±3.0	>±3.0	V	VO
±2.2	>±1.5	>±1.8	>±2.0	±2.2	>±1.5	>±1.8	>±2.0	V	CMIR
±25	>±10	>±18	>±18	±7	>±3.0	>±5	>±5	mA	IO
±25	>±9	>±18	>±18	±7	>±2.5	>±5	>±5	mA	IO

Notes

§ ALL versions: **Parameter is 100% tested at +25°C in die form at I_{cc} = 1mA, 3.4mA, and 9mA.**

*AJ version: With I_{CC} (TYP) =3.4mA, parameter is 100% tested at +25°C and sample tested at -40°C and +85°C.

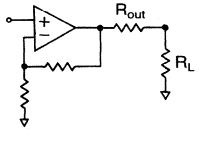
†AJ version: With I_{CC} (TYP) = 3.4 mA, parameter is sample tested at +25°C.

†AI version: With I_{CC} (TYP) = 3.4 mA, parameter is 100% tested at +25°C and sample tested at -40°C and +85°C.

*,†A8 version: With I_{CC} (TYP) = 3.4 mA, parameter is 100% tested at +25°C, -55°C, and +125°C.

Conditions are different for the three supply currents:

I_{cc}	R_L	R_{OUT}	A_V
9mA	75Ω	75Ω	+2
3.4mA	500Ω	0Ω	+6
1mA	1000Ω	0Ω	+6

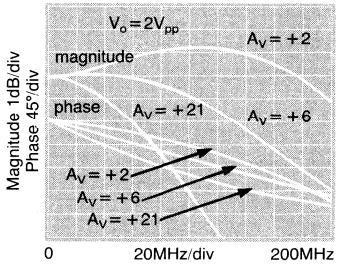


**** xx/yy/zz MHz indicates that the CLC505 is specified at xxMHz for I_{cc} = 9mA, yyMHz for I_{cc}=3.4mA, and zzMHz for I_{cc}=1mA.**

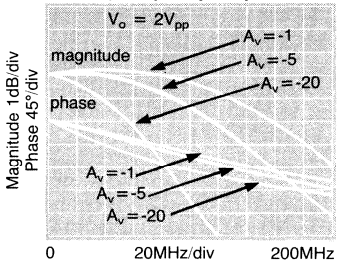
Typical Performance Characteristics (T_A = +25°C, A_V = +6, R_f = 1000Ω, C_p = 100pF)

I_{cc} = 9mA, R_L = 250Ω

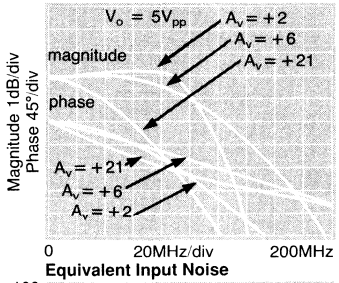
Non-Inverting Frequency Response



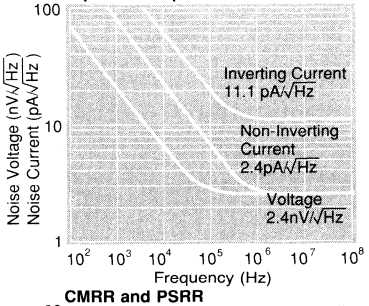
Inverting Frequency Response



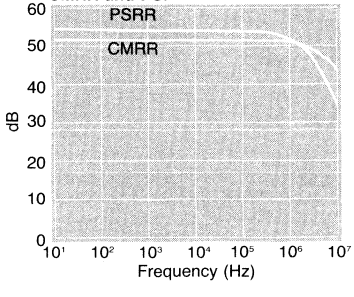
Large Signal Frequency Response



Equivalent Input Noise

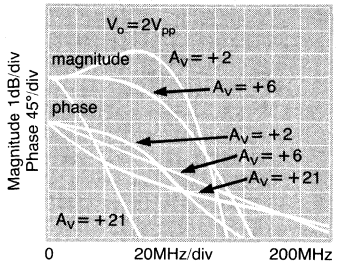


CMRR and PSRR

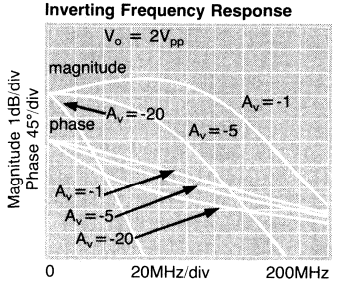


I_{cc} = 3.4mA, R_L = 500Ω

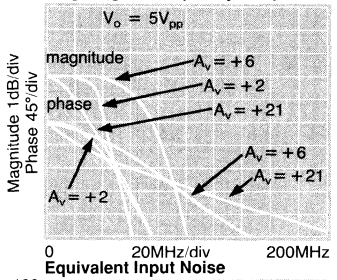
Non-Inverting Frequency Response



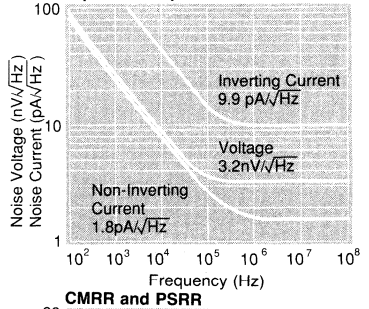
Inverting Frequency Response



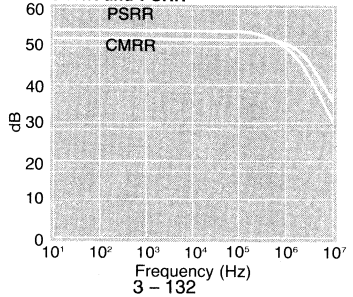
Large Signal Frequency Response



Equivalent Input Noise

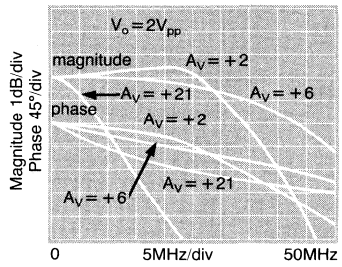


CMRR and PSRR

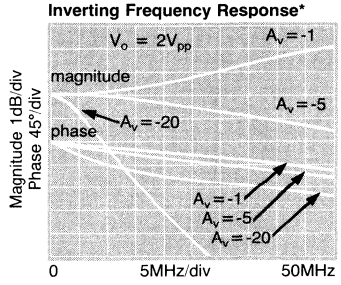


I_{cc} = 1mA, R_L = 1000Ω

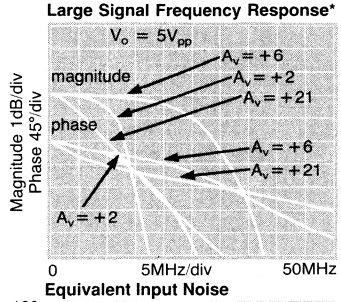
Non-Inverting Frequency Response*



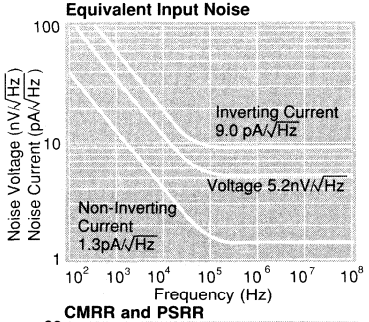
Inverting Frequency Response*



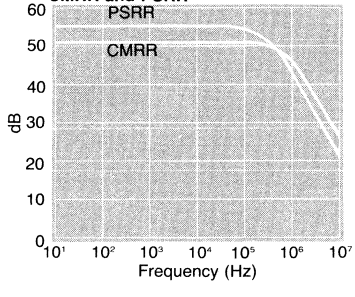
Large Signal Frequency Response*



Equivalent Input Noise

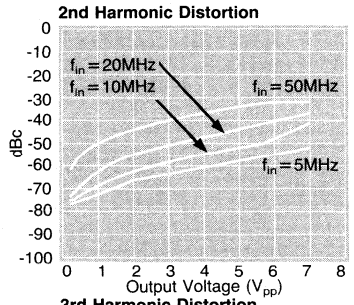


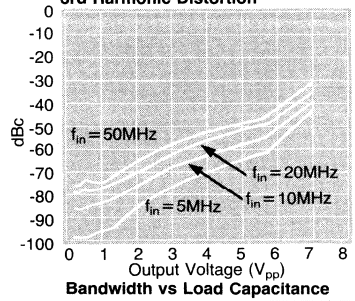
CMRR and PSRR

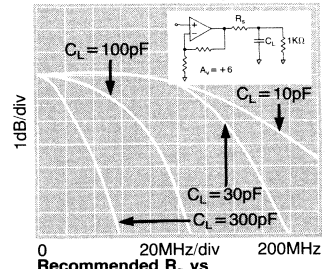


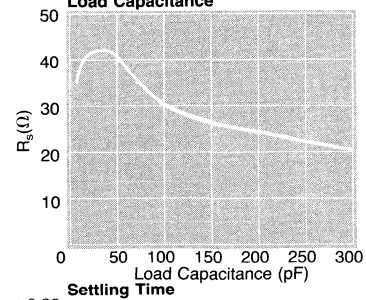
Typical Performance Characteristics (T_A = +25°C, A_V = +6, R_L = 100Ω, C_L = 100pF)

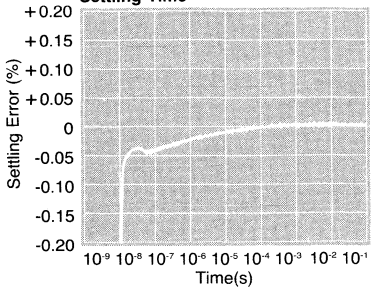
I_{cc} = 9mA, R_L = 250Ω



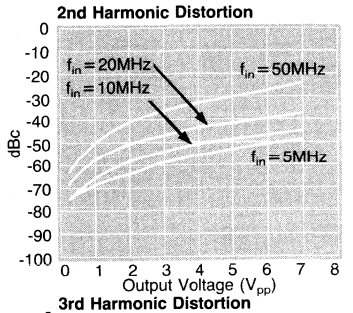


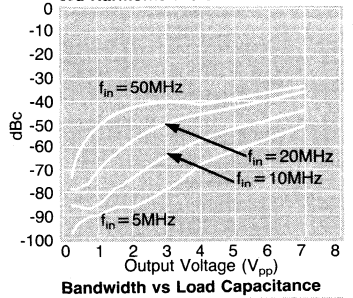


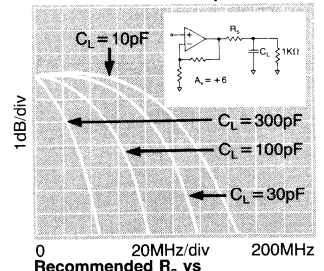


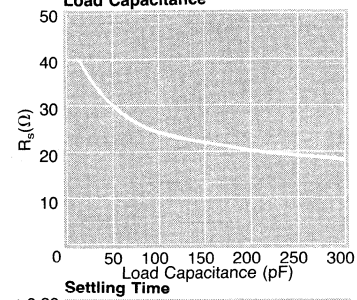


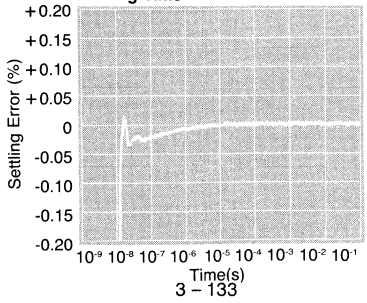
I_{cc} = 3.4mA, R_L = 500Ω



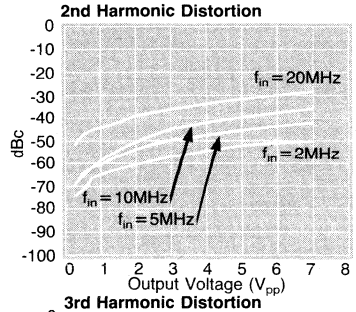


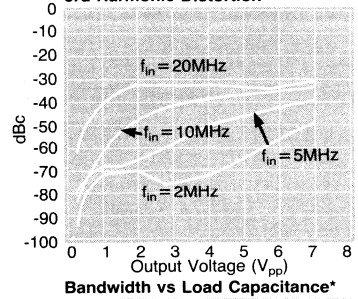


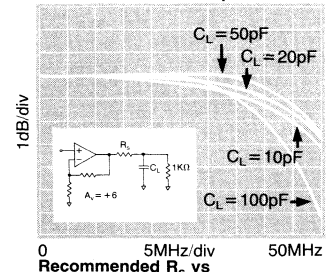


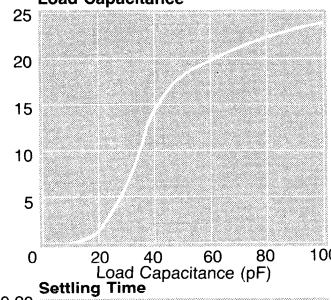


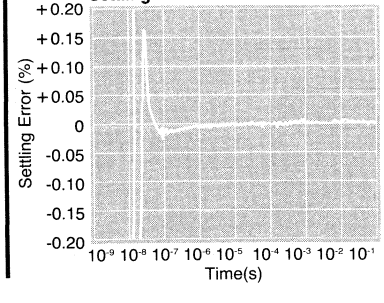
I_{cc} = 1mA, R_L = 1000Ω







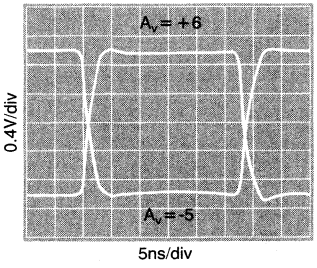




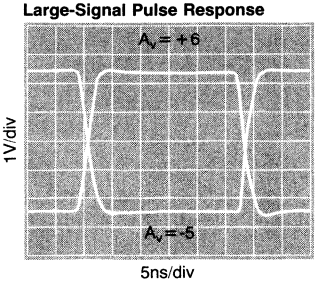
Typical Performance Characteristics (T_A = +25°C, A_V = +6, R_f = 1000Ω, C_p = 100pF)

I_{cc} = 9mA, R_L = 250Ω

Small-Signal Pulse Response

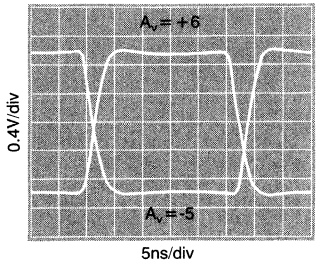


Large-Signal Pulse Response

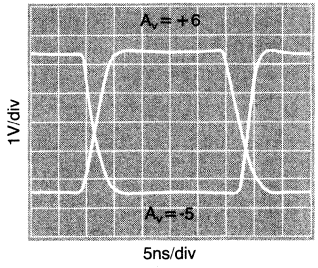


I_{cc} = 3.4mA, R_L = 500Ω

Small-Signal Pulse Response

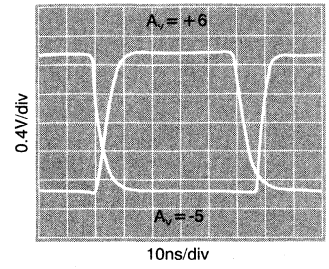


Large-Signal Pulse Response

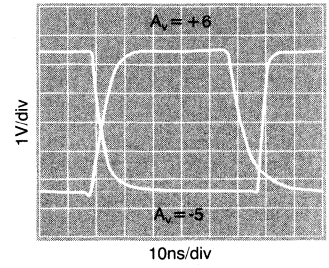


I_{cc} = 1mA, R_L = 1000Ω

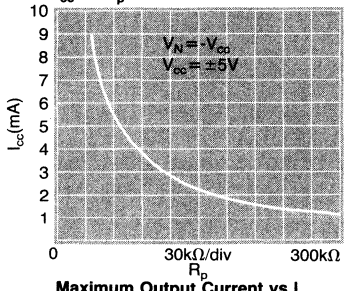
Small-Signal Pulse Response*



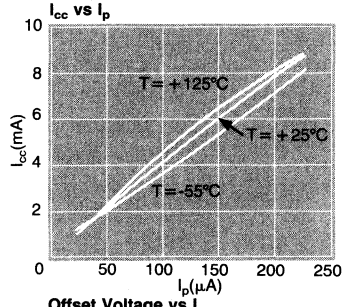
Large-Signal Pulse Response*



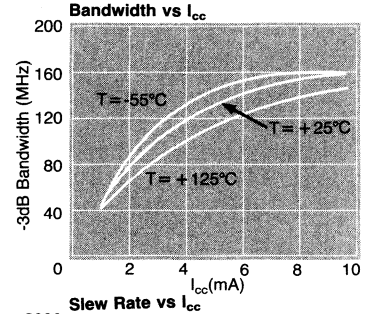
I_{cc} vs R_p



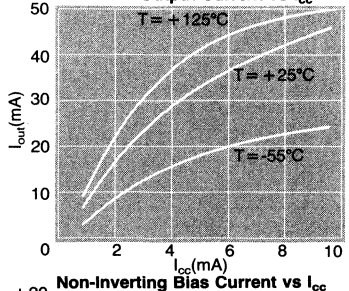
I_{cc} vs I_p



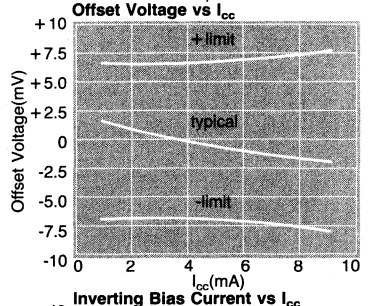
Bandwidth vs I_{cc}



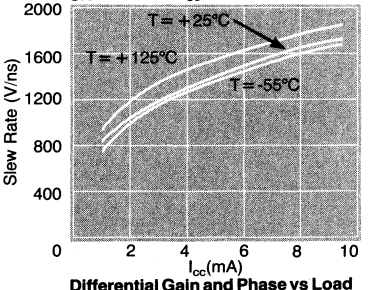
Maximum Output Current vs I_{cc}



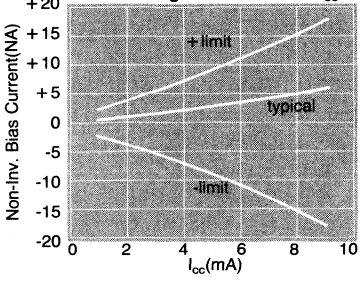
Offset Voltage vs I_{cc}



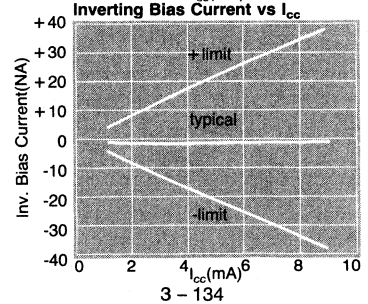
Slew Rate vs I_{cc}



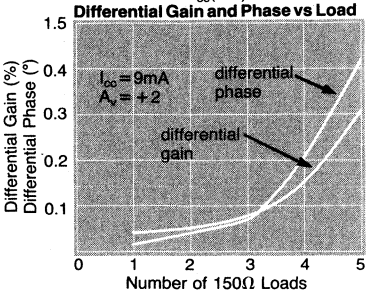
Non-Inverting Bias Current vs I_{cc}

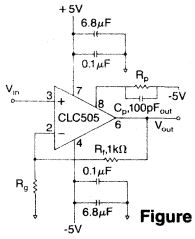


Inverting Bias Current vs I_{cc}



Differential Gain and Phase vs Load

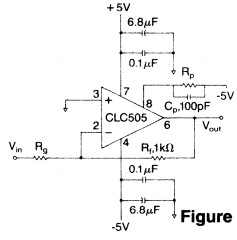




$$A_V = 1 + \frac{R_f}{R_g}$$

note: C_p may also be connected from pin 8 to ground

Figure 1: recommended non-inverting gain circuit



$$A_V = \frac{-R_f}{R_g}$$

note: C_p may also be connected from pin 8 to ground

Figure 2: recommended inverting gain circuit

Description

The CLC505 is a progammable-supply current, current-feedback operational amplifier. Supply current and consequently dynamic performance can be easily adjusted by selecting the value of a single external resistor (R_p). This capability is reflected in the datasheet by three complete sets of specifications, each at a different value of supply current.

Selecting an Operating Point

The operating point is determined by the supply current, which in turn is determined by current (I_p) flowing out of pin 8. As the supply current is reduced the following effects will be observed:

Specification	Effect as I_{cc} decreases
bandwidth	decreases
rise time	increases
output drive	decreases
input bias current	decreases
input impedance	increases (see source impedance discussion)

Both the specification pages and the plot pages illustrate these effects to help make the supply current vs. performance tradeoff. Performance is specified and tested at I_{cc} = 1mA, 3.4mA, and 9mA as indicated in the data sheet. (Note some test conditions and especially the load resistance are different for the three supply current settings.) The performance plots show typical performance for all three supply current levels (again, with different load resistors for the various supply currents). Finally, the last set of plots show graphically the relationship between the supply current (I_{cc}) and various performance parameters, as well as I_{cc} vs. the programming current, I_p.

When making the supply current vs. performance tradeoff, it is first a good idea to see if one of the standard operating points (I_{cc} = 9mA, 3.4mA, or 1mA) fits your application. If it does, performance guaranteed on the specification pages will apply directly to your application. In addition, the value of R_p may be obtained directly from the specification page.

The following discussion will assist in selecting I_{cc} for applications that cannot operate at one of the specified supply current settings.

The typical performance plots should be used to select a value of I_{cc} suitable to your application's TYPICAL requirement for critical specifications. Then, use the performance plots and the max/min limits on the specification pages to interpolate between values of I_{cc} to estimate max/min values in your application.

From the selected value of I_{cc}, the "programming current" (I_p) may be easily calculated:

$$I_p = I_{cc} / 39$$

The plot of I_{cc} vs I_p in the plot pages shows this relationship graphically. Knowing I_p leads to a direct calculation of R_p

$$R_p = [(+V_{cc}\text{-}1.6)\text{-}V_n] / I_p$$

$$R_p = 8.4/I_p \text{ (for } +V_{cc} = +5V \text{ and } V_n = -5V)$$

V_n is the voltage externally applied to R_p. (Throughout the data sheet and in most applications, V_n is $-V_{cc}$ or more specifically, -5V.) The term ($+V_{cc}$-1.6V) is the voltage at pin 8.

Since the op amp side of R_p is very nearly at a fixed voltage (V_{cc}-1.6V), I_p is a function of V_n and R_p. V_n, therefore does not have to be connected to $-V_{cc}$ as long as R_p is chosen accordingly. This is beneficial in applications where non-standard supply voltages are used or when there is a need to power down the op amp via digital logic control.

First, an operating point needs to be established as discussed above. From this, I_p is obtained. I_p, in concert with the available V_n, determines R_p.

Example

An application requires that V_{cc} = +/-3V and performance in the 1mA operating point range. The required I_p can therefore be determined as discussed above.

$$I_p = 26\mu A$$

R_p is connected from pin 8 to $-V_{cc}$ and V_{cc} = +/-3V. Now calculate R_p under new conditions:

$$R_p = [(+V_{cc}\text{-}1.6V)\text{-}(-V_{cc})] / I_p$$

$$R_p = [(+3V\text{-}1.6V)\text{-}(-3V)] / 26\mu A$$

$$R_p = 169k\Omega$$

The CLC505 will have performance similar to $R_p = 300k\Omega$ shown on the datasheet, but with 40% less power dissipation due to the reduced supply voltages. (The op-amp will also have a more restricted common-mode range and output swing.) This calculation is approximate and a prudent design would include substantial performance margin for max/min limits. Comlinear application engineers are available for assistance.

Dynamic Shutdown Capability

The CLC505 may be powered on and off very quickly by controlling the voltage applied to R_p. If R_p is connected between pin 8 and the output of a CMOS gate powered from +/-5V supplies, the gate can be used to turn the amplifier on and off. This is shown in figure 3 below:

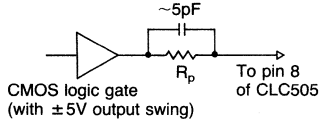


Figure 3: dynamic control of power consumption

When the gate output is switched from high to low, the CLC505 will turn on. In the off state, the supply current typically reduces to 0.2mA or less. The speed with which the CLC505 turns on or off is limited by the capacitance at pin 8. To improve switching time, a speed up capacitor from the gate output to pin 8 is recommended. The value of this capacitor will depend on the total capacitance connected to pin 8 and is best established experimentally. Turn-on and turn-off times of 100ns to 200ns are achievable with ordinary CMOS gates.

Example:

An open collector logic device is used to dynamically control the power dissipation of the circuit. Here, the desired connection for R_p is from pin 8 to the open collector logic device.

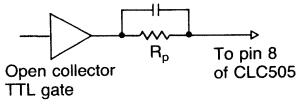


Figure 4: controlling power on state with TTL logic

When the logic gate goes low, the CLC505 is turned on. Performance desired is that given for $I_{cc}=3.4mA$ under standard conditions. From the I_{cc} vs I_p plot, $I_p=84\mu A$. Then calculating R_p:

$$R_p = [(+V_{cc}-1.6V)-(V_n)]/I_p$$
$$R_p = [(+5V-1.6V)-(0)]84\mu A$$
$$R_p = 40k\Omega$$

NOTE: The rapid turn on and off ability of the CLC505 is not recommended for signal isolation applications (such as multiplexing). While the power dissipation of the amplifier drops in the off state, the amplifier may still have some gain at low frequencies.

Slew Rate

Slew rate limiting is a nonlinear response which occurs in amplifiers when the output voltage swing approaches hard, abrupt limits in the speed at which it can change. In most applications, this results in an easily identifiable "slew rate" as well as a dramatic increase in distortion for large signal levels. The CLC505 has been designed to provide enough slew rate to avoid slew rate limiting in most circuit configurations. The large signal ($5V_{pp}$) bandwidth of 80MHz at $I_{cc}=3.4mA$, therefore, is only slightly less than the 100MHz small signal bandwidth. The result is a low-distortion, linear system for both small signals *and* large signals.

The CLC505 reaches slew rate limits only for low non-inverting gains. In other words, slew rate limiting is constrained by common mode voltage swings at the input. (This is different from traditional slew rate constraints.) The large-signal frequency response plot at a gain of +2 shows a break in the response, which shows that a slew rate limit has been reached. Note also that the frequency response plots at gain of +21 show that the large signal and small signal responses are nearly identical.

Differential Gain and Phase

Differential gain and phase are measurements useful primarily in composite video channels. They are measured by monitoring the gain and phase changes of a high frequency carrier (3.58MHz typically) as the output of the amplifier is swept over a range of DC voltages.

Specifications for the CLC505 include differential gain and phase. The test signals used are based on a $1V_{pp}$ video level. Test conditions used are the following:

DC sweep range:	0 to 100 IRE units (black to white)
Carrier:	3.58MHz at 40 IRE units peak to peak

The amplifier conditions are significantly different for the three values of supply current specified. At $I_{cc}=9mA$, the amplifier is specified for a gain of +2 and 150Ω load (for a backmatched 75Ω system). IRE amplitudes at $I_{cc}=9mA$, are referred to the 75Ω load resistor.

At $I_{cc}=1mA$ and $I_{cc}=3.4mA$, the CLC505 is less capable of driving a 150Ω load due to output current limitations. For this reason lighter loads are used and a termination resistor is omitted. The gain and load resistance for $I_{cc}=3.4mA$ are $A_v=+6$ and $R_L=500\Omega$. The gain and load resistance for $I_{cc}=1mA$ are $A_v=+6$ and $R_L=1K\Omega$.

Source Impedance

For best results, source impedance in the non-inverting circuit configuration (see Figure 1) should be kept below 5kΩ. Above 5kΩ it is possible for oscillation to occur, depending on other circuit parasitics. For high signal source impedances, a resistor with a value of less than 5kΩ may be used to terminate the non-inverting input to ground.

Feedback Resistor

In current-feedback op amps, the value of the feedback resistor plays a major role in determining amplifier dynamics. It is important to select the correct value resistor. The CLC505 provides optimum performance with a 1kΩ feedback resistor. Furthermore, the specifications shown on the previous pages are valid only when a 1kΩ feedback resistor is used. Selection of an incorrect value can lead to severe rolloff in frequency response (if the resistor value is too large) or peaking or oscillation (if the value is too low). See Comlinear application notes AN and AN 300-1 for a complete discussion of current feedback.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC505 are available.

High-Power Amplifiers
Contents

Comlinear Corporation

Wideband, Low Distortion DriveR-*amps*

CLC560

APPLICATIONS:

- output amplification
- arbitrary waveform generation
- ATE systems
- cable/line driving
- function generators
- SAW drivers
- flash A/D driving and testing

FEATURES:

- 120MHz bandwidth at +24dBm output
- low distortion (2nd/3rd: -60/-62dBc @ 20MHz and 10dBm)
- output short circuit protection
- user-definable output impedance, gain, and compensation
- internal current limiting

DESCRIPTION:

The CLC560 is a wideband dc coupled, amplifier that combines high output drive and low distortion. At an output of +24dBm ($10V_{pp}$ into 50Ω), the –3dB bandwidth is 120MHz. As illustrated in the table below, distortion performance remains excellent even when amplifying high-frequency signals to high output power levels.

Typical Distortion Performance

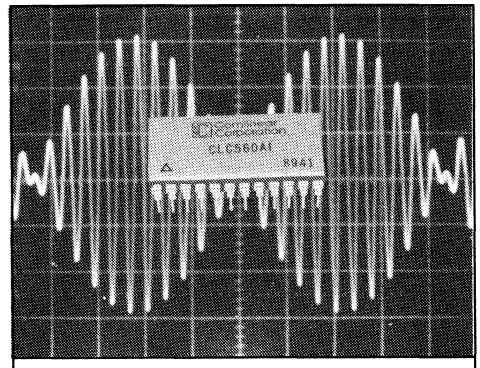
Output Power	20MHz 2nd	20MHz 3rd	50MHz 2nd	50MHz 3rd	100MHz 2nd	100MHz 3rd
10dBm	-60	-62	-50	-54	-54	-44
18dBm	-51	-48	-40	-40	-36	-29
24dBm	-46	-38	-33	-25		

With the output current internally limited to 250mA, the CLC560 is fully protected against shorts to ground and can, with the addition of a series limiting resistor at the output, withstand shorts to the ±15V supplies.

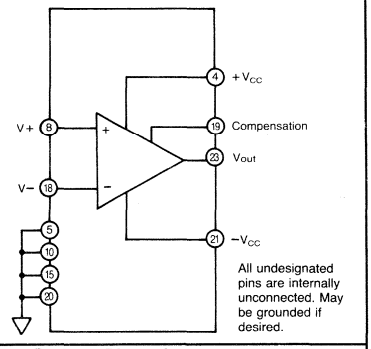
The CLC560 has been designed for maximum flexibility in a wide variety of demanding applications. The two resistors comprising the feedback network set both the gain and the output impedance, without requiring the series backmatch resistor needed by most op amps. This allows driving into a matched load without dropping half the voltage swing through a series matching resistor. External compensation allows user adjustment of the frequency response. The CLC560 is specified for both maximally flat frequency response and 0% pulse overshoot compensations.

The combination of wide bandwidth, high output power, and low distortion, coupled with gain, output impedance and frequency response flexibility, makes the CLC560 ideal for waveform generator applications. Excellent stability driving capacitive loads yields superior performance driving ADC's, long transmission lines, and SAW devices. A companion part, the CLC561, offers higher full power bandwidth for broadband sinusoidal applications.

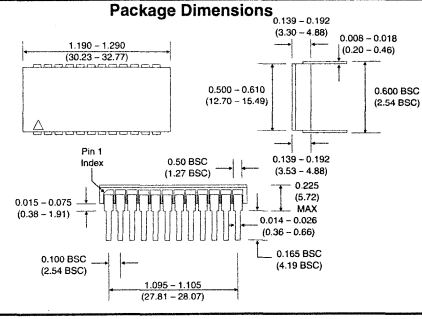
The CLC560 is constructed using thin film resistor/bipolar transistor technology. The CLC560AI is specified over a temperature range of –25°C to +85°C, while the CLC560A8C is specified over a range of –55°C to +125°C and is fully compliant with MIL-STD-883, Level B. Both devices are packaged in 24-pin, 600 mil wide, ceramic DIPs. The DESC SMD number is 5962-90756.



Pinout



Package Dimensions



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Electrical Characteristics ($A_V = +10$, $V_{CC} = \pm 15V$, $R_f = 410\Omega$, $R_g = 40\Omega$, $R_O = 50\Omega$, $R_L = 50\Omega$)

NOTES TO THE ELECTRICAL SPECIFICATIONS

The electrical characteristics shown here apply to the specific test conditions shown above (see also Figure 1 in description of the operation). The CLC560 provides an equivalent, non-zero, output impedance determined by the external resistors. The signal gain to the load is therefore load dependent. **The signal gain shown above ($A_V = +10$) is the no load gain.** The actual gain to the matching 50 ohm load used in these specifications is half of this (+5).

The CLC560 requires an external compensation capacitor. Unless otherwise noted, this has been set to 10.5pF for the frequency domain specifications (yielding a maximally flat frequency response) and 12.5pF for the time domain specifications (yielding a 0% small signal pulse overshoot response).

Parameters preceded by an * are the final electrical test parameters and are 100% tested at 25°C on all versions. The A8C grade part is also 100% tested at -55°C and 125°C case temperature.

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Case Temperature	CLC560A8	+25°C	−55°C	+25°C	+125°C		
Case Temperature	CLC560AI	+25°C	−25°C	+25°C	+ 85°C		
FREQUENCY DOMAIN (Maximally Flat Compensation)							
−3dB bandwidth							
*maximally flat compensation	$V_{OUT}<2V_{pp}$ (+10dBm)	215	>175	>185	>175	MHz	SSBW
0% overshoot compensation	$V_{OUT}<2V_{pp}$ (+10dBm)	210	>170	>180	>170	MHz	
large signal bandwidth	$V_{OUT}<10V_{pp}$ (+24dBm)	120	>115	>100	>90	MHz	FPBW
(see Frequency Response vs. Output Power plot)							
gain flatness	$V_{OUT}<2V_{pp}$ (+10dBm)						
* peaking	0.1 - 50MHz	0	<0.50	<0.40	<0.50	dB	GFPL
* peaking	>50MHz	0	<1.25	<0.75	<1.00	dB	GFPH
* roll off at	100MHz	0.1	<1.00	<0.75	<1.00	dB	GFR
group delay	to 100MHz	3.1	—	—	—	ns	GD
linear phase deviation	to 100MHz	0.6	<1.7	<1.2	<2.7	°	LPD
return loss (see discussion of R_X)	to 100MHz	−15	<−12	<−12	<−12	dB	RL
DISTORTION (Maximally Flat Compensation)							
2nd harmonic distortion							
*24dBm ($10V_{pp}$):	20MHz	−46	<−36	<−36	<−33	dBc	HD2HL
*	50MHz	−33	<−27	<−27	<−27	dBc	HD2HM
*18dBm ($5V_{pp}$):	20MHz	−51	<−44	<−44	<−42	dBc	HD2ML
*	50MHz	−40	<−35	<−35	<−30	dBc	HD2MM
*	100MHz	−36	<−25	<−28	<−26	dBc	HD2MH
*10dBm ($2V_{pp}$):	20MHz	−60	<−54	<−54	<−50	dBc	HD2LL
*	50MHz	−50	<−43	<−43	<−40	dBc	HD2LM
*	100MHz	−54	<−32	<−32	<−32	dBc	HD2LH
3rd harmonic distortion							
*24dBm ($10V_{pp}$):	20MHz	−38	<−32	<−32	<−25	dBc	HD3HL
*	50MHz	−25	<−21	<−21	<−20	dBc	HD3HM
*18dBm ($5V_{pp}$):	20MHz	−48	<−42	<−45	<−42	dBc	HD3ML
*	50MHz	−40	<−36	<−36	<−30	dBc	HD3MM
	100MHz	−29	<−25	<−25	<−25	dBc	HD3MH
*10dBm ($2V_{pp}$):	20MHz	−62	<−58	<−58	<−57	dBc	HD3LL
*	50MHz	−54	<−50	<−50	<−48	dBc	HD3LM
	100MHz	−44	<−40	<−40	<−36	dBc	HD3LH
2-tone 3rd order intermod intercept[1]	20MHz	40	>38	>38	>38	dBm	IM3L
	50MHz	35	>32	>32	>32	dBm	IM3M
	100MHz	25	>23	>23	>20	dBm	IM3H

Electrical Characteristics (A_V = +10, V_{CC} = ±15V, R_f = 410Ω, R_g = 40Ω, R_O = 50Ω, R_L = 50Ω)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Case Temperature	CLC560A8	+25°C	−55°C	+25°C	+125°C		
Case Temperature	CLC560AI	+25°C	−25°C	+25°C	+ 85°C		
TIME DOMAIN (0% Overshoot Compensation)							
rise and fall time							
2V step		1.6	<2.0	<1.9	<2.0	ns	TRS
10V step		3.6	<3.8	<4.5	<5.3	ns	TRL
settling time to 0.1% (time<1μs)	5V step	10	<15	<15	<25	ns	TS
long term thermal tail (time>1μs)	5V step	0.4	<0.5	<0.5	<0.5	%	SE
slew rate	$10V_{pp}$, 175MHz	2600	>2300	>2000	>1800	V/μs	SR
overshoot	2V step						
maximally flat compensation		5	<13	<10	<13	%	OSMF
0% overshoot compensation		0	<5	<3	<5	%	OSZO
EQUIVALENT INPUT NOISE							
voltage	>100KHz	2.1	<2.5	<2.5	<2.5	nV/√Hz	VN
inverting current	>100KHz	34	<40	<40	<45	pA/√Hz	ICN
non-inverting current	>100KHz	2.8	<4.5	<4.5	<5.0	pA/√Hz	NCN
noise floor	>100KHz	−159	<−157	<−157	<−157	dBm/(1Hz)	SNF
integrated noise	1kHz to 200MHz	35	<45	<45	<45	μV	INV
noise figure	>100KHz	15	<17	<17	<17	dB	NF
STATIC, DC							
*input offset voltage		2.0	<14.0	<5.0	<15.0	mV	VIO
average temperature coefficient		35	<100	—	<100	μV/°C	DVIO
*non-inverting bias current		5.0	<35	<20	<20	μA	IBN
average temperature coefficient		20	<175	—	<100	nA/°C	DIBN
*inverting bias current		10.0	<50	<30	<50	μA	IBI
average temperature coefficient		100	<200	—	<200	nA/°C	DIBI
*power supply rejection ratio (DC)		60	>58	>58	>57	dB	PSRR
*supply current	no load	50	<60	<60	<65	mA	ICC
MISCELLANEOUS							
open loop current gain	(± 2% tolerance)	10.0	—	—	—	mA/mA	G
average temperature coefficient		+0.02	<+.03	—	<+.02	%/°C	DG
inverting input resistance	(±5% tolerance)	14.0	—	—	—	Ω	RIN
average temperature coefficient		+.02	<+.025	—	<+.025	Ω/°C	DRIN
non-inverting input resistance		700	>200	>400	>400	KΩ	RNI
non-inverting input capacitance	to 100MHz	2.3	<3.0	<3.0	<3.0	pF	CNI
output voltage range @ 150mA load current		±10.5	>10.0	>10.0	>10.0	V	VO
output current limit		210	<250	<250	<250	ma	OCL

Absolute Maximum Ratings

$\pm V_{CC}$ (reversed supplies will destroy part)	±20V
differential input voltage	±3V
common mode input voltage	$\pm V_{CC}$
junction temp. (see thermal model)	+175°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C
output current (internally limited)	±250mA

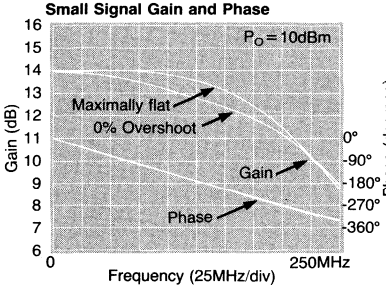
Recommended Operating Conditions

$\pm V_{CC}$	±10 to ±15
I_{out}	≤±200mA
common mode input voltage	$<\pm(\lvert V_{CC}\rvert - 6)V$
output impedance	25Ω to 200Ω
gain range (no-load voltage gain)	+5 to +80
case temp. AI	−25°C to +85°C
A8	−55°C to +125°C

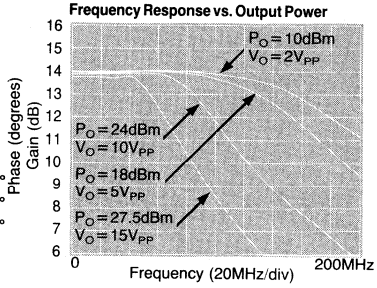
NOTES:
1. Test tones are set ±100kHz of indicated frequency.

Typical Performance Characteristics (T_A = 25°C, Circuit of Figure 1 unless otherwise specified)

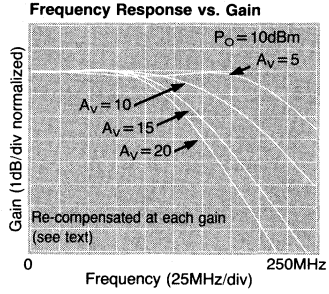
Small Signal Gain and Phase



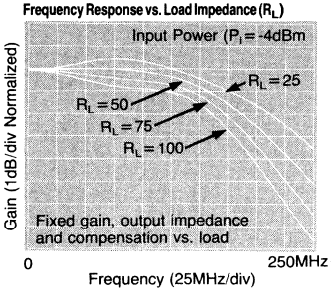
Frequency Response vs. Output Power



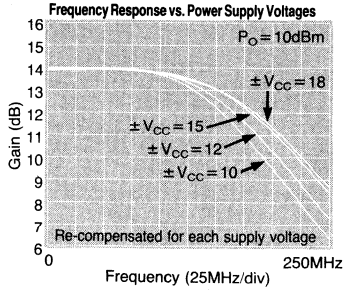
Frequency Response vs. Gain



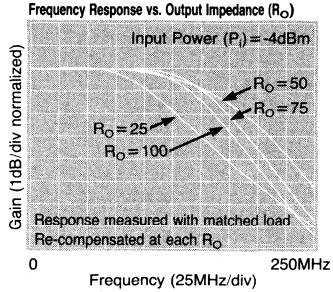
Frequency Response vs. Load Impedance (R_L)



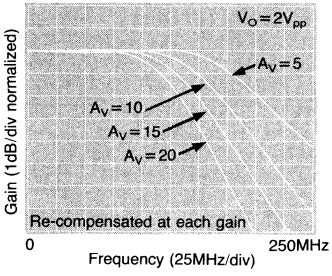
Frequency Response vs. Power Supply Voltages



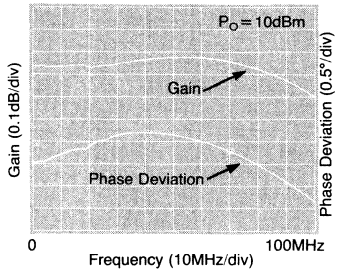
Frequency Response vs. Output Impedance (R_O)



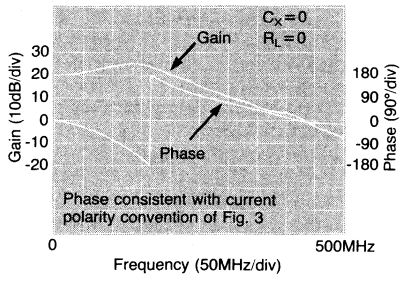
Frequency Response vs. Gain with R_O = R_L = 75Ω



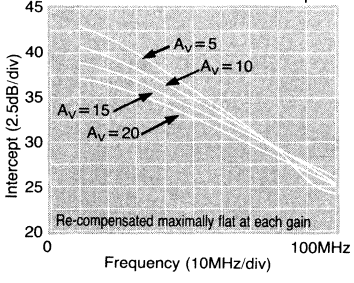
Gain Flatness and Deviation from Linear Phase



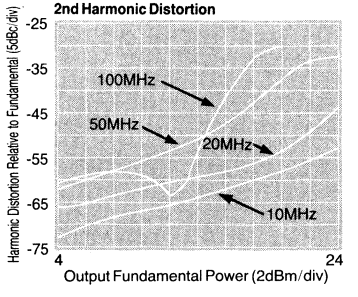
Internal Current Gain and Phase



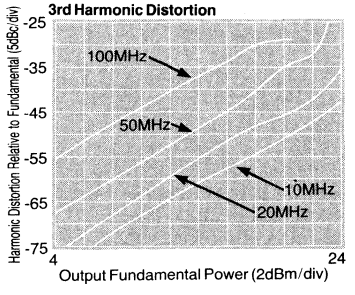
Two Tone, 3rd-Order Intermodulation Intercept



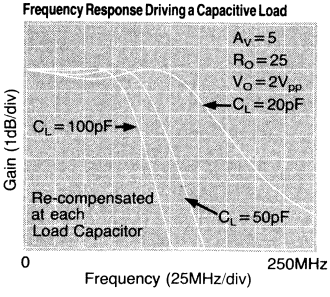
2nd Harmonic Distortion



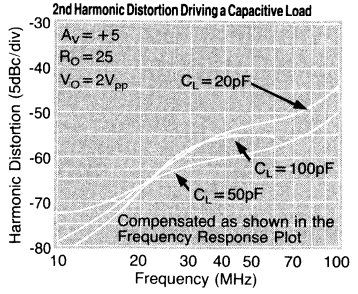
3rd Harmonic Distortion



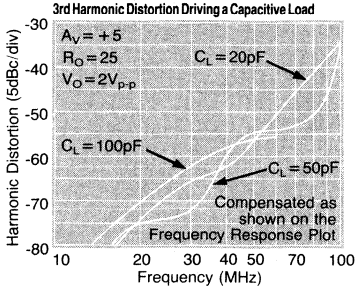
Frequency Response Driving a Capacitive Load



2nd Harmonic Distortion Driving a Capacitive Load

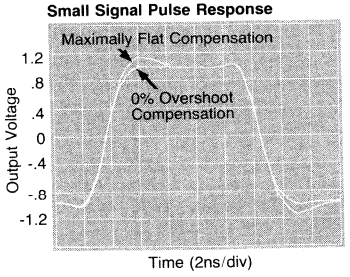


3rd Harmonic Distortion Driving a Capacitive Load

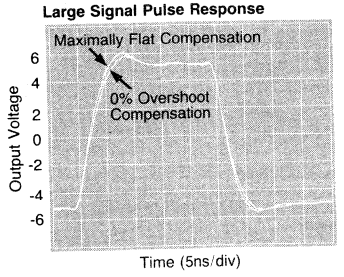


Typical Performance Characteristics (T_A = 25°C, Circuit of Figure 1 unless otherwise specified)

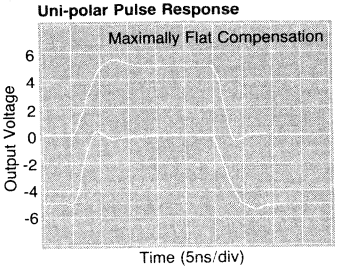
Small Signal Pulse Response



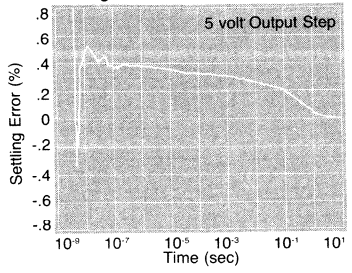
Large Signal Pulse Response



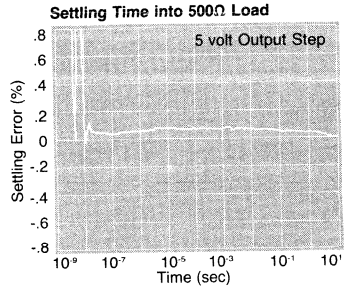
Uni-polar Pulse Response



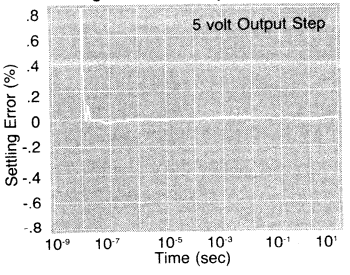
Settling Time into 50Ω Load



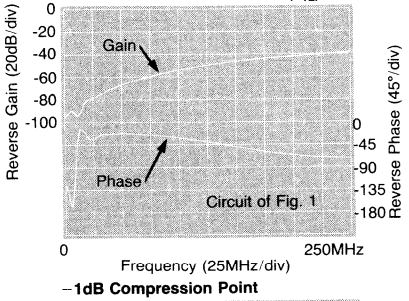
Settling Time into 500Ω Load



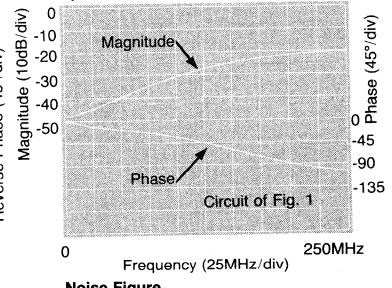
Settling Time into a 50pF Load



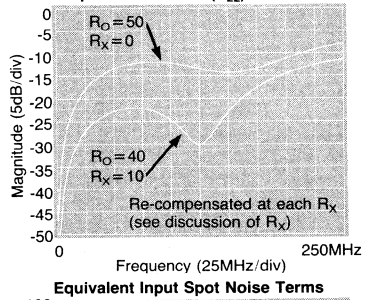
Reverse Transmission Gain and Phase (S_{12})



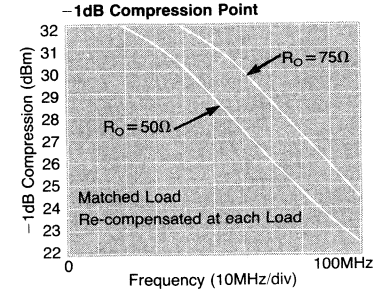
Input Return Loss (S_{11})



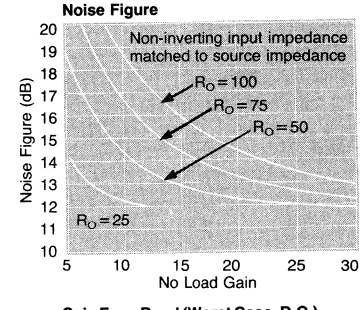
Output Return Loss (S_{22})



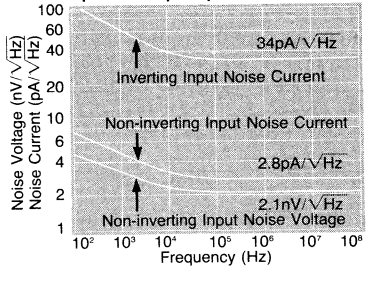
–1dB Compression Point



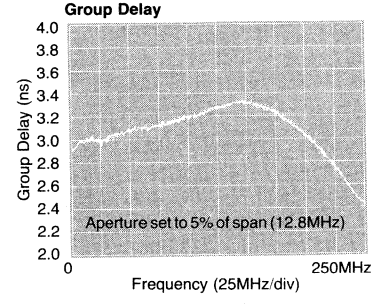
Noise Figure



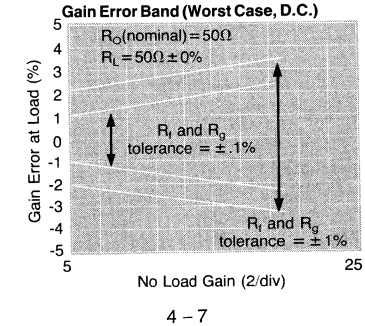
Equivalent Input Spot Noise Terms



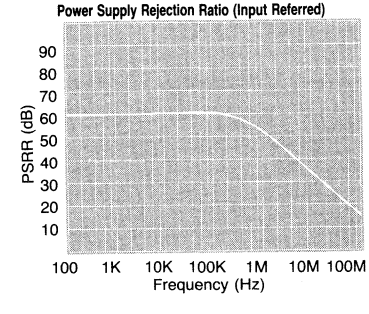
Group Delay



Gain Error Band (Worst Case, D.C.)



Power Supply Rejection Ratio (Input Referred)



SUMMARY DESIGN EQUATIONS AND DEFINITIONS

$$R_f = (G + 1)\,R_o - A_V\,R_i$$ — R_f – Feedback resistor from output to inverting input

$$R_g = \frac{R_f - R_o}{A_v - 1}$$ — R_g – Gain setting resistor from inverting input to ground

$$C_x = \frac{1}{\frac{R_o}{300\left(1 - \frac{2}{R_g}\right)} - .08}$$ — C_x – External compensation capacitor from output to pin 19 (in pF)

Where:

R_o – Desired equivalent output impedance
A_v – Non-inverting input to output voltage gain with no load
G – Internal current gain from inverting input to output = 10 ± 1%
R_i – Internal inverting input impedance = 14Ω ± 5%

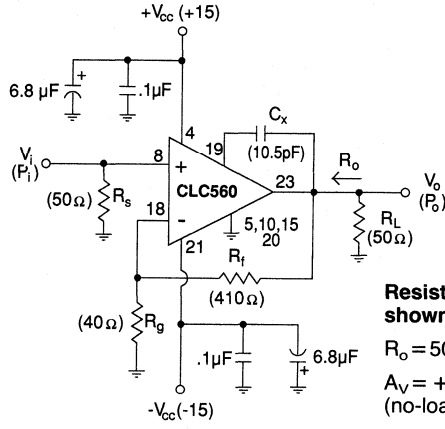
and

R_s – Non-inverting input termination resistor
R_L – Load Resistor
A_L – Voltage gain from non-inverting input to load resistor

CLC560 Description of Operation

Looking at the circuit of Figure 1 (the topology and resistor values used in setting the data sheet specifications), the CLC560 appears to bear a strong external resemblance to a classical op amp. As shown in the simplified block diagram of Figure 2, however, it differs in several key areas. Principally, the error signal is a current into the inverting input (current feedback) and the forward gain from this current to the output is relatively low, but very well controlled, current gain. The CLC560 has been intentionally designed to have a low internal gain and a current mode output in order that an equivalent output impedance can be achieved without the series matching resistor more commonly required of low output impedance op amps. Many of the benefits of a high loop gain have, however, been retained through a very careful control of the CLC560's internal characteristics.

The feedback and gain setting resistors determine both the output impedance and the gain. R_f predominately sets the output impedance (R_o), while R_g predominately determines the no load gain (A_v). Solving for the required R_f and R_g, given a desired R_o and A_v, yields the design equations shown below. Conversely, given an R_f and R_g, the performance equations show that both R_f and R_g play a part in setting R_o and A_v. Independent R_o and A_v adjustment would be possible if the inverting input impedance (R_i) were 0 but, with $R_i = 14\Omega$ as shown in the specification listing, independent gain and output impedance setting is not directly possible.



Resistor Values shown result in:

$R_o = 50\Omega$

$A_V = +10$ (no-load gain)

$A_L = +5$[14dB] (gain to 50Ω load)

Figure 1: Test Circuit

Design Equations

$$R_f = (G+1)\,R_o - A_V\,R_i$$

$$R_g = \frac{R_f - R_o}{A_v - 1}$$

Where:

G≡forward current gain (=10)
R_i≡inverting node input resistance (=14Ω)
R_o≡desired output impedance
A_v≡desired non-inverting voltage gain with no load

Performance Equations

$$R_o = \frac{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}{G + 1 + \frac{R_i}{R_g}}$$

$$A_v = 1 + \frac{R_f}{R_g}\left[\frac{G - \frac{R_i}{R_f}}{G + 1 + \frac{R_i}{R_g}}\right]$$

Simplified Circuit Description

Looking at the CLC560's simplified schematic in Figure 2, the amplifier's operation may be described. Going from the non-inverting input at pin 8 to the inverting input at pin 18, transistors Q1 - Q4 act as an open loop unity gain buffer forcing the inverting node voltage to follow the non-inverting voltage input.

Transistors Q3 and Q4 also act as a low impedance (14Ω looking into pin 18) path for the feedback error current. This current, (i_{err}), flows through those transistors into a very well defined current mirror having a gain of 10 from this error current to the output. The current mirror outputs act as the amplifier output.

The input stage bias currents are supply voltage independent. Since these set the bias level for the whole part, relatively constant performance over supply voltage is achieved. A current sense in the error current leg of the 10X current mirror feeds back to the bias current setup providing a current shutdown feature when the output current approaches 250mA.

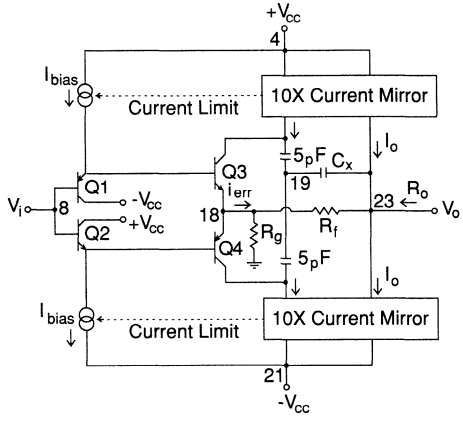
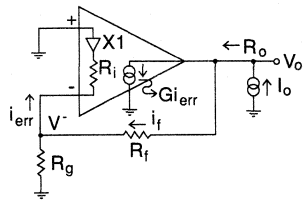


Figure 2: Simplified Circuit Diagram



Get both V_o and I_o into terms of just the error current, i_{err}, using

$V^- = i_{err} R_i$ and

$$i_f = i_{err} + \frac{V^-}{R_g} = i_{err}\left(1 + \frac{R_i}{R_g}\right)$$

$$V_o = V^- + i_f R_f = i_{err}\left[R_i + R_f\left(1 + \frac{R_i}{R_g}\right)\right]$$

$$V_o = i_{err}\left[R_f + R_i\left(1 + \frac{R_f}{R_g}\right)\right]$$

and

$$I_o = Gi_{err} + i_f = i_{err}\left[G + 1 + \frac{R_i}{R_g}\right]$$

then

$$R_o \equiv \frac{V_o}{I_o} = \frac{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}{G + 1 + \frac{R_i}{R_g}}$$

$$\text{note that } R_o\Big|_{R_i=0} = \frac{R_f}{G+1}$$

Figure 3: Output Impedance Derivation

Developing the Performance Equations

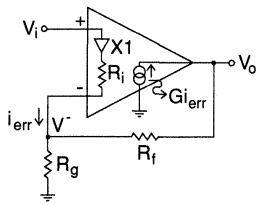
The CLC560 is intended to provide both a controllable voltage gain from input to output as well as a controllable output impedance. It is best to treat these two operations separately with no load in place. Then, with the no-load gain and output impedance determined, the gain to the load will simply be the no-load gain attenuated by the voltage divider formed by the load and the equivalent output impedance.

Figure 3 steps through the output impedance development using an equivalent model of Figure 2. Offering an equivalent, non-zero, output impedance into a matched load allows the CLC560 to operate at lower internal voltage swings for a given desired swing at the load. This allows higher voltage swings to be delivered at the load for a given power supply voltage at lower distortion levels than an equivalent op amp needing to generate twice the voltage swing actually desired at the matched load. This improved distortion is specified and tested over a wide range as shown in the specification listing.

Note that the R_o expression simplifies considerably if $R_i = 0$. Also note that if the forward current gain were to go to infinity, the output impedance would go to 0. This would be the normal op amp topology with a very high internal gain. **The CLC560 achieves a non-zero R_o by setting the internal forward gain to be a low, well controlled, value.**

Developing the No-Load Gain Expression

Taking the output impedance expression as one constraint setting the external resistor values, we now need to develop the no-load voltage gain expression from the non-inverting input to the output as the other constraint. Figure 4 shows the derivation of the no load gain.



No load gain

$$A_v \equiv \frac{V_o}{V_i}$$

Recognize that [taking V_i positive]

$$V_o = V^- + Gi_{err} R_f$$

Solving for V^- from two directions

$$V^- = V_i - i_{err} R_i = (G+1)\, i_{err} R_g$$

solving for i_{err} from this

$$i_{err} = \frac{V_i}{(G+1) R_g + R_i}$$

then

$$V^- = V_i - \frac{V_i R_i}{(G+1) R_g + R_i}$$

and, substituting for V^- and i_{err} in the original V_o expression

$$V_o = V_i - \frac{V_i R_i}{(G+1) R_g + R_i} + \frac{GR_f V_i}{(G+1) R_g + R_i}$$

which simplifies to

$$V_o = V_i \left[1 + \frac{GR_f - R_i}{(G+1) R_g + R_i} \right]$$

pulling an $\frac{R_f}{R_g}$ out of the fraction

$$A_v \equiv \frac{V_o}{V_i} = 1 + \frac{R_f}{R_g} \left[\frac{G - \frac{R_i}{R_f}}{G+1+\frac{R_i}{R_g}} \right]$$

note that $A_v \Big|_{R_i=0} = 1 + \frac{R_f}{R_g} \left(\frac{G}{G+1} \right)$

Figure 4: Voltage Gain Derivation

Note again that if $R_i = 0$ this expression would simplify considerably. Also, if G were very large the voltage gain expression would reduce to the familiar non-inverting op amp gain equation. These two performance equations, shown below, provide a means to derive the design equations for R_f and R_g given a desired no load gain and output impedance. The details of that derivation may be found in Application Note OA-10.

Performance Equations

$$R_o = \frac{R_f + R_i \left(1 + \frac{R_f}{R_g}\right)}{G+1+\frac{R_i}{R_g}}$$

$$A_v = 1 + \frac{R_f}{R_g} \left[\frac{G - R_i/R_f}{G+1+R_i/R_g} \right]$$

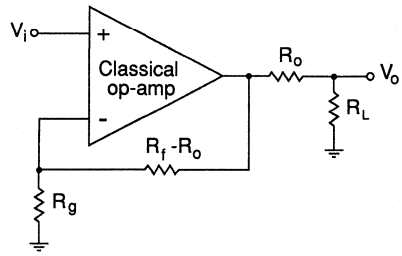
Design Equations

$$R_f = (G+1)\, R_o - A_v R_i$$

$$R_g = \frac{R_f - R_o}{A_v - 1}$$

Equivalent Model

Given that the physical feedback and gain setting resistors have been determined in accordance with the design equations shown above, an equivalent model may be created for the gain to the load where the amplifier block is taken as a standard op amp. Figure 5 shows this analysis model and the resulting gain equation to the load.



$$\frac{V_o}{V_i} = \left(1 + \frac{R_f - R_o}{R_g} \right) \frac{R_L}{R_L + R_o}$$

Substituting in for R_f and R_g with their design equation yields

$$\frac{V_o}{V_i} = A_v \frac{R_L}{R_L + R_o} = A_L \text{ (gain to load)}$$

Figure 5: Equivalent Model

This model is used to generate the DC error and noise performance equations. As with any equivalent model, the primary intent is to match the external terminal characteristics recognizing that the model distorts the internal currents and voltages. In this case, the model would incorrectly predict the output pin voltage swing for a given swing at the load. But it does provide a simplified means of getting to the external terminal characteristics.

External Compensation Capacitor (C_x)

As shown in the test circuit of Figure 1, the CLC560 requires an external compensation capacitor from the output to pin 19. The recommended values described here assume that a maximally flat frequency response into a matched load is desired. The required C_x varies widely with the desired value of output impedance and to a lesser degree on the desired gain. Note from Figure 2, the simplified internal schematic, that the actual total compensation (C_t) is the series combination of C_x and the internal 10pF from pin 19 to the compensation nodes. The total compensation (C_t) is developed in two steps as shown below.

$$C_1 = \frac{300}{R_o} \left(1 - \frac{2.0}{R_g} \right) \text{ pF intermediate equation}$$

$$C_t = \frac{C_1}{1 + (.02)\, C_1} \text{ pF total compensation}$$

With this total value derived, the required external C_x is developed by backing out the effect of the internal 10pF. This, and an expression for the external C_x without the intermediate steps are shown below.

$$C_x = \frac{10\ C_t}{10 - C_t}$$

or

$$C_x = \frac{1}{\frac{R_o}{300\left(1-\frac{2}{R_g}\right)} - .08}\ \text{pF}$$

The plot of Figure 6 shows the required C_x vs. gain for several desired output impedances using the equations shown above. Note that for lower R_o's, C_x can get very large. But, since the total compensation is actually the series combination of C_x and 10pF, going to very high C_x's is increasingly ineffective as the total compensation is only slightly changed. This, in part, sets the lower limits on allowable R_o.

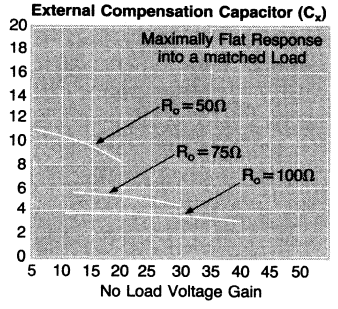


Figure 6: External Compensation Capacitance (C_x)

A 0% small signal overshoot response can be achieved by increasing C_x slightly from the maximally flat value. Note that this applies only for small signals due to slew rate effects coming into play for large, fast edge rates.

Beyond the nominal compensation values developed thus far, this external C_x provides a very flexible means for tailoring the frequency response under a wide variety of gain and loading conditions. It is oftentimes useful to use a small adjustable cap in development to determine a C_x suitable to the application, then fixing that value for production. An excellent 5pF to 20pF trimmer cap for this is a Sprague-Goodman part #GKX20000.

When the CLC560 is used to drive a capacitive load, such as an ADC or SAW device, the load will act to compensate the response along with C_x. Generally, considerably lower C_x values are required than the earlier development would indicate. This is advantageous in that a low R_o would be desired to drive a capacitive load which, without the compensating effect of load itself, would otherwise require very large C_x values.

Gain and Output Impedance Range

Figure 7 shows a plot of the recommended gain and output impedances for the CLC560. Operation outside of this region is certainly possible with some degradation in performance. Several factors contribute to set this range. At very low output impedances, the required value of feedback resistor becomes so low as to excessively load the output causing a rapid degradation in distortion. The maximum R_o was set somewhat arbitrarily at 200Ω. This allows the CLC560 to drive into a 2:1 step down transformer matching to a 50Ω load. (This offers some advantages from a distortion standpoint. See Application Note OA-10 for details.)

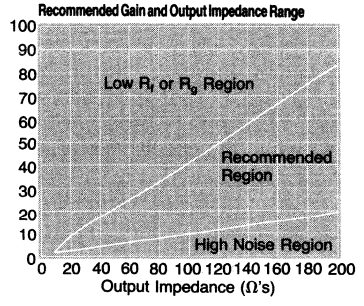


Figure 7: Recommended Gain and Output Impedance Range

For a given R_o, the minimum gain shown in Figure 7 has been set to keep the equivalent input noise voltage less than $4nV/\sqrt{Hz}$. Generally, the equivalent input noise voltage decreases with higher signal gains. The high gain limit has been set by targeting a minimum R_g of 10Ω or a minimum R_f of 100Ω.

Amplifier Configurations (Additional discussion in Application Note OA-10)

The CLC560 is intended for a fixed, non-inverting, gain configuration as shown in Figure 1. The CLC561 offers an enhanced slew rate at the expense of higher long-term thermal tail in the pulse response than the CLC560. Due to its low internal forward gain, the inverting node **does not** present a low impedance, or virtual ground, node. Hence, in an inverting configuration, the signal's source impedance will see a finite load whose value depends on the output loading. Inverting mode operation can be best achieved using a wideband, unity gain buffer with low output impedance, such as the CLC110, to isolate the source from this varying load. A DC level can, however, be summed into the inverting node to offset the output either for offset correction or signal conditioning. Application Note OA-10 describes this and a composite amplifier structure that enhances the DC and gain accuracy characteristics of the CLC560.

Accuracy Calculations

Several factors contribute to limit the achievable CLC560 accuracy. These include the DC errors, noise effects, and the impact internal amplifier characteristics have on the signal gain. Both the output DC error and noise model may be developed using the equivalent model of Figure 5. Generally, non-inverting input errors show up at the output with the same gain as the input signal, while the inverting current errors have a gain of simply $(R_f - R_o)$ to the output voltage (neglecting the R_o to R_L attenuation).

Output DC offset:

The DC error terms shown in the specification listing along with the model of Figure 5 may be used to estimate the output DC offset voltage and drift. Each term shown in the specification listing can be of either polarity. While the equations shown below are for output offset voltage, the same equation may be used for the drift with each term replaced by its temperature drift value shown in the specification listing.

Output DC offset

$$V_{os} = \left(I_{bn} \cdot R_s \pm V_{io}\right) \cdot \left(1 + \frac{R_f - R_o}{R_g}\right) \pm I_{bi}\,(R_f - R_o)$$

Where: $I_{bn} \equiv$ non-inverting bias current
$I_{bi} \equiv$ inverting bias current
$V_{io} \equiv$ input offset voltage

An example calculation for the circuit of Figure 1 using typical 25°C DC error terms and $R_s = 25\Omega$ $R_L = 50\Omega$ yields

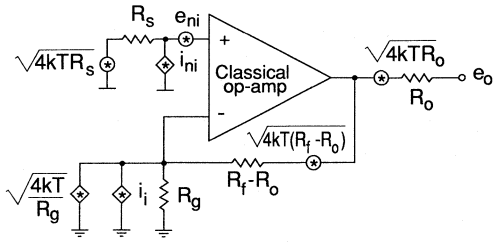
$$V_o\Big|_{DC} = [(5\mu A \cdot 25\Omega \pm 2.0mV)\,10 \pm 10\mu A(360\Omega)]\,\tfrac{1}{2} = \pm 12.4\,mV$$

↑ attenuation between R_o and R_L

Recall that the source impedance, R_s, includes both the terminating and signal source impedance and that the actual DC level to the load includes the voltage divider between R_o and R_L. Also note that for the CLC560, as well as for all current feedback amplifiers, the non-inverting and inverting bias currents do not track each other in either magnitude or polarity. Hence, there is no meaning in an offset current specification, and source impedance matching to cancel bias currents is ineffective.

Noise Analysis:

Although the DC error terms are in fact random, the calculation shown above assumes they are all additive in a worst case sense. The effect of all the various noise sources are combined as a root sum of squared terms to get an overall expression for the spot noise voltage. The circuit of Figure 8 shows the equivalent circuit with all the various noise voltages and currents included along with their gains to the output.



Where:	Gain to e_o
e_{ni} – non-inverting input voltage noise	A_v
i_{ni} – non-inverting input current noise	$A_v R_s$
i_i – inverting input current noise	$R_f - R_o$
$\sqrt{4kTR_s}$ – source resistance voltage noise	A_v
$\sqrt{4kT/R_g}$ – gain setting resistor noise current	$R_f - R_o$
$\sqrt{4kT(R_f - R_o)}$ – feedback resistor voltage noise	1
$\sqrt{4kTR_o}$ – output resistor voltage noise	1

Figure 8

To get an expression for the equivalent output noise voltage, each of these noise voltage and current terms must be taken to the output through their appropriate gains and combined as the root sum of squares.

$$e_o = \sqrt{(e_{ni}^2 + (i_{ni}R_s)^2 + 4kTR_s)\,A_v^2 + i_i^2(R_f - R_o)^2} \cdots \overline{+ 4kT(R_f - R_o)\,A_v + 4kTR_o}$$

Where the $4kT(R_f - R_o)A_v$ term is the combined noise power of R_g and $R_f - R_o$.

It is often more useful to show the noise as an equivalent input spot noise voltage where every term shown above is reflected to the input. This allows a direct measure of the input signal to noise ratio. This is done by dividing every term inside the radical by the signal voltage gain squared. This, and an example calculation for the circuit of Figure 1, are shown below. Note that R_L may be neglected in this calculation.

$$e_n = \sqrt{e_{ni}^2 + (i_{ni}R_s)^2 + 4kTR_s + \frac{i_i^2(R_f - R_o)^2}{A_v^2} + \cdots \overline{\frac{4kT(R_f - R_o)}{A_v} + \frac{4kTR_o}{A_v^2}}}$$

For the circuit of Figure 1, the equivalent input noise voltage may be calculated using the data sheet spot noises and $R_s = 25\Omega$, $R_L = \infty$. Recall that $4kT = 16E{-}21J$. All terms cast as $(nV/\sqrt{Hz})^2$

$$e_n = \sqrt{(2.1)^2 + (.07)^2 + (.632)^2 + (1.22)^2 + (.759)^2 + (.089)^2}$$
$$= 2.62nV/\sqrt{Hz}$$

Gain Accuracy (DC):
A classical op amp's gain accuracy is principally set by the accuracy of the external resistors. The CLC560 also depends on the internal characteristics of the forward current gain and inverting input impedance. The performance equations for A_v and R_o along with the Thevinin model of Figure 5 are the most direct way of assessing the absolute gain accuracy. Note that internal temperature drifts will decrease the absolute gain slightly as the part warms up. Also note that the parameter tolerances affect both the signal gain and output impedance. The gain tolerance to the load must include both of these effects as well as any variation in the load. The impact of each parameter shown in the performance equations on the gain to the load (A_L) is shown below.

Increasing current gain G	Increases A_L
Increasing inverting input R_i	Decreases A_L
Increasing R_f	Increases A_L
Increasing R_g	Decreases A_L

Applications Suggestions

Driving a capacitive load:
The CLC560 is particularly suitable for driving a capacitive load. Unlike a classical op amp (with an inductive output impedance), the CLC560's output impedance, while starting out real at the programmed value, goes somewhat capacitive at higher frequencies. This yields a very stable performance driving a capacitive load. The overall response is limited by the (1/RC) bandwidth set by the CLC560's output impedance and the load capacitance. It is therefore advantageous to set a low R_o with the constraint that extremely low R_f values will degrade the distortion performance. $R_o = 25\Omega$ was selected for the data sheet plots. Note from distortion plots into a capacitive load that the CLC560 achieves better than 60dBc THD (10 bits) driving $2V_{pp}$ into a 50pF load through 30MHz.

Improving the output impedance match vs. frequency – Using R_x:
Using the loop gain to provide a non-zero output impedance provides a very good impedance match at low frequencies. As shown on the Output Return Loss plot, however, this match degrades at higher frequency. Adding a small external resistor in series with the output, R_x, as part of the output impedance (and adjusting the programmed R_o accordingly) provides a much better match over frequency. Figure 9 shows this approach.

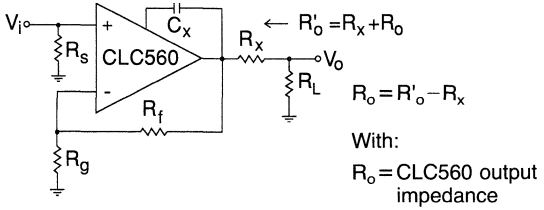


Figure 9

Increasing R_x will decrease the achievable voltage swing at the load. A minimum R_x should be used consistent with the desired output match. As discussed in the thermal analysis discussion, R_x is also very useful in limiting the internal power under an output shorted condition.

Interpreting the Slew Rate:
The slew rate shown in the data sheet applies to the voltage swing at the load for the circuit of Figure 1. Twice this value would be required of a low output impedance amplifier using an external matching resistor to achieve the same slew rate at the load.

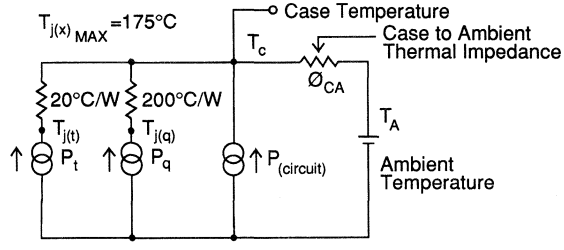
Layout Suggestions:
The fastest fine scale pulse response settling requires careful attention to the power supply de-coupling. Generally, the larger electrolytic capacitor ground connections should be as near the load ground (or cable shield connection) as is reasonable, while the higher frequency ceramic de-coupling caps should be as near the CLC560's supply pins as possible to a low inductance ground plane.

Evaluation Boards and Encased Versions:
An evaluation board (showing a good high frequency layout) for the CLC560 is available. This board may be ordered as part #730019. In addition, encased versions of the CLC560 are also available. These are modular amplifiers similar to Comlinear's other E-series parts.

Thermal Analysis and Protection

A thermal analysis of a chip and wire hybrid is directed at determining the maximum junction temperature of all the internal transistors. From the total internal power dissipation, a case temperature may be developed using the ambient temperature and the case to ambient thermal impedance. Then, each of the dominant power dissipating paths are considered to determine which has the maximum rise above case temperature.

The thermal model and analysis steps are shown below. As is typical, the model is cast as an electrical model where the temperatures are voltages, the power dissipators are current sources, and the thermal impedances are resistances. Refer to the summary design equations and Figure 1 for a description of terms.



$I_o = V_o/R_{eq}$ total output current

with $R_{eq} = R_L \parallel \left[\frac{R_f A_L}{A_L - 1}\right]$ total load

$I_t = \frac{1}{2}(I_o + \sqrt{I_o^2 + (.06)^2}$ total internal output stage current

$P_t = I_t \cdot (V_{cc} - V_o - .7 - 15.3\Omega \cdot I_t)$ output stage power

$P_q = .2 \cdot I_t \cdot (V_{cc} - 1.4 - 17.3\Omega \cdot I_t)$
power in hottest internal junction prior to output stage

$P_{circuit} = 1.3 \cdot V_{cc} \cdot (2 \cdot I_t - I_o + 19.2mA) - P_t - P_q$
power in remainder of circuit [note $V_{cc} = |-V_{cc}|$]

Note that the P_t and P_q equations are written for positive V_o. Absolute values of $-V_{cc}$, V_o, and I_o should be used for a negative going V_o since we are only interested in delta V's. For bipolar swings, the two powers for each output polarity are developed as shown above then ratioed by the duty cycle. Having the total internal power, as well as its component parts, the maximum junction temperature may be computed as follows.

$T_c = T_A + (P_q + P_T + P_{circuit}) \cdot \emptyset_{CA}$ Case Temperature

$\emptyset_{CA} = 35°C/W$ for the CLC560 with no heatsink in still air

$T_j(t) = T_c + P_t \cdot 20°C/W$
output transistor junction temperature

$T_j(q) = T_c + P_q \cdot 200°C/W$
hottest internal junction temperature

The Limiting Factor for Output Power is Maximum Junction Temperature

Reducing θ_{ca} through either heatsinking and/or airflow can greatly reduce the junction temperatures. One effective means of heatsinking the CLC560 is to use a thermally conductive pad under the part from the package bottom to a top surface ground plane on the component side. Tests have shown a θ_{ca} of 24°C in still air using a "Sil Pad" available from Bergquist (800-347-4572) as Comlinear part #550006.

As an example of calculating the maximum internal junction temperatures, consider the circuit of Figure 1 driving ±2.5V, 50% duty cycle, square wave into a 50Ω load.

$R_{eq} = 50\Omega \parallel \left[\frac{410\Omega \cdot 5}{5-1}\right] = 45.6\Omega$

$I_o = 2.5V/(45.6\Omega) = 54.9mA$

$I_T = \frac{1}{2}(54.9mA + \sqrt{(54.9mA)^2 + (.06)^2}) = 68.1mA$

$P_T = 68.1mA[15 - 2.5 - .7 - 15.3\Omega \cdot 68.1mA] = 733mW$
total power in both sides of the output stage

$P_q = .2 \cdot 68.1mA[15 - 1.4 - 17.3\Omega \cdot 68.1mA] = 169mW$
total power in both sides of hottest junctions prior to output stage

$P_{circuit} = 1.3 \cdot (15) \cdot [2 \cdot 68.1mA - 54.9mA + 19.2mA] - 733mW - 169mW = 1.058W$
power in the remainder of circuit

With these powers and $T_A = 25°C$ and $\emptyset_{ca} = 35°C/W$

$T_c = 25°C + (.733 + .169 + 1.058) \cdot 35 = 94°C$
case temperature

From this, the hottest internal junctions may be found as

$T_j(t) = 94°C + \frac{1}{2}(.733) \cdot 20 = 101°C$ output stage

$T_j(q) = 94°C + \frac{1}{2}(.169) \cdot 200 = 111°C$
hottest internal junction

Note that ½ of the total P_T and P_q powers were used here since the 50% duty cycle output splits the power evenly between the two halves of the circuit whereas the total powers were used to get case temperature.

Even with the output current internally limited to 250mA, the CLC560's short circuiting capability is principally a thermal issue. Generally, the CLC560 can survive short duration shorts to ground without any special effort. For protection against shorts to the ±15 volt supply voltages, it is very useful to reduce some of the voltage across the output stage transistors by using some external output resistance, R_x, as shown in Figure 9. Application Note OA-10 discusses this in detail.

Evaluation Board

An evaluation board (part number 730019) for the CLC560 is available.

Comlinear Corporation

Wideband, Low Distortion DriveR-amps

CLC561

APPLICATIONS:

- output amplification
- arbitrary waveform generation
- ATE systems
- cable/line driving
- function generators
- SAW drivers
- flash A/D driving and testing

FEATURES:

- 150MHz bandwidth at +24dBm output
- low distortion (2nd/3rd: -59/-62dBc @ 20MHz and 10dBm)
- output short circuit protection
- user-definable output impedance, gain, and compensation
- internal current limiting

DESCRIPTION:

The CLC561 is a wideband dc coupled, amplifier that combines high output drive and low distortion. At an output of +24dBm ($10V_{pp}$ into 50Ω), the –3dB bandwidth is 150MHz. As illustrated in the table below, distortion performance remains excellent even when amplifying high-frequency signals to high output power levels.

Typical Distortion Performance

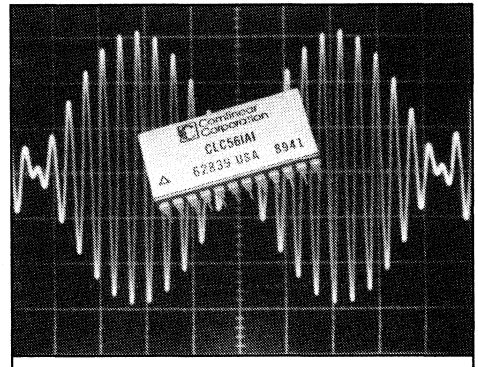
Output Power	20MHz 2nd	20MHz 3rd	50MHz 2nd	50MHz 3rd	100MHz 2nd	100MHz 3rd
10dBm	–59	–62	–52	–60	–35	–49
18dBm	–52	–48	–45	–46	–30	–36
24dBm	–50	–41	–36	–32	–40	–30

With the output current internally limited to 250mA, the CLC561 is fully protected against shorts to ground and can, with the addition of a series limiting resistor at the output, withstand shorts to the ±15V supplies.

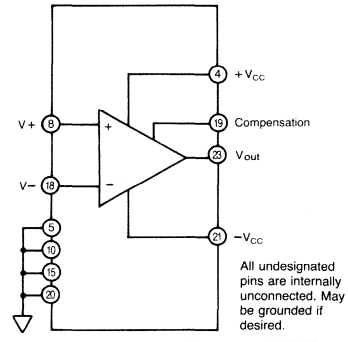
The CLC561 has been designed for maximum flexibility in a wide variety of demanding applications. The two resistors comprising the feedback network set both the gain and the output impedance, without requiring the series backmatch resistor needed by most op amps. This allows driving into a matched load without dropping half the voltage swing through a series matching resistor. External compensation allows user adjustment of the frequency response. The CLC561 is specified for both maximally flat frequency response and 0% pulse overshoot compensations.

The combination of wide bandwidth, high output power, and low distortion, coupled with gain, output impedance and frequency response flexibility, makes the CLC561 ideal for waveform generator applications. Excellent stability driving capacitive loads yields superior performance driving ADC's, long transmission lines, and SAW devices. A companion part, the CLC560, offers superior pulse fidelity for high accuracy dc coupled applications.

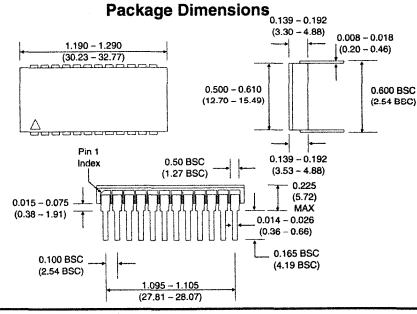
The CLC561 is constructed using thin film resistor/bipolar transistor technology. The CLC561AI is specified over a temperature range of –25°C to +85°C, while the CLC561A8C is specified over a range of –55°C to +125°C and is fully compliant with MIL-STD-883, Level B. Both devices are packaged in 24-pin, 600 mil wide, ceramic DIPs. Contact Comlinear for DESC SMD number.



Pinout



Package Dimensions



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Electrical Characteristics ($A_V = +10$, $V_{CC} = \pm 15V$, $R_f = 410\Omega$, $R_g = 40\Omega$, $R_O = 50\Omega$, $R_L = 50\Omega$)

NOTES TO THE ELECTRICAL SPECIFICATIONS

The electrical characteristics shown here apply to the specific test conditions shown above (see also Figure 1 in description of operation). The CLC561 provides an equivalent, non-zero, output impedance determined by the external resistors. The signal gain to the load is therefore load dependent. **The signal gain shown above ($A_V = +10$) is the no load gain.** The actual gain to the matching 50 ohm load used in these specifications is half of this (+5).

The CLC561 requires an external compensation capacitor. Unless otherwise noted, this has been set to 10.5pF for the frequency domain specifications (yielding a maximally flat frequency response) and 12.5pF for the time domain specifications (yielding a 0% small signal pulse overshoot response).

Parameters preceded by an * are the final electrical test parameters and are 100% tested at 25°C on all versions. The A8C (military) grade part is also 100% tested at -55°C and 125°C case temperature.

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Case Temperature	CLC561A8	+25°C	−55°C	+25°C	+125°C		
Case Temperature	CLC561AI	+25°C	−25°C	+25°C	+ 85°C		
FREQUENCY DOMAIN (Maximally Flat Compensation)							
-3dB bandwidth							
*maximally flat compensation	$V_{OUT}<2V_{pp}$ (+10dBm)	215	>175	>185	>175	MHz	SSBW
0% overshoot compensation	$V_{OUT}<2V_{pp}$ (+10dBm)	210	>170	>180	>170	MHz	
large signal bandwidth	$V_{OUT}<10V_{pp}$ (+24dBm)	150	>145	>135	>120	MHz	FPBW
(see Frequency Response vs. Output Power plot)							
gain flatness	$V_{OUT}<2V_{pp}$ (+10dBm)						
* peaking	0.1 - 50MHz	0	<0.50	<0.40	<0.50	dB	GFPL
* peaking	>50MHz	0	<1.75	<0.75	<1.00	dB	GFPH
* roll off	at 100MHz	0.1	<1.00	<0.75	<1.00	dB	GFR
group delay	to 100MHz	2.9	—	—	—	ns	GD
linear phase deviation	to 100MHz	0.6	<1.7	<1.2	<1.7	°	LPD
return loss (see discussion of R_X)	to 100MHz	−15	<−11	<−11	<−11	dB	RL
DISTORTION (Maximally Flat Compensation)							
2nd harmonic distortion							
*24dBm ($10V_{pp}$):	20MHz	−50	<−38	<−40	<−38	dBc	HD2HL
*	50MHz	−36	<−29	<−29	<−22	dBc	HD2HM
	100MHz	−40	<−25	<−25	<−25	dBc	HD2HH
*18dBm ($5V_{pp}$):	20MHz	−52	<−42	<−44	<−42	dBc	HD2ML
*	50MHz	−45	<−30	<−35	<−30	dBc	HD2MM
*	100MHz	−30	<−22	<−25	<−25	dBc	HD2MH
*10dBm ($2V_{pp}$):	20MHz	−59	<−48	<−52	<−48	dBc	HD2LL
*	50MHz	−52	<−36	<−40	<−40	dBc	HD2LM
*	100MHz	−35	<−27	<−28	<−28	dBc	HD2LH
3rd harmonic distortion							
*24dBm ($10V_{pp}$):	20MHz	−41	<−34	<−34	<−30	dBc	HD3HL
*	50MHz	−32	<−26	<−26	<−21	dBc	HD3HM
	100MHz	−30	<−24	<−24	<−24	dBc	HD3HH
*18dBm ($5V_{pp}$):	20MHz	−48	<−40	<−44	<−44	dBc	HD3ML
*	50MHz	−46	<−37	<−37	<−35	dBc	HD3MM
	100MHz	−36	<−30	<−30	<−30	dBc	HD3MH
*10dBm ($2V_{pp}$):	20MHz	−62	<−54	<−57	<−57	dBc	HD3LL
*	50MHz	−60	<−49	<−52	<−49	dBc	HD3LM
	100MHz	−49	<−45	<−45	<−45	dBc	HD3LH
2-tone 3rd order intermod intercept[1]	20MHz	38	>36	>36	>36	dBm	IM3L
	50MHz	35	>32	>32	>32	dBm	IM3M
	100MHz	29	>27	>27	>23	dBm	IM3H

Electrical Characteristics (A_V = +10, V_{CC} = ±15V, R_f = 410Ω, R_g = 40Ω, R_O = 50Ω, R_L = 50Ω)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Case Temperature	CLC561A8	+25°C	−55°C	+25°C	+125°C		
Case Temperature	CLC561AI	+25°C	−25°C	+25°C	+ 85°C		
TIME DOMAIN (0% Overshoot Compensation)							
rise and fall time							
2V step		1.5	<2.0	<1.9	<2.0	ns	TRS
10V step		2.4	<2.8	<2.8	<3.4	ns	TRL
settling time to 0.5% (time<1μs)	5V step	7	<12	<12	<15	ns	TS
long term thermal tail (time>1μs)	5V step	1.5	<2.0	<2.0	<2.0	%	SE
slew rate	$10V_{pp}$, 175MHz	3300	>3000	>2900	>2500	V/μs	SR
overshoot	2V step						
maximally flat compensation		5	<13	<10	<13	%	OSMF
0% overshoot compensation		0	<5	<3	<5	%	OSZO
EQUIVALENT INPUT NOISE							
voltage	>100KHz	2.1	<2.5	<2.5	<2.5	nV/√Hz	VN
inverting current	>100KHz	34	<40	<40	<45	pA/√Hz	ICN
non-inverting current	>100KHz	2.8	<4.5	<4.5	<5.0	pA/√Hz	NCN
noise floor	>100KHz	−159	<−157	<−157	<−157	dBm/(1Hz)	SNF
integrated noise	1kHz to 200MHz	35	<45	<45	<45	μV	INV
noise figure	>100KHz	15	<17	<17	<17	dB	NF
STATIC, DC							
*input offset voltage		2.0	<14.0	<5.0	<15.0	mV	VIO
average temperature coefficient		35	<100	—	<100	μV/°C	DVIO
*non-inverting bias current		5.0	<35	<20	<20	μA	IBN
average temperature coefficient		20	<175	—	<100	nA/°C	DIBN
*inverting bias current		10.0	<50	<30	<50	μA	IBI
average temperature coefficient		100	<200	—	<200	nA/°C	DIBI
*power supply rejection ratio (DC)		57	>54	>54	>52	dB	PSRR
*supply current	no load	50	<60	<60	<65	mA	ICC
MISCELLANEOUS							
open loop current gain	(± 2% tolerance)	10.0	—	—	—	mA/mA	G
average temperature coefficient		+0.02	<+.03	—	<+.02	%/°C	DG
inverting input resistance	(±5% tolerance)	14.0	—	—	—	Ω	RIN
average temperature coefficient		+.02	<+.025	—	<+.025	Ω/°C	DRIN
non-inverting input resistance		700	>200	>400	>400	KΩ	RNI
non-inverting input capacitance	to 100MHz	2.7	<3.5	<3.5	<3.5	pF	CNI
output voltage range @ 150mA load current		±10.5	—	>±10.0	—	V	VO
output current limit		210	<250	<250	<250	mA	OCL

Absolute Maximum Ratings

V_{cc} (reversed supplies will destroy part)	±20V
differential input voltage	±3V
common mode input voltage	$\pm V_{cc}$
junction temp. (see thermal model)	+175°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	±300°C
output current (internally limited)	±250mA

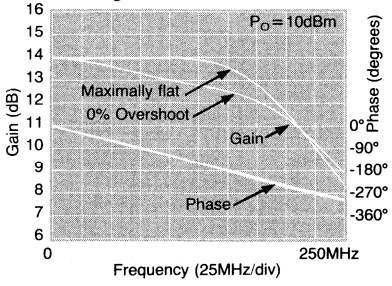
Recommended Operating Conditions

$\pm V_{CC}$	±10 to ±15
I_{out}	≤±200mA
common mode input voltage	<±(|V_{CC}| − 6)V
output impedance	25Ω to 200Ω
gain range (no-load voltage gain)	+5 to +80
case temp. AI	−25°C to +85°C
A8	−55°C to +125°C

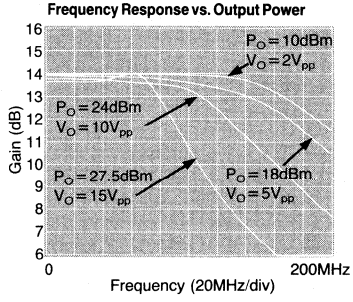
NOTES:
1. Test tones are set ±100kHz of indicated frequency.

Typical Performance Characteristics (T_A = 25°C, Circuit of Figure 1 unless otherwise specified)

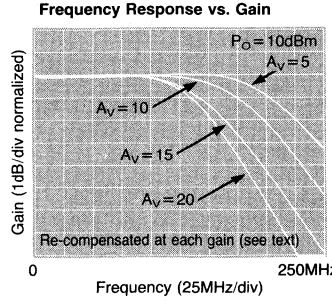
Small Signal Gain and Phase



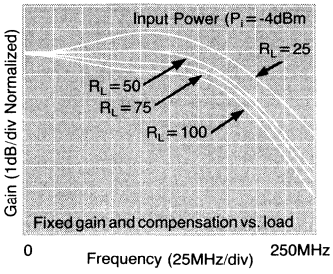
Frequency Response vs. Output Power



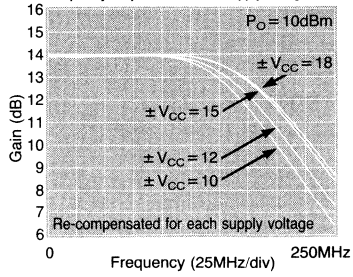
Frequency Response vs. Gain



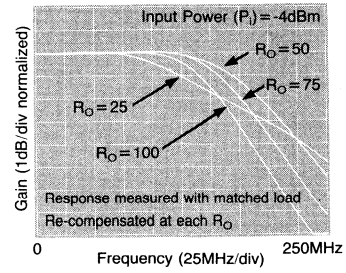
Frequency Response vs. Load Impedance (R_L)



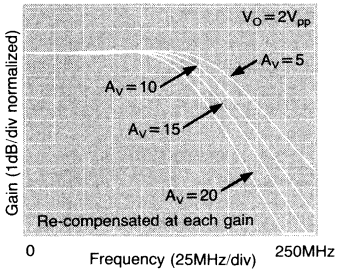
Frequency Response vs. Power Supply Voltages



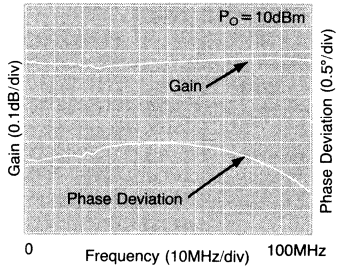
Frequency Response vs. Output Impedance (R_O)



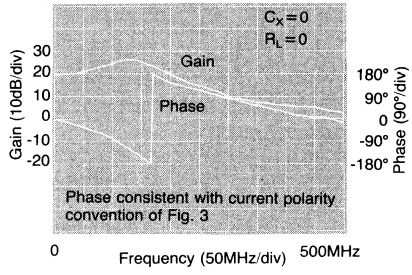
Frequency Response vs. Gain with $R_O = R_L = 75\Omega$



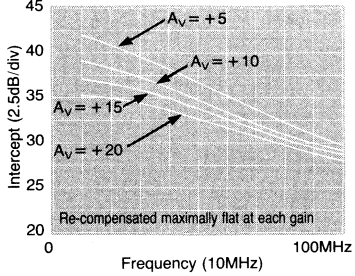
Gain Flatness and Deviation from Linear Phase



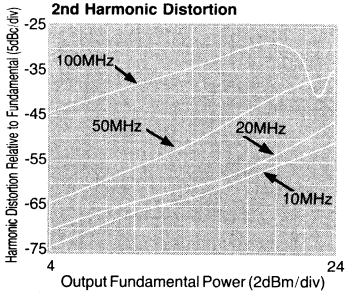
Internal Current Gain and Phase



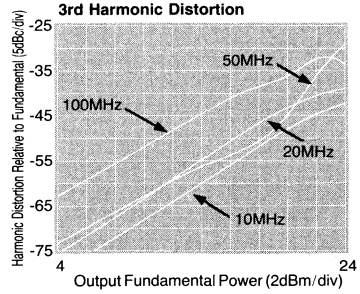
Two Tone, 3rd-Order Intermodulation Intercept



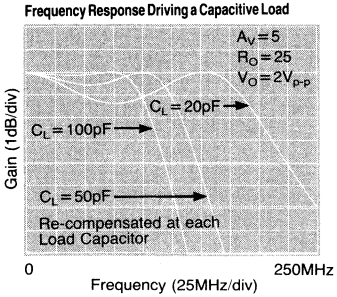
2nd Harmonic Distortion



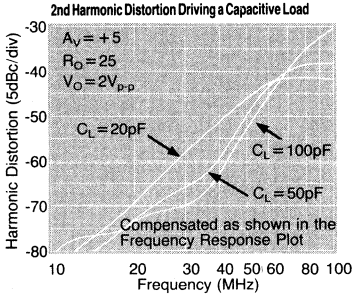
3rd Harmonic Distortion



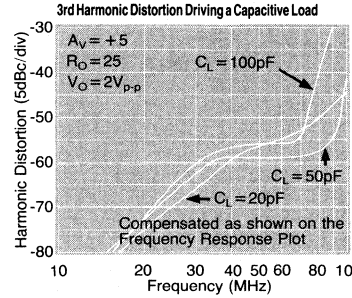
Frequency Response Driving a Capacitive Load



2nd Harmonic Distortion Driving a Capacitive Load

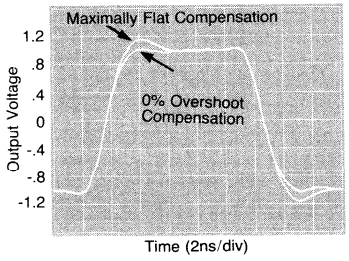


3rd Harmonic Distortion Driving a Capacitive Load

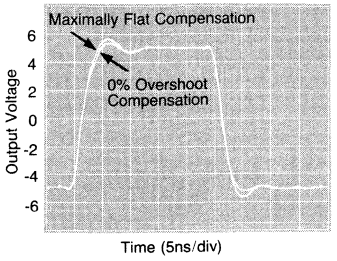


Typical Performance Characteristics (T_A = 25°C, Circuit of Figure 1 unless otherwise specified)

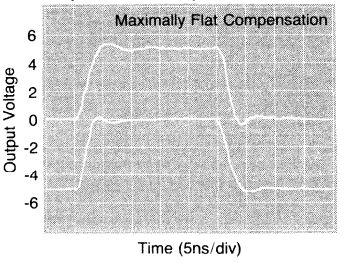
Small Signal Pulse Response



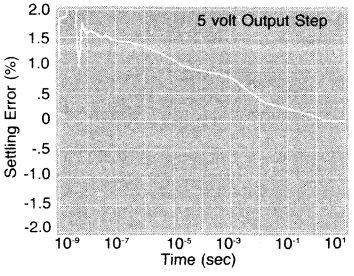
Large Signal Pulse Response



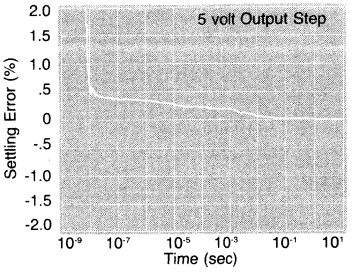
Uni-polar Pulse Response



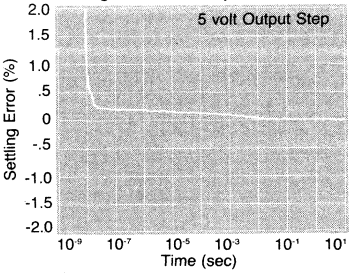
Settling Time into 50Ω Load



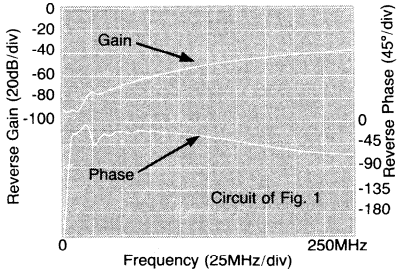
Settling Time into 500Ω Load



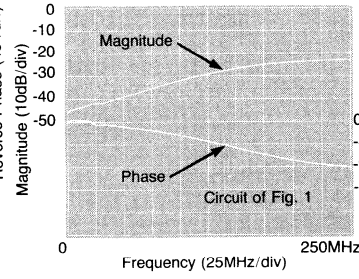
Settling Time into a 50pF Load



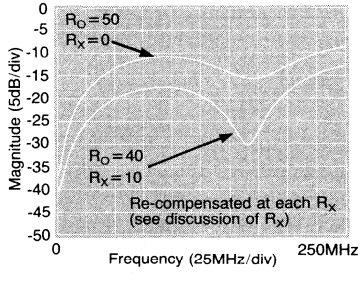
Reverse Transmission Gain and Phase (S_{12})



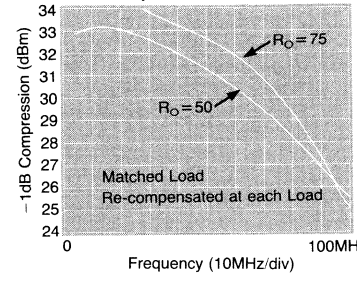
Input Return Loss (S_{11})



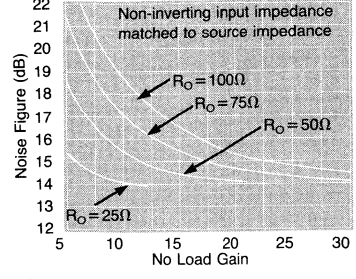
Output Return Loss (S_{22})



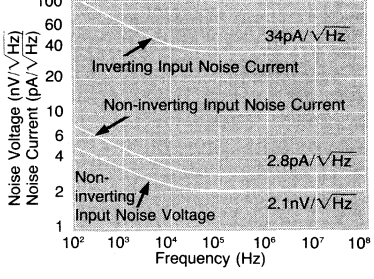
–1dB Compression Point



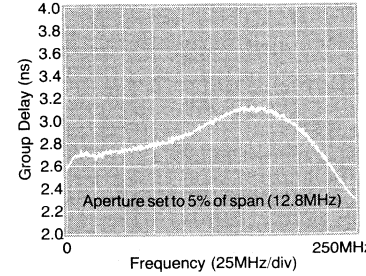
Noise Figure



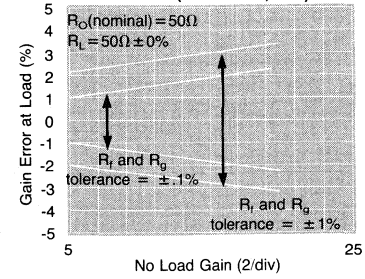
Equivalent Input Spot Noise Terms



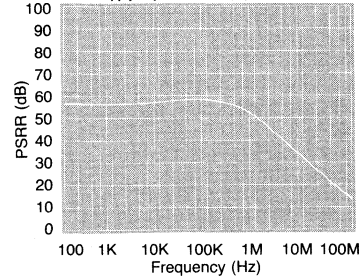
Group Delay



Gain Error Band (Worst Case, D.C.)



Power Supply Rejection Ratio (Input Referred)



SUMMARY DESIGN EQUATIONS AND DEFINITIONS

$R_f = (G + 1) R_o - A_V R_i$ — R_f – Feedback resistor from output to inverting input

$$R_g = \frac{R_f - R_o}{A_v - 1}$$ — R_g – Gain setting resistor from inverting input to ground

$$C_x = \frac{1}{\frac{R_o}{300\left(1 - \frac{2}{R_g}\right)} - .08}$$ C_x – External compensation capacitor from output to pin 19 (in pF)

Where:

R_o – Desired equivalent output impedance
A_v – Non-inverting input to output voltage gain with no load
G – Internal current gain from inverting input to output = 10 ± 1%
R_i – Internal inverting input impedance = 14Ω ± 5%

and

R_s – Non-inverting input termination resistor
R_L – Load Resistor
A_L – Voltage gain from non-inverting input to load resistor

CLC561 Description of Operation

Looking at the circuit of Figure 1 (the topology and resistor values used in setting the data sheet specifications), the CLC561 appears to bear a strong external resemblance to a classical op amp. As shown in the simplified block diagram of Figure 2, however, it differs in several key areas. Principally, the error signal is a current into the inverting input (current feedback) and the forward gain from this current to the output is relatively low, but very well controlled, current gain. The CLC561 has been intentionally designed to have a low internal gain and a current mode output in order that an equivalent output impedance can be achieved without the series matching resistor more commonly required of low output impedance op amps. Many of the benefits of a high loop gain have, however, been retained through a very careful control of the CLC561's internal characteristics.

The feedback and gain setting resistors determine both the output impedance and the gain. R_f predominately sets the output impedance (R_o), while R_g predominately determines the no load gain (A_v). Solving for the required R_f and R_g, given a desired R_o and A_v, yields the design equations shown below. Conversely, given an R_f and R_g, the performance equations show that both R_f and R_g play a part in setting R_o and A_v. Independent R_o and A_v adjustment would be possible if the inverting input impedance (R_i) were 0 but, with $R_i = 14\Omega$ as shown in the specification listing, independent gain and output impedance setting is not directly possible.

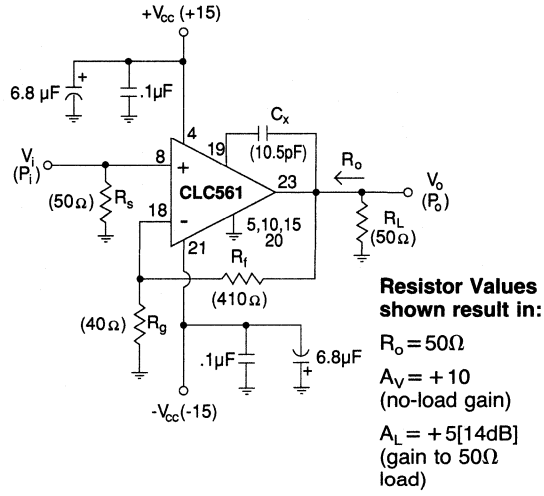


Figure 1: Test Circuit

Design Equations

$$R_f = (G+1) R_o - A_V R_i$$

$$R_g = \frac{R_f - R_o}{A_v - 1}$$

Where:

G≡forward current gain (=10)
R_i≡inverting node input resistance (=14Ω)
R_o≡desired output impedance
A_v≡desired non-inverting voltage gain with no load

Performance Equations

$$R_o = \frac{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}{G + 1 + \frac{R_i}{R_g}}$$

$$A_v = 1 + \frac{R_f}{R_g}\left[\frac{G - \frac{R_i}{R_f}}{G + 1 + \frac{R_i}{R_g}}\right]$$

Simplified Circuit Description

Looking at the CLC561's simplified schematic in Figure 2, the amplifier's operation may be described. Going from the non-inverting input at pin 8 to the inverting input at pin 18, transistors Q1 - Q4 act as an open loop unity gain buffer forcing the inverting node voltage to follow the non-inverting voltage input.

Transistors Q3 and Q4 also act as a low impedance (14Ω looking into pin 18) path for the feedback error current. This current, (i_{err}), flows through those transistors into a very well defined current mirror having a gain of 10 from this error current to the output. The current mirror outputs act as the amplifier output.

The input stage bias currents are supply voltage independent. Since these set the bias level for the whole part, relatively constant performance over supply voltage is achieved. A current sense in the error current leg of the 10X current mirror feeds back to the bias current setup providing a current shutdown feature when the output current approaches 250mA.

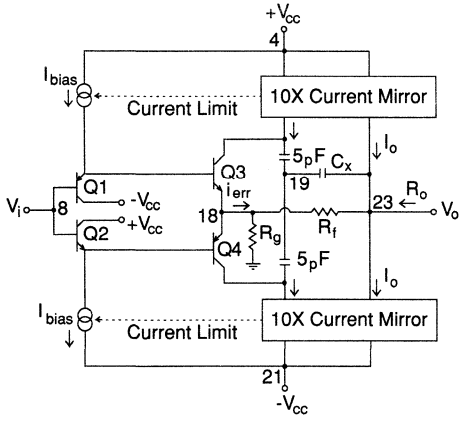
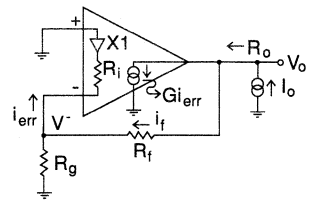


Figure 2: Simplified Circuit Diagram

Developing the Performance Equations

The CLC561 is intended to provide both a controllable voltage gain from input to output as well as a controllable output impedance. It is best to treat these two operations separately with no load in place. Then, with the no-load gain and output impedance determined, the gain to the load will simply be the no-load gain attenuated by the voltage divider formed by the load and the equivalent output impedance.

Figure 3 steps through the output impedance development using an equivalent model of Figure 2. Offering an equivalent, non-zero, output impedance into a matched load allows the CLC561 to operate at lower internal voltage swings for a given desired swing at the load. This allows higher voltage swings to be delivered at the load for a given power supply voltage at lower distortion levels than an equivalent op amp needing to generate twice the voltage swing actually desired at the matched load. This improved distortion is specified and tested over a wide range as shown in the specification listing.



Get both V_o and I_o into terms of just the error current, i_{err}, using

$V- = i_{err} R_i$ and

$$i_f = i_{err} + \frac{V-}{R_g} = i_{err}\left(1 + \frac{R_i}{R_g}\right)$$

$$V_o = V- + i_f R_f = i_{err}\left[R_i + R_f\left(1 + \frac{R_i}{R_g}\right)\right]$$

$$V_o = i_{err}\left[R_f + R_i\left(1 + \frac{R_f}{R_g}\right)\right]$$

and

$$I_o = Gi_{err} + i_f = i_{err}\left[G + 1 + \frac{R_i}{R_g}\right]$$

then

$$R_o \equiv \frac{V_o}{I_o} = \frac{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}{G + 1 + \frac{R_i}{R_g}}$$

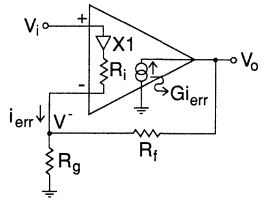
note that $R_o\Big|_{R_i=0} = \frac{R_f}{G+1}$

Figure 3: Output Impedance Derivation

Note that the R_o expression simplifies considerably if $R_i = 0$. Also note that if the forward current gain were to go to infinity, the output impedance would go to 0. This would be the normal op amp topology with a very high internal gain. **The CLC561 achieves a non-zero R_o by setting the internal forward gain to be a low, well controlled, value.**

Developing the No-Load Gain Expression

Taking the output impedance expression as one constraint setting the external resistor values, we now need to develop the no-load voltage gain expression from the non-inverting input to the output as the other constraint. Figure 4 shows the derivation of the no load gain.



No load gain

$$A_v \equiv \frac{V_o}{V_i}$$

Recognize that [taking V_i positive]

$$V_o = V^- + Gi_{err} R_f$$

Solving for V^- from two directions

$$V^- = V_i - i_{err} R_i = (G+1)\, i_{err} R_g$$

solving for i_{err} from this

$$i_{err} = \frac{V_i}{(G+1) R_g + R_i}$$

then

$$V^- = V_i - \frac{V_i R_i}{(G+1) R_g + R_i}$$

and, substituting for V^- and i_{err} in the original V_o expression

$$V_o = V_i - \frac{V_i R_i}{(G+1) R_g + R_i} + \frac{GR_f V_i}{(G+1) R_g + R_i}$$

which simplifies to

$$V_o = V_i \left[1 + \frac{GR_f - R_i}{(G+1) R_g + R_i} \right]$$

pulling an $\frac{R_f}{R_g}$ out of the fraction

$$A_v \equiv \frac{V_o}{V_i} = 1 + \frac{R_f}{R_g} \left[\frac{G - \frac{R_i}{R_f}}{G + 1 + \frac{R_i}{R_g}} \right]$$

note that $A_v \Big|_{R_i = 0} = 1 + \frac{R_f}{R_g} \left(\frac{G}{G+1} \right)$

Figure 4: Voltage Gain Derivation

Note again that if $R_i = 0$ this expression would simplify considerably. Also, if G were very large the voltage gain expression would reduce to the familiar non-inverting op amp gain equation. These two performance equations, shown below, provide a means to derive the design equations for R_f and R_g given a desired no load gain and output impedance. The details of that derivation may be found in Application Note OA-10.

Performance Equations

$$R_o = \frac{R_f + R_i \left(1 + \frac{R_f}{R_g} \right)}{G + 1 + \frac{R_i}{R_g}}$$

$$A_v = 1 + \frac{R_f}{R_g} \left[\frac{G - R_i/R_f}{G + 1 + R_i/R_g} \right]$$

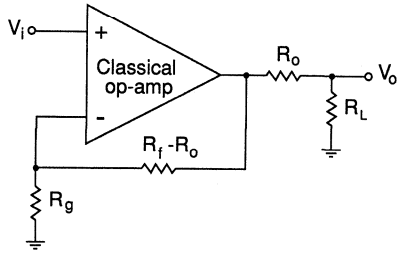
Design Equations

$$R_f = (G+1) R_o - A_v R_i$$

$$R_g = \frac{R_f - R_o}{A_v - 1}$$

Equivalent Model

Given that the physical feedback and gain setting resistors have been determined in accordance with the design equations shown above, an equivalent model may be created for the gain to the load where the amplifier block is taken as a standard op amp. Figure 5 shows this analysis model and the resulting gain equation to the load.



$$\frac{V_o}{V_i} = \left(1 + \frac{R_f - R_o}{R_g} \right) \frac{R_L}{R_L + R_o}$$

Substituting in for R_f and R_g with their design equation yields

$$\frac{V_o}{V_i} = A_v \frac{R_L}{R_L + R_o} = A_L \text{ (gain to load)}$$

Figure 5: Equivalent Model

This model is used to generate the DC error and noise performance equations. As with any equivalent model, the primary intent is to match the external terminal characteristics recognizing that the model distorts the internal currents and voltages. In this case, the model would incorrectly predict the output pin voltage swing for a given swing at the load. But it does provide a simplified means of getting to the external terminal characteristics.

External Compensation Capacitor (C_x)

As shown in the test circuit of Figure 1, the CLC561 requires an external compensation capacitor from the output to pin 19. The recommended values described here assume that a maximally flat frequency response into a matched load is desired. The required C_x varies widely with the desired value of output impedance and to a lesser degree on the desired gain. Note from Figure 2, the simplified internal schematic, that the actual total compensation (C_t) is the series combination of C_x and the internal 10pF from pin 19 to the compensation nodes. The total compensation (C_t) is developed in two steps as shown below.

$$C_1 = \frac{300}{R_o} \left(1 - \frac{2.0}{R_g} \right) \text{ pF intermediate equation}$$

$$C_t = \frac{C_1}{1 + (.02)\, C_1} \text{ pF total compensation}$$

With this total value derived, the required external C_x is developed by backing out the effect of the internal 10pF. This, and an expression for the external C_x without the intermediate steps are shown below.

$$C_x = \frac{10\ C_t}{10 - C_t}$$

or

$$C_x = \frac{1}{\frac{R_o}{300\left(1-\frac{2}{R_g}\right)} - .08}\ pF$$

The plot of Figure 6 shows the required C_x vs. gain for several desired output impedances using the equations shown above. Note that for lower R_o's, C_x can get very large. But, since the total compensation is actually the series combination of C_x and 10pF, going to very high C_x's is increasingly ineffective as the total compensation is only slightly changed. This, in part, sets the lower limits on allowable R_o.

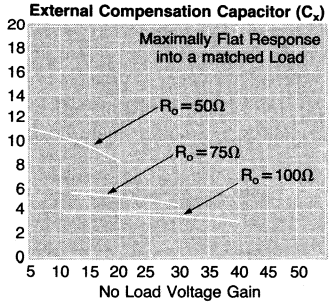


Figure 6: External Compensation Capacitance (C_x)

A 0% small signal overshoot response can be achieved by increasing C_x slightly from the maximally flat value. Note that this applies only for small signals due to slew rate effects coming into play for large, fast edge rates.

Beyond the nominal compensation values developed thus far, this external C_x provides a very flexible means for tailoring the frequency response under a wide variety of gain and loading conditions. It is oftentimes useful to use a small adjustable cap in development to determine a C_x suitable to the application, then fixing that value for production. An excellent 5pF to 20pF trimmer cap for this is a Sprague-Goodman part #GKX20000.

When the CLC561 is used to drive a capacitive load, such as an ADC or SAW device, the load will act to compensate the response along with C_x. Generally, considerably lower C_x values are required than the earlier development would indicate. This is advantageous in that a low R_o would be desired to drive a capacitive load which, without the compensating effect of load itself, would otherwise require very large C_x values.

Gain and Output Impedance Range

Figure 7 shows a plot of the recommended gain and output impedances for the CLC561. Operation outside of this region is certainly possible with some degradation in performance. Several factors contribute to set this range. At very low output impedances, the required value of feedback resistor becomes so low as to excessively load the output causing a rapid degradation in distortion. The maximum R_o was set somewhat arbitrarily at 200Ω. This allows the CLC561 to drive into a 2:1 step down transformer matching to a 50Ω load. (This offers some advantages from a distortion standpoint. See Application Note OA-10 for details.)

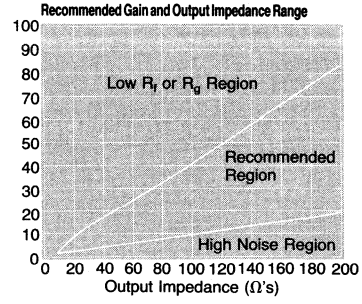


Figure 7: Recommended Gain and Output Impedance Range

For a given R_o, the minimum gain shown in Figure 7 has been set to keep the equivalent input noise voltage less than $4nV/\sqrt{Hz}$. Generally, the equivalent input noise voltage decreases with higher signal gains. The high gain limit has been set by targeting a minimum R_g of 10Ω or a minimum R_f of 100Ω.

Amplifier Configurations (Additional discussion in Application Note OA-10)

The CLC561 is intended for a fixed, non-inverting, gain configuration as shown in Figure 1. The CLC560 offers the better pulse fidelity with its improved thermal tail in the pulse response (vs. the CLC561). Due to its low internal forward gain, the inverting node **does not** present a low impedance, or virtual ground, node. Hence, in an inverting configuration, the signal's source impedance will see a finite load whose value depends on the output loading. Inverting mode operation can be best achieved using a wideband, unity gain buffer with low output impedance, such as the CLC110, to isolate the source from this varying load. A DC level can, however, be summed into the inverting node to offset the output either for offset correction or signal conditioning. Application Note OA-10 describes this and a composite amplifier structure that enhances the DC and gain accuracy characteristics of the CLC561.

Accuracy Calculations

Several factors contribute to limit the achievable CLC561 accuracy. These include the DC errors, noise effects, and the impact internal amplifier characteristics have on the signal gain. Both the output DC error and noise model may be developed using the equivalent model of Figure 5. Generally, non-inverting input errors show up at the output with the same gain as the input signal, while the inverting current errors have a gain of simply $(R_f - R_o)$ to the output voltage (neglecting the R_o to R_L attenuation).

Output DC offset:

The DC error terms shown in the specification listing along with the model of Figure 5 may be used to estimate the output DC offset voltage and drift. Each term shown in the specification listing can be of either polarity. While the equations shown below are for output offset voltage, the same equation may be used for the drift with each term replaced by its temperature drift value shown in the specification listing.

Output DC offset

$$V_{os} = \left(I_{bn} \cdot R_s \pm V_{io}\right) \cdot \left(1 + \frac{R_f - R_o}{R_g}\right) \pm I_{bi}\,(R_f - R_o)$$

Where: $I_{bn} \equiv$ non-inverting bias current
$I_{bi} \equiv$ inverting bias current
$V_{io} \equiv$ input offset voltage

An example calculation for the circuit of Figure 1 using typical 25°C DC error terms and $R_s = 25\Omega$ $R_L = 50\Omega$ yields

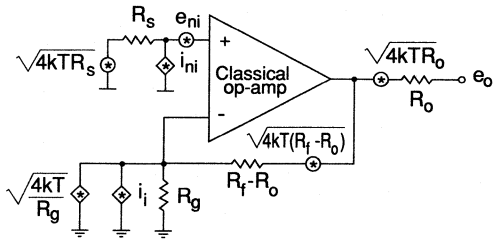
$$V_o\Big|_{DC} = [(5\mu A \cdot 25\Omega \pm 2.0mV)\,10 \pm 10\mu A(360\Omega)]\,\tfrac{1}{2} = \pm 12.4\,mV$$

attenuation between R_o and R_L

Recall that the source impedance, R_s, includes both the terminating and signal source impedance and that the actual DC level to the load includes the voltage divider between R_o and R_L. Also note that for the CLC561, as well as for all current feedback amplifiers, the non-inverting and inverting bias currents do not track each other in either magnitude or polarity. Hence, there is no meaning in an offset current specification, and source impedance matching to cancel bias currents is ineffective.

Noise Analysis:

Although the DC error terms are in fact random, the calculation shown above assumes they are all additive in a worst case sense. The effect of all the various noise sources are combined as a root sum of squared terms to get an overall expression for the spot noise voltage. The circuit of Figure 8 shows the equivalent circuit with all the various noise voltages and currents included along with their gains to the output.



Where:	Gain to e_o
e_{ni} – non-inverting input voltage noise	A_v
i_{ni} – non-inverting input current noise	$A_v R_s$
i_i – inverting input current noise	$R_f - R_o$
$\sqrt{4kTR_s}$ – source resistance voltage noise	A_v
$\sqrt{4kT/R_g}$ – gain setting resistor noise current	$R_f - R_o$
$\sqrt{4kT(R_f - R_o)}$ – feedback resistor voltage noise	1
$\sqrt{4kTR_o}$ – output resistor voltage noise	1

Figure 8

To get an expression for the equivalent output noise voltage, each of these noise voltage and current terms must be taken to the output through their appropriate gains and combined as the root sum of squares.

$$e_o = \sqrt{(e_{ni}^2 + (i_{ni}R_s)^2 + 4kTR_s)\,A_v^2 + i_i^2(R_f - R_o)^2} \cdots \overline{+ 4kT(R_f - R_o)\,A_v + 4kTR_o}$$

Where the $4kT(R_f - R_o)A_v$ term is the combined noise power of R_g and $R_f - R_o$.

It is often more useful to show the noise as an equivalent input spot noise voltage where every term shown above is reflected to the input. This allows a direct measure of the input signal to noise ratio. This is done by dividing every term inside the radical by the signal voltage gain squared. This, and an example calculation for the circuit of Figure 1, are shown below. Note that R_L may be neglected in this calculation.

$$e_n = \sqrt{e_{ni}^2 + (i_{ni}R_s)^2 + 4kTR_s + \frac{i_i^2(R_f - R_o)^2}{A_v^2}} + \cdots \overline{\frac{4kT(R_f - R_o)}{A_v} + \frac{4kTR_o}{A_v^2}}$$

For the circuit of Figure 1, the equivalent input noise voltage may be calculated using the data sheet spot noises and $R_s = 25\Omega$, $R_L = \infty$. Recall that $4kT = 16E{-}21J$. All terms cast as $(nV/\sqrt{Hz})^2$

$$e_n = \sqrt{(2.1)^2 + (.07)^2 + (.632)^2 + (1.22)^2 + (.759)^2 + (.089)^2}$$
$$= 2.62nV/\sqrt{Hz}$$

Gain Accuracy (DC):
A classical op amp's gain accuracy is principally set by the accuracy of the external resistors. The CLC561 also depends on the internal characteristics of the forward current gain and inverting input impedance. The performance equations for A_v and R_o along with the Thevinin model of Figure 5 are the most direct way of assessing the absolute gain accuracy. Note that internal temperature drifts will decrease the absolute gain slightly as the part warms up. Also note that the parameter tolerances affect both the signal gain and output impedance. The gain tolerance to the load must include both of these effects as well as any variation in the load. The impact of each parameter shown in the performance equations on the gain to the load (A_L) is shown below.

Increasing current gain G	Increases A_L
Increasing inverting input R_i	Decreases A_L
Increasing R_f	Increases A_L
Increasing R_g	Decreases A_L

Applications Suggestions

Driving a capacitive load:
The CLC561 is particularly suitable for driving a capacitive load. Unlike a classical op amp (with an inductive output impedance), the CLC561's output impedance, while starting out real at the programmed value, goes somewhat capacitive at higher frequencies. This yields a very stable performance driving a capacitive load. The overall response is limited by the (1/RC) bandwidth set by the CLC561's output impedance and the load capacitance. It is therefore advantageous to set a low R_o with the constraint that extremely low R_f values will degrade the distortion performance. $R_o = 25\Omega$ was selected for the data sheet plots. Note from distortion plots into a capacitive load that the CLC561 achieves better than 60dBc THD (10 bits) driving $2V_{pp}$ into a 50pF load through 30MHz.

Improving the output impedance match vs. frequency – Using R_x:
Using the loop gain to provide a non-zero output impedance provides a very good impedance match at low frequencies. As shown on the Output Return Loss plot, however, this match degrades at higher frequency. Adding a small external resistor in series with the output, R_x, as part of the output impedance (and adjusting the programmed R_o accordingly) provides a much better match over frequency. Figure 9 shows this approach.

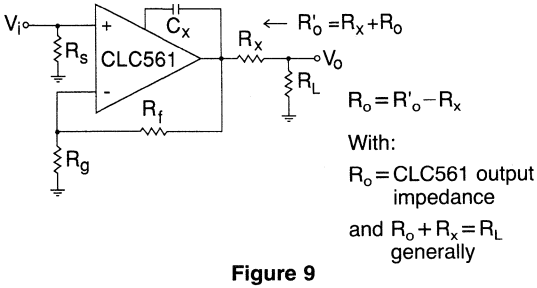


Figure 9

Increasing R_x will decrease the achievable voltage swing at the load. A minimum R_x should be used consistent with the desired output match. As discussed in the thermal analysis discussion, R_x is also very useful in limiting the internal power under an output shorted condition.

Interpreting the Slew Rate:
The slew rate shown in the data sheet applies to the voltage swing at the load for the circuit of Figure 1. Twice this value would be required of a low output impedance amplifier using an external matching resistor to achieve the same slew rate at the load.

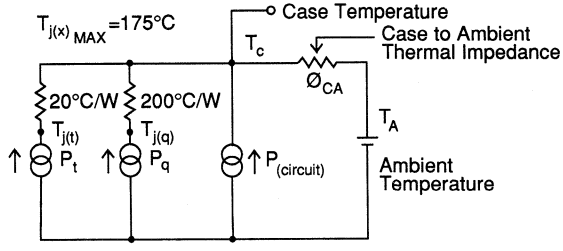
Layout Suggestions:
The fastest fine scale pulse response settling requires careful attention to the power supply de-coupling. Generally, the larger electrolytic capacitor ground connections should be as near the load ground (or cable shield connection) as is reasonable, while the higher frequency ceramic de-coupling caps should be as near the CLC561's supply pins as possible to a low inductance ground plane.

Evaluation Boards and Encased Versions:
An evaluation board (showing a good high frequency layout) for the CLC561 is available. This board may be ordered as part #730019. In addition, encased versions of the CLC561 are also available. These are modular amplifiers similar to Comlinear's other E-series parts.

Thermal Analysis and Protection

A thermal analysis of a chip and wire hybrid is directed at determining the maximum junction temperature of all the internal transistors. From the total internal power dissipation, a case temperature may be developed using the ambient temperature and the case to ambient thermal impedance. Then, each of the dominant power dissipating paths are considered to determine which has the maximum rise above case temperature.

The thermal model and analysis steps are shown below. As is typical, the model is cast as an electrical model where the temperatures are voltages, the power dissipators are current sources, and the thermal impedances are resistances. Refer to the summary design equations and Figure 1 for a description of terms.



$I_o = V_o/R_{eq}$ total output current

with $R_{eq} = R_L \parallel \left[\frac{R_f A_L}{A_L - 1}\right]$ total load

$I_t = \frac{1}{2}(I_o + \sqrt{I_o^2 + (.06)^2}$ total internal output stage current

$P_t = I_t \cdot (V_{cc} - V_o - .7 - 15.3\Omega \cdot I_t)$ output stage power

$P_q = .2 \cdot I_t \cdot (V_{cc} - 1.4 - 17.3\Omega \cdot I_t)$
power in hottest internal junction prior to output stage

$P_{circuit} = 1.3 \cdot V_{cc} \cdot (2 \cdot I_t - I_o + 19.2mA) - P_t - P_q$
power in remainder of circuit [note $V_{cc} = |-V_{cc}|$]

Note that the P_t and P_q equations are written for positive V_o. Absolute values of $-V_{cc}$, V_o, and I_o should be used for a negative going V_o since we are only interested in delta V's. For bipolar swings, the two powers for each output polarity are developed as shown above then ratioed by the duty cycle. Having the total internal power, as well as its component parts, the maximum junction temperature may be computed as follows.

$T_c = T_A + (P_q + P_T + P_{circuit}) \cdot \emptyset_{CA}$ Case Temperature

$\emptyset_{CA} = 35°C/W$ for the CLC561 with no heatsink in still air

$T_j(t) = T_c + P_t \cdot 20°C/W$
output transistor junction temperature

$T_j(q) = T_c + P_q \cdot 200°C/W$
hottest internal junction temperature

The Limiting Factor for Output Power is Maximum Junction Temperature

Reducing θ_{ca} through either heatsinking and/or airflow can greatly reduce the junction temperatures. One effective means of heatsinking the CLC561 is to use a thermally conductive pad under the part from the package bottom to a top surface ground plane on the component side. Tests have shown a θ_{ca} of 24°C/W in still air using a "Sil-Pad" available from Bergquist (800-347-4572) as Comlinear part #550006.

As an example of calculating the maximum internal junction temperatures, consider the circuit of Figure 1 driving ±2.5V, 50% duty cycle, square wave into a 50Ω load.

$R_{eq} = 50\Omega \parallel \left[\frac{410\Omega \cdot 5}{5-1}\right] = 45.6\Omega$

$I_o = 2.5V/(45.6\Omega) = 54.9mA$

$I_T = \frac{1}{2}(54.9mA + \sqrt{(54.9mA)^2 + (.06)^2}) = 68.1mA$

$P_T = 68.1mA[15 - 2.5 - .7 - 15.3\Omega \cdot 68.1mA] = 733mW$
total power in both sides of the output stage

$P_q = .2 \cdot 68.1mA[15 - 1.4 - 17.3\Omega \cdot 68.1mA] = 169mW$
total power in both sides of hottest junctions prior to output stage

$P_{circuit} = 1.3 \cdot (15) \cdot [2 \cdot 68.1mA - 54.9mA + 19.2mA] - 733mW - 169mW = 1.058W$
power in the remainder of circuit

With these powers and $T_A = 25°C$ and $\emptyset_{ca} = 35°C/W$

$T_c = 25°C + (.733 + .169 + 1.058) \cdot 35 = 94°C$
case temperature

From this, the hottest internal junctions may be found as

$T_j(t) = 94°C + \frac{1}{2}(.733) \cdot 20 = 101°C$ output stage

$T_j(q) = 94°C + \frac{1}{2}(.169) \cdot 200 = 111°C$
hottest internal junction

Note that ½ of the total P_T and P_q powers were used here since the 50% duty cycle output splits the power evenly between the two halves of the circuit whereas the total powers were used to get case temperature.

Even with the output current internally limited to 250mA, the CLC561's short circuiting capability is principally a thermal issue. Generally, the CLC561 can survive short duration shorts to ground without any special effort. For protection against shorts to the ±15 volt supply voltages, it is very useful to reduce some of the voltage across the output stage transistors by using some external output resistance, R_x, as shown in Figure 9. Application Note OA-10 discusses this in detail.

Evaluation Board

An evaluation board (part number 730019) for the CLC561 is available.

Variable Gain Amplifiers
Contents

Comlinear Corporation

Amplifier with Voltage Controlled Gain, AGC+*Amp*

CLC520

APPLICATIONS:

- wide-bandwidth AGC systems
- automatic signal-leveling
- video signal processing
- voltage controlled filters
- differential amplifier
- amplitude modulation

DESCRIPTION

The CLC520 is a wideband DC-coupled amplifier with voltage-controlled gain (AGC). The amplifier has a high-impedance differential signal input, a high-bandwidth gain control input and a single-ended voltage output. Signal channel performance is outstanding with 160MHz small signal bandwidth, 0.5 degree linear phase deviation (to 60MHz) and 0.04% signal nonlinearity at $4V_{pp}$ output.

Gain-control is very flexible. Maximum gain may be set over a nominal range of 2 to 100 with one external resistor. In addition, the gain-control input provides more than 40dB of voltage-controlled gain adjustment from the maximum gain setting. For example, a CLC520 may be set for a maximum gain of 2 (or 6dB) for a voltage-controlled gain range from 6dB to less than –34dB. Alternatively, the CLC520 could be set for a maximum gain of 100 (40dB) for a voltage-controlled gain range from 40dB to less than 0dB.

Besides being flexible, the gain-control is easy to use. Gain-control bandwidth is superb, 100MHz, simplifying AGC/ALC loop stabilization. And since the gain is minimum with a zero volt input and maximum with a +2 volt input, driving the control input is simple.

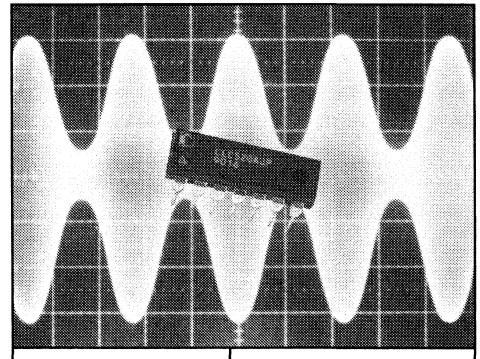
Finally, differential inputs, and a ground-referenced voltage output take the trouble out of designing DC-coupled AGC circuits for display normalizers, etc. The CLC520 is available in several versions:

CLC520AJP	–40°C to +85°C	14-pin plastic DIP
CLC520AJE	–40°C to +85°C	14-pin plastic SOIC
CLC520AID	–40°C to +85°C	14-pin side-brazed DIP
CLC520A8D	–55°C to +125°C	14-pin side-brazed DIP, MIL-STD-883, Level B
CLC520ALC	–55°C to +125°C	dice
CLC520AMC	–55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

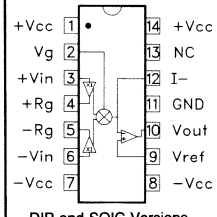
Contact factory for other packages. DESC SMD number 5962-91694.

FEATURES (typical):

- 160MHz, –3dB bandwidth
- 2000 V/μsec slew rate
- 0.04% signal nonlinearity at $4V_{pp}$ output
- –43dB feedthrough at 30MHz
- user adjustable gain range
- differential voltage input and single-ended voltage output

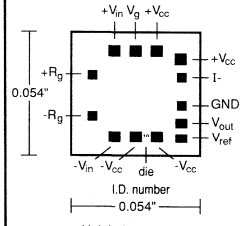


Pinout



DIP and SOIC Versions

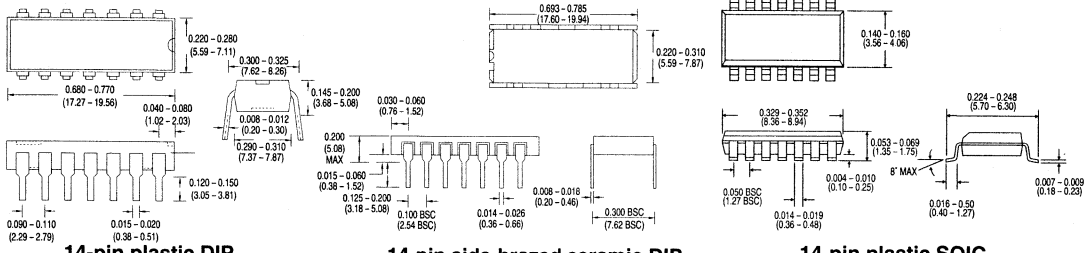
Chip Topography



Height is 0.014 inches.

NOTE: Backside connected to $-V_{cc}$. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



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Electrical Characteristics (V_{cc}=±5V, R_f=100Ω, R_f=1kΩ, R_g=182Ω, A_v=+10, V_g= +2V)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC520A8/AL/AM	+25°C	– 55°C	+25°C	+125°C		
Ambient Temperature	CLC520AJ/AI	+25°C	– 40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
† – 3dB bandwidth	V_{out} <0.5V_{pp}	160	>110	>120	>120	MHz	SSBW
	V_{out} <0.5V_{pp} (AJE only)	140	>90	>100	>100	MHz	SSBW
	V_{out} <4.0V_{pp}	140	>85	>100	>100	MHz	LSBW
– 3dB bandwidth	V_{out} <0.5V_{pp}						
gain control channel	V_{in}=+0.2V, V_g=+1VDC	100	>80	>80	>80	MHz	SBWC
gain flatness	V_{out} <0.5V_{pp}						
√ peaking	0.1MHz to 30MHz	0	<0.4	<0.3	<0.4	dB	GFPL
† peaking	0.1MHz to 20MHz	0	<0.7	<0.5	<0.7	dB	GFPH
√ rolloff	0.1MHz to 30MHz	0.1	<0.4	<0.3	<0.4	dB	GFRL
† rolloff	0.1MHz to 60MHz	0.5	<1.3	<1	<1.3	dB	GFRH
linear phase deviation	0.1MHz to 60MHz	0.5	<1.2	<1	<1.2	°	LPD
†feedthrough	V_g=0V, V_{in}= – 22dBm						
	at 30MHz	– 43	<– 38	<– 38	<– 38	dB	FDTH
	AJ only	– 38	<– 31	<– 31	<– 31	dB	FDTH
rise and fall time	0.5V step	2.5	<3.7	<3	<3	ns	TRS
	4.0V step	3.7	<5	<5	<5	ns	TRL
settling time to ±0.1%	2.0V step	12	<18	<18	<18	ns	TS
overshoot	0.5V step	0	<15	<15	<15	%	OS
slew rate	4V step	2000	>1450	>1450	>1450	V/µsec	SR
†2nd harmonic distortion	2V_{pp}, 20MHz	– 47	<– 40	<– 40	<– 35	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 20MHz	– 60	<– 50	<– 50	<– 45	dBc	HD3
equivalent output noise	(+10 for input noise)[1]						
noise floor	1MHz to 200MHz	– 132	<– 130	<– 130	<– 129	dBm/Hz	SNF
integrated noise	1MHz to 200MHz	800	<1000	<1000	<1100	µV	INV
differential gain[2]	at 3.58MHz	0.15				%	DG
differential phase[2]	at 3.58MHz	0.15				°	DP
STATIC, DC PERFORMANCE							
integral signal nonlinearity	V_{out}=4V_{pp}	0.04	<0.1	<0.1	<0.2	%	SGNL
gain accuracy	R_f=1kΩ, R_g=182Ω						
for nominal max gain = 20dB		±0	<±1.0	<±0.5	<±0.5	dB	GACCU
*output offset voltage		40	<150	<120	<150	mV	VOS
average temperature coefficent		100	<400	—	<300	µV/°C	DVOS
*input bias current		12	<61	<28	<28	µA	IB
average temperature coefficient		100	<415	—	<165	nA/°C	DIB
input offset current		0.5	<4	<2	<2	µA	IOS
average temperature coefficient		5	<40	—	<20	nA/°C	DIOS
†power supply sensitivity	output referred DC	10	<28	<28	<28	MV/V	PSS
common mode rejection ratio	input referred	70	>59	>59	>59	dB	CMRR
*supply current	no load	28	<38	<38	<38	mA	ICC
V_{in} signal input	resistance	200	>50	>100	>100	kΩ	RIN
	capacitance	1	<2	<2	<2	pF	CIN
V_{in} differential voltage range	for R_g=182Ω only	±280	>±250	>±250	>±210	mV	DMIR
V_{in} common mode voltage range		±2.2	>1.4	>±2	>±2	V	CMIR
V_g control input	resistance	750	>535	>600	>600	Ω	RINC
	capacitance	1	<2	<2	<2	pF	CINC
V_g input voltage	for maximum gain	1.6	<2	<2	<2	kΩ	VGHI
	for minimum gain	0.4	>0	>0	>0	V	VGLO
output impedance	at DC	0.1	<0.3	<0.2	<0.2	Ω	RO
output voltage range	no load	±3.5	>±3	>±3.2	>±3.2	V	VO
output current	– 40°C to +85°C	±70	>±35	>±50	>±50	mA	IO
	– 55°C to +125°C	±70	>±30	>±50	>±50	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, however, maximum reliability is obtained if I_{out} does not exceed...	70mA
common mode input voltage	±V_{cc}
V_{in} differential input voltage	10V
V_g input voltage	±V_{cc}
V_{ref} input voltage	±V_{cc}
junction temperature	+175°C
operating temperature range	
AJ/AI	– 40°C to + 85°C
A8/AL/AM	– 55°C to + 125°C
storage temperature range	– 65°C to +150°C
lead solder duration (+300°C)	10 sec

Miscellaneous Ratings

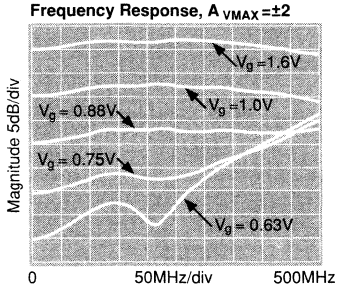
recommended gain range:	± 2 to ±100
recommended V_{REF}	± 150mV

Notes:

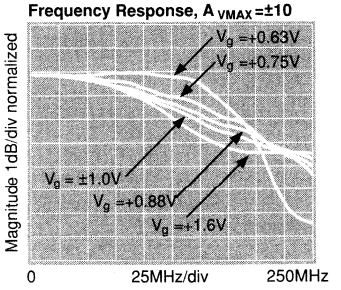
*	AI, AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested at +25°C, – 55°C, +125°C.
†	A8	100% tested at +25°C, sample – 55°C, +125°C.
√	A8	100% tested at +25°C
*	AL/AM	100% wafer probe tested at +25°C to +25°C min/max specifications
note 1:		Measured at A_{vmax} = 10, V_g = +2V
note 2:		Differential gain and phase are measured at: A_v= +20, V_g = +2V, R_L = 150Ω, R_f=2kΩ, R_g = 182Ω, equivalent video signal of 0-100 IRE with 40 IRE_{pp} at 3.58 MHz.

Typical Performance Characteristics (T_A=25°C, V_{cc}=±5V, R_s=100Ω, R_f=1kΩ, R_L=182Ω, A_V=+10, V_o=2V)

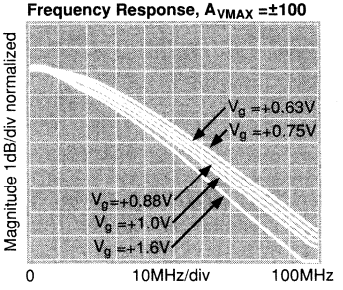
Frequency Response, A_{VMAX}=±2



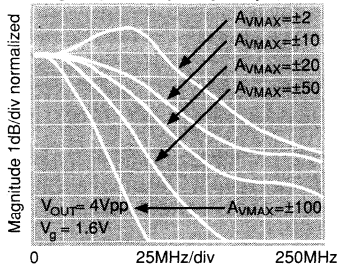
Frequency Response, A_{VMAX}=±10



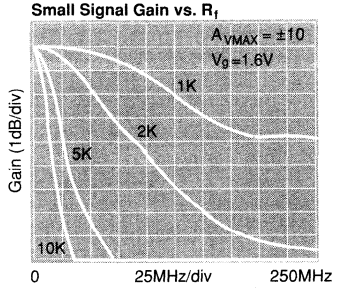
Frequency Response, A_{VMAX}=±100



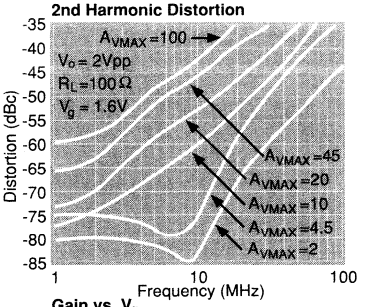
Large Signal Frequency Response



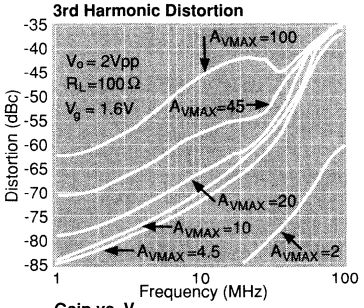
Small Signal Gain vs. R_f



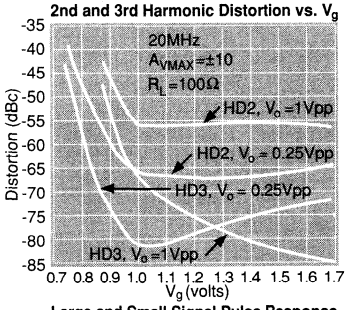
2nd Harmonic Distortion



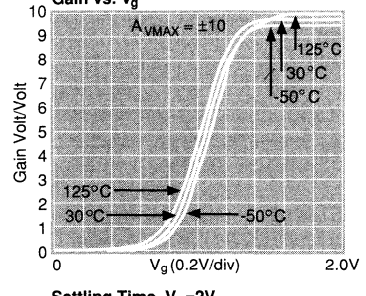
3rd Harmonic Distortion



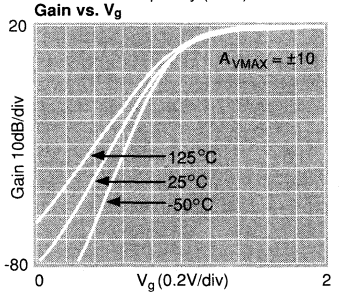
2nd and 3rd Harmonic Distortion vs. V_g



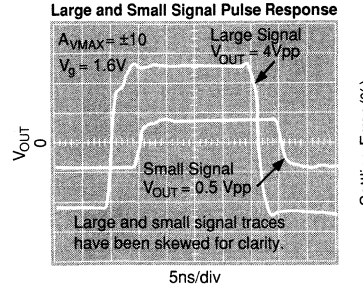
Gain vs. V_g



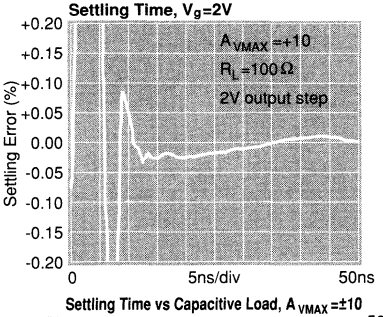
Gain vs. V_g



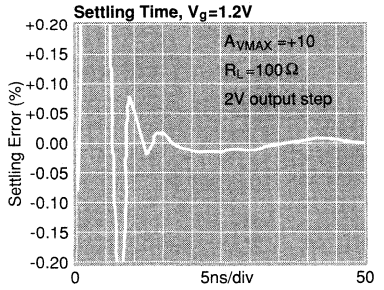
Large and Small Signal Pulse Response



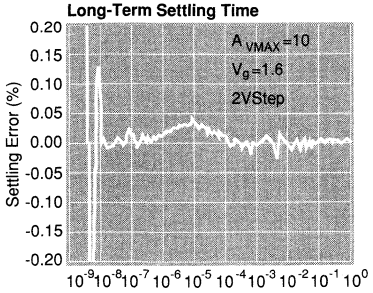
Settling Time, V_g=2V



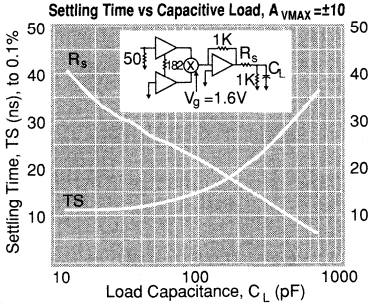
Settling Time, V_g=1.2V



Long-Term Settling Time

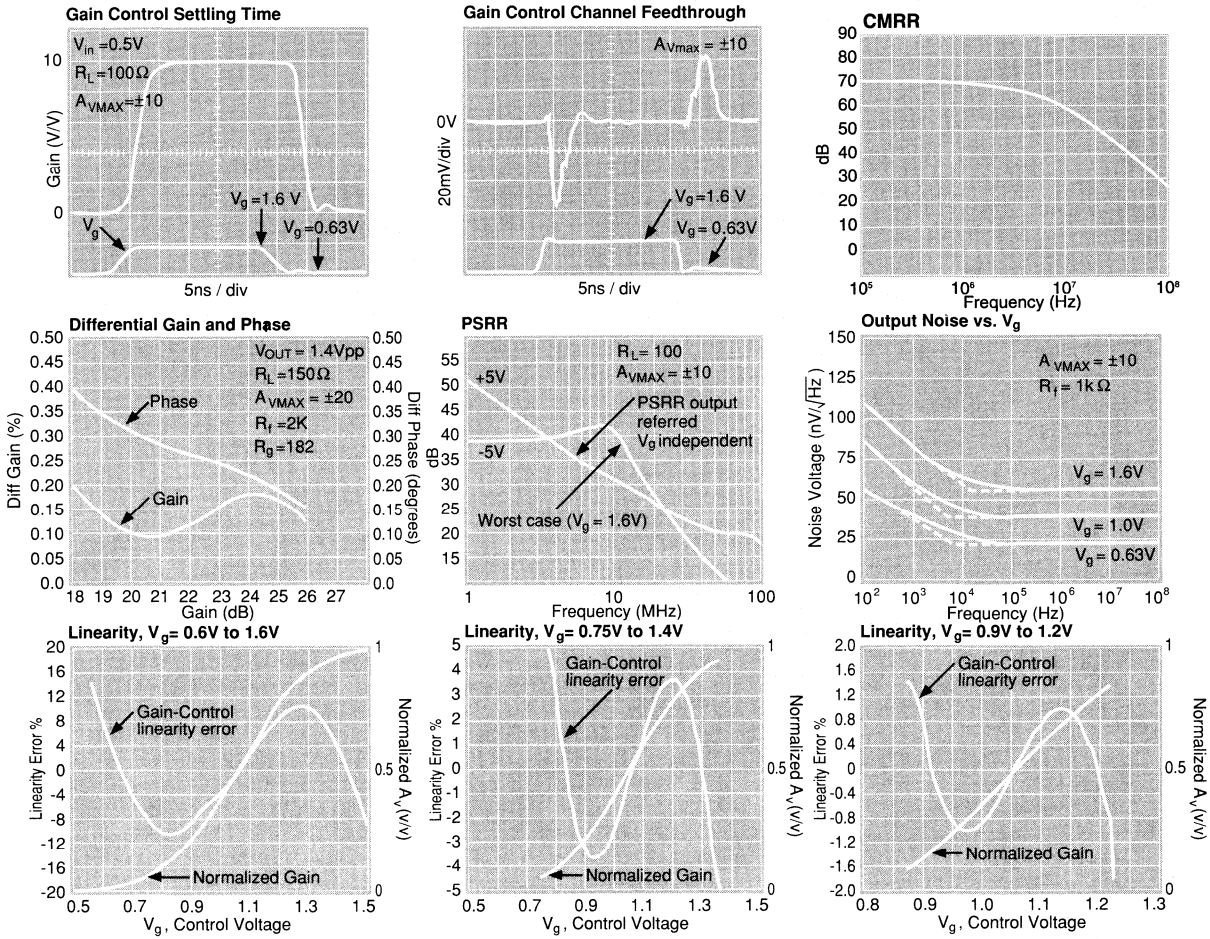


Settling Time vs Capacitive Load, A_{VMAX}=±10



5

Typical Performance Characteristics (T_A=25°C, V_{cc}=±5V, R_L=100Ω, R_f=1kΩ, R_g=182Ω, A_V=+10, V_g=+2V)



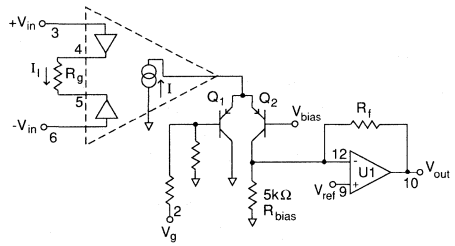


Figure 1: CLC520 Simplified Schematic

Simplified Circuit Description

A simplified schematic for the CLC520 is given in Figure 1. $+V_{in}$ and $-V_{in}$ are buffered with closed-loop voltage followers inducing a signal current in R_g proportional to $(+V_{in}) - (-V_{in})$, the differential input voltage. This current controls a current source which supplies two well-matched transistors, Q1 and Q2.

The current flowing through Q2 is converted to the final output voltage using R_f and output amplifier, U1. By changing the fraction of the signal current I which flows through Q2 the gain is changed. This is done by changing the voltage applied differentially to the bases of Q1 and Q2. For example, with $V_g = 0$, Q1 conducts heavily and Q2 is off. With none of I flowing through R_f, the CLC520's input to output gain is strongly attenuated. With $V_g = 2V$, Q1 is off and all of the signal current flows through Q2 to R_f producing maximum gain. With V_g set to 1.1V, the bases of Q1 and Q2 are set to approximately the same voltage, Q1 and Q2 have the same collector currents – equal to one half of signal current I, thus the gain is approximately one half the maximum gain at $V_g = 1.1V$.

Typical application circuit

Figure 2 illustrates a voltage-controlled gain block offering broadband performance in a 50Ω system environment. The input signal is applied to pin 3 of the CLC520 and terminating resistor R2. Gain-control signals are applied to pin 2. The net gain-control port input impedance is 50Ω, set by the parallel combination of R1 and the 750Ω input impedance of pin 2 of the CLC520.

R_f is set to the standard value, 1kΩ, and R_g sets the maximum voltage gain (with a high Z load connected to the output) to 10V/V. Output impedance is set by R_o to 50Ω so with 50Ω source and load terminations, the gain is approximately 14dB.

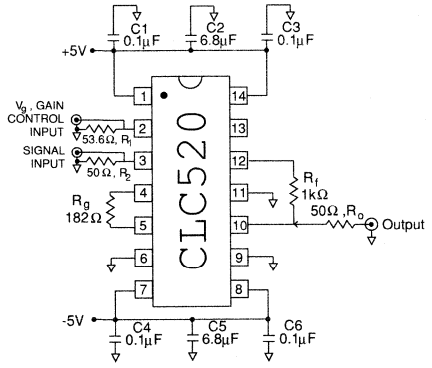


Figure 2: CLC520 Typical Application Circuit

Capacitors C1-C6 provide broadband power-supply bypassing. C2 and C5 should be tantalum capacitors. All other capacitors should be high-quality ceramic capacitors (CK-05 or equivalent).

Adjusting offset

Offset can be broken into two parts: an input-referred and an output-referred term. The input-referred offset shows up as a variation in output voltage as V_g is changed. This can be trimmed using the circuit in Figure 3 by placing a low frequency square wave (V_l=0V, V_h=2V) into V_g (with V_{in} set to zero volts) and adjusting R1 until the CLC520 output produces a steady DC value. After adjusting the input-referred offset, adjust R2 (with V_{in}=0, V_g=0) until V_{out} is zero. Finally, in inverting applications V_{in} may be applied to pin 6 and the offset adjustment to pin 3. This offset trim does not improve output offset temperature coefficient.

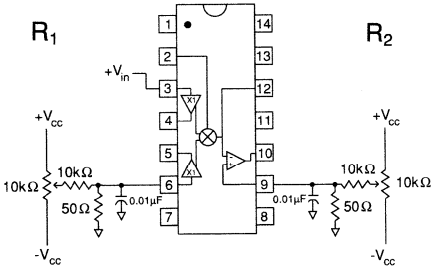


Figure 3: CLC520 Offset Adjustment Circuitry (other external elements not shown)

Selecting component values

Maximum input amplitude and maximum gain are the two key specifications that determine component values in a CLC520 application.

The output stage op amp is a current-feedback type amplifier optimized for R_f=1kΩ. R_g can then be computed as:

$$R_g = \frac{R_f \cdot 1.85}{A_{vmax}} - 3.0\Omega \text{ with } R_f = 1k\Omega \quad (1)$$

To determine whether the maximum input amplitude will overdrive the CLC520, compute:

$$V_{dmax} = (R_g + 3.0\Omega) \cdot 0.00135 \quad (2)$$

the maximum differential input voltage for linear operation.

If the maximum input amplitude exceeds this limit, the CLC520 should either be moved to a location in the signal chain where amplitudes are reduced, A_{vmax} should be reduced or the values for R_g and R_f should be increased.

If the input amplitude is reduced, recompute the impact of the CLC520 on signal-to-noise ratio. If A_{vmax} is reduced,

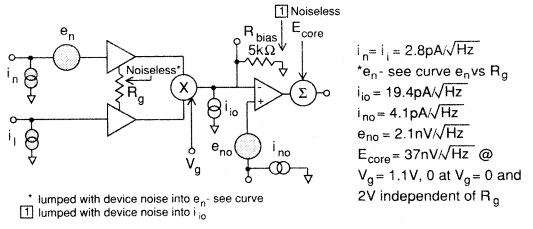


Figure 4: CLC520 Noise Model

"downstream" amplifier gain should be increased, or another gain stage added to make up for reduced A_{vmax}.

To increase R_g and R_f, compute the lowest acceptable value for R_g:

$$R_g > 740 \cdot V_{dmax} - 3\Omega \quad (3)$$

where $V_{dmax} = (+V_{in}) - (-V_{in})$, the largest expected peak differential input voltage. Operating with R_g larger than this value insures linear operation of the input buffers.

R_f may be computed from the selected R_g and A_{vmax}:

$$R_f = \frac{A_{vmax} \cdot (R_g + 3.0\Omega)}{1.85} \quad (4)$$

R_f should be >=1kΩ. R_f<1kΩ can be implemented using a loop gain reducing resistor to ground on the inverting summing node of the output amplifier (see application note OA-13).

Printed Circuit Layout

A good high-frequency PCB layout including ground plane construction and power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the I− input (pin 12); keep trace area small. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

For best performance at low maximum gains (A_{vmax}<10) R_g+ and R_g− connections should be treated in a similar fashion. Capacitance to ground should be minimized by removing the ground plane from under the body of R_g.

Parasitic or load capacitance directly on the output (pin 10) degrades phase margin leading to frequency response peaking. A small series resistor before this capacitance, if present, effectively decouples this effect (see Settling Time vs. Capacitive Load).

Precision buffed resistors (PRP8351 series from Precision Resistive Products) must be used for R_f for rated performance. Precision buffed resistors are suggested for R_g for low gain settings (A_{vmax}<10). Carbon composition resistors and RN55D metal-film resistors may be used with reduced performance.

Evaluation PC boards (part no. 730021) for the CLC520 are available from Comlinear at minimal cost.

Predicting the output noise

Seven noise sources (e_n, i_n, i_i, i_{io}, i_{no}, e_{no}, E_{core}) are used to model the CLC520 noise performance (Figure 4). e_n, i_n, and i_i model the equivalent input noise terms for the input buffer while i_{io}, i_{no}, and e_{no} model the noise terms for the output buffer. To simplify the model e_n includes the effect of resistor R_g (see Figure 5 for e_n vs R_g). To simplify the model further, R_{bias} is assumed noiseless and its noise contribution is included in i_{io}.

An additional term E_{core} mimics the active device noise contribution from the Gilbert multiplier core. Core noise is theoretically zero when the multiplier is set to maximum gain or zero gain (V_g>1.6V or V_g<0.63V respectively at room temperature) and reaches a maximum of 37nV/√Hz at A_{vmax}/2.

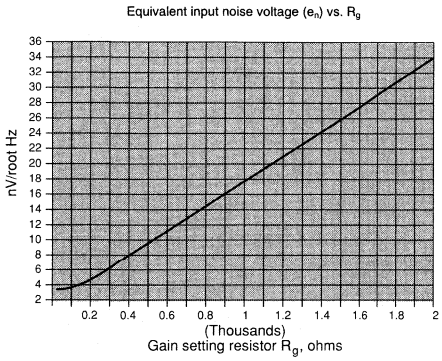


Figure 5

Several points should be made concerning this model. First, external component noise contributions need to be factored in when computing total output referred noise. The only exception is R_g, where its noise contribution is already factored in. Second, the model ignores flicker noise contributions. Applications where noise below approximately 100KHz must be considered should use this model with caution. Third this model very accurately predicts output noise voltage for the typical application circuit (see above) but will be less accurate the further component values deviate from those in the typical application circuit. In general, however, the model should predict the equivalent output noise above the flicker noise region to within a few dB of actual performance over the normal range of A_{vmax} and component values.

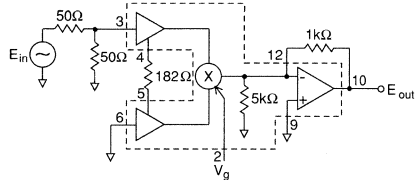


Figure 6: Typical Circuit

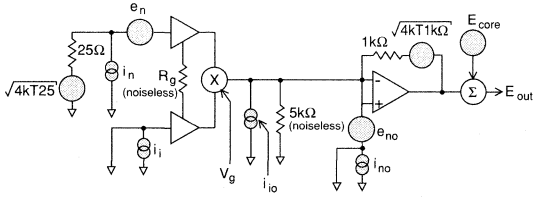


Figure 7: Noise Model for Typical Circuit

Calculating CLC520 output noise in a typical circuit

To calculate the noise in a CLC520 application, the noise terms given for the amplifier as well as the noise terms of the external components must be included. To clarify the techniques used, output noise in a typical circuit will be calculated. (Figure 6)

The noise model is depicted in Figure 7. The diagram assumes spot noise sources with $V_{rms}/\sqrt{Hz}$ and $Amps_{rms}/\sqrt{Hz}$ units. The Thevenin equivalent of the source and input termination is used: 25Ω in series with a noise voltage source. R_g is assumed noiseless since its effect is included in e_n. The internal 5kΩ resistor at the CLC520 core output is also assumed noiseless since its effect is included in i_{io}. The noise contribution from R_f is modeled as a noise voltage source.

The easiest way to analyze the output noise of this circuit is to break the analysis into three pieces: an input buffer noise calculation, an output buffer noise calculation, and a core noise calculation. The output contribution of the input buffer varies with the gain. The output contribution of the output buffer is constant. The core noise contribution is zero at maximum and minimum gain and reaches a peak at $A_{vmax}/2$. Summing the noise powers for each of these terms gives the total output noise power.

Since we assume all noise terms are uncorrelated, the equivalent input noise voltage squared is given by:

$$E_{it}^2 = 4kT25 + (I_n 25)^2 + e_n^2$$

i_i does not contribute to the input buffer noise because the input buffer inverting input is grounded. e_n is taken from Figure 5.

The equivalent output buffer noise is given by:

$$E_{ot}^2 = (i_{io} \cdot 1k\Omega)^2 + 4kT(1k\Omega) + \left[e_{no}\left(1 + \frac{1k\Omega}{5k\Omega}\right)\right]^2$$

I_{no} does not contribute to the output buffer noise because the output buffer non-inverting input is grounded.

The core noise is already output referred and is $37nV/\sqrt{Hz}$ at $V_g = 1.1$ ($A_{vmax}/2$) and approaches zero as A_v goes to 0 or A_{vmax}.

The total output noise voltage is given by:

$$E_{TOTAL}^2 = E_{it}^2 A_v^2 + E_{ot}^2 + C E_{core}^2$$

Where A_v is the input to output voltage gain (which varies as V_g varies).

C accounts for the variation in core noise contribution as V_g is adjusted. C = 1 when gain A_v is $A_{vmax}/2$. C is zero at A_{vmax} and $A_v = 0$ and varies between 0 and 1 for all other values.

Using these equations, total calculated output noise for the circuit was $20nV/\sqrt{Hz}$ at minimum gain, $49nV/\sqrt{Hz}$ at mid-gain, and $53nV/\sqrt{Hz}$ at maximum gain.

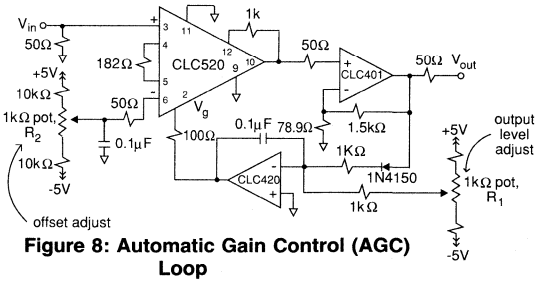


Figure 8: Automatic Gain Control (AGC) Loop

AGC circuits

Figure 8 shows a typical AGC circuit. The CLC520 is followed up with a CLC401 for higher overall gain. The output of the CLC401 is rectified and fed to an inverting integrator using a CLC420 (wideband voltage feedback op amp). When the output voltage, V_{out}, is too large the integrator output voltage ramps down reducing the net gain of the CLC520 and V_{out}. If the output voltage is too small, the integrator ramps up increasing the net gain and the output voltage. Actual output level is set with R1. To prevent shifts in DC output voltage with changes in input signal level, trim pot R2 is provided. AGC circuits are always limited in the range of input signals over which constant output level can be maintained. In this circuit, we would expect that reasonable AGC action could be maintained over the gain adjustment range of the CLC520 (at least 40dB). In practice, rectifier dynamic range limits reduce this slightly.

Evaluation Board

Evaluation PC boards (part number 730029 for through-hole and 730023 for SOIC) for the CLC520 are available.

Comlinear Corporation

Wideband Variable Gain Amplifier

Preliminary CLC522

APPLICATIONS:

- high-speed analog signal processing
- RF modulators & mixers
- automatic gain control & leveling loops
- video production switching
- instrumentation
- voltage controlled filters

FEATURES (typical):

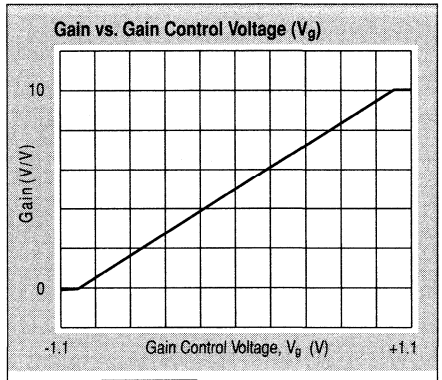
- linear wideband (165MHz) gain control
- 165MHz signal channel bandwidth
- differential voltage input; single-ended voltage output
- 0.05% signal channel nonlinearity
- adjustable maximum gain
- 40dB variable gain range
- -50/-65dBc 2nd/3rd harmonic distortion
- 0.15%, 0.08° differential gain, phase

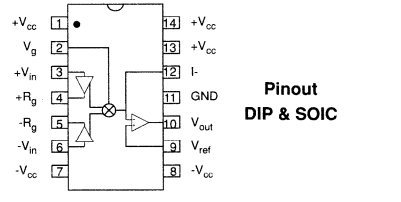
DESCRIPTION

The CLC522 variable gain amplifier (VGA) is a dc-coupled, two-quadrant multiplier with differential voltage inputs and a single-ended voltage output. The CLC522 is a complete VGA system which does not require external buffering since two input buffers and an output op amp are integrated with the multiplier core. Only two external resistors are needed to set the CLC522's maximum gain and gain control is easily achieved through a single high impedance voltage input. The CLC522 provides a linear in V/V relationship between the amplifier's gain and the gain-control input voltage.

The CLC522's maximum gain may be set externally over a nominal range of 2V/V to 100V/V with the gain control input providing a 40dB gain range down from the maximum setting. For example, set for a maximum gain of 100V/V, the CLC522 will provide a 100V/V to 1V/V gain control range by sweeping the gain control input through its full scale range of +1V to -1V.

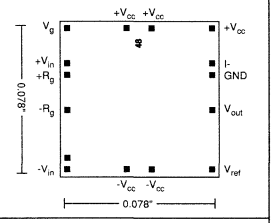
Set at a maximum gain of 10V/V, the CLC522 provides a 165MHz signal channel bandwidth and a 165MHz gain control bandwidth. Gain nonlinearity over the full 40dB gain range is 0.5% and gain accuracy at the maximum gain of 10V/V is typically ±0.3%.





Pinout DIP & SOIC

Chip Topography

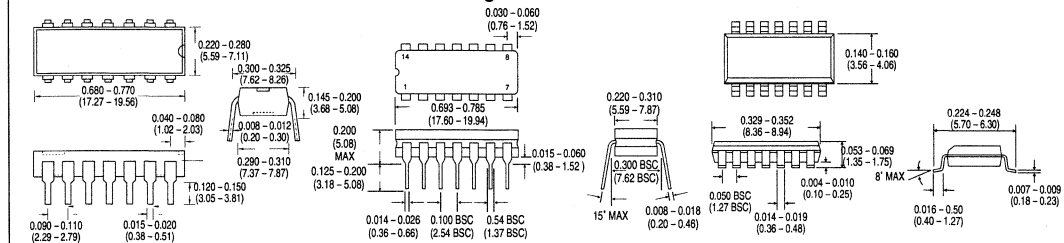


The CLC522 is available in the following versions.

CLC522AJP	-40°C to +85°C	14-pin Plastic DIP
CLC522AJE	-40°C to +85°C	14-pin Plastic SOIC
CLC522AIB	-40°C to +85°C	14-pin CERDIP
CLC522A8B	-55°C to +125°C	14-pin CERDIP, MIL-STD-883, Level B
CLC522A8L-2	-55°C to +125°C	20-pin LCC, MIL-STD-883, Level B
CLC522ALC	-55°C to +125°C	dice
CLC522AMC	-55°C to +125°C	dice, MIL-STD-883, Level B

Contact factory for other packages and DESC SMD number.

Package Dimensions



Comlinear Corporation * 4800 Wheaton Drive, Fort Collins, CO 80525 * (303) 226-0500 * FAX (303) 226-0564

CLC522 Electrical Characteristics ($\pm V_{cc}$=±5V, R_L=100Ω, R_f=1kΩ', R_g=182Ω', A_V=+10V/V, V_g=+1.1V)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS				UNITS
Ambient Temperature	CLC522AJ/AI	+25°C	0° to 70°C	-40°C	+25°C	+85°C	
Ambient Temperature	CLC522A8	+25°C		-55°C	+25°C	+125°C	
FREQUENCY RESPONSE							
†small signal bandwidth	V_{out} < 0.5V_{pp}	165	115	110	120	110	MHz
	V_{out} < 5.0V_{pp}	150	95	100	100	90	MHz
gain control bandwidth	V_{out}, V_g < 0.5V_{pp}	165	115	110	120	110	MHz
gain flatness	V_{out} < 0.5V_{pp}						
† peaking	DC-30MHz	0	0.1	0.1	0.1	0.1	dB
† rolloff	DC-30MHz	0.05	0.25	0.4	0.25	0.25	dB
† peaking	DC-200MHz	0	0.5	0.5	0.5	0.7	dB
† rolloff	DC-60MHz	0.3	1.0	1.3	1.0	1.0	dB
linear phase deviation	DC-60MHz	0.5	1.1	1.2	1.0	1.2	°
†feedthrough	30MHz, V_g < -1.1V_{DC}	-62	-57	-57	-57	-57	dB
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	2.2	3.0	2.9	2.9	3.2	ns
	5.0V step	3.0	5.0	5.0	5.0	5.0	ns
settling time to ±0.1%	2.0V step	12	18	18	18	18	ns
overshoot	0.5V step	2	15	15	15	15	%
slew rate	4V step	2000	1400	1400	1400	1400	V/µsec
DISTORTION AND NOISE PERFORMANCE							
†2nd harmonic distortion	2V_{pp}, 20MHz	-50	-44	-44	-44	-44	dBc
†3rd harmonic distortion	2V_{pp}, 20MHz	-65	-56	-58	-58	-54	dBc
equivalent output noise	(see noise model)						
noise floor	1-200MHz	-132	-129	-130	-130	-129	dBm_{1Hz}
spot noise	1-200MHz	58	65	62	62	68	nV/√Hz
STATIC DC PERFORMANCE							
*integral signal nonlinearity	V_{out}=4V_{pp}	0.04	0.1	0.1	0.1	0.1	%
gain control nonlinearity		0.5	2.2	3.0	2.0	2.5	%
input bias current		15	47	82	38	38	µA
average temperature coefficient		125	300	600	---	210	nA/°C
gain error	A_V = 10V/V	±0.0	±0.5	+0.5,-1.0	±0.5	±0.5	dB
*output offset voltage		25	95	120	85	90	mV
average temperature coefficient		100	350	400	---	300	µV/°C
*input bias current		9	26	45	21	21	µA
average temperature coefficient		65	175	275	---	125	nA/°C
input offset current		0.2	3.0	4.0	2.0	2.0	µA
average temperature coefficient		5	30	40	---	20	nA/°C
†power supply sensitivity	output referred	10	40	40	40	40	mV/V
♠common mode rejection ratio	input referred	70	59	59	59	59	dB
*supply current	no load	46	62	63	61	61	mA
MISCELLANEOUS PERFORMANCE							
V_{in} signal inputs	resistance	1500	450	175	650	650	kΩ
	capacitance	1.0	2.0	2.0	2.0	2.0	pF
*V_{in} differential voltage range	V_{in} = I_T· R_g	±320	±230	±250	±250	±210	mV
buffer tail current (I_T)		1.8	1.26	1.37	1.37	1.15	mA
V_{in} common mode voltage range		±2.2	±1.2	±1.4	±1.2	±1.2	V
V_g control input	resistance	100	30	15	38	38	kΩ
	capacitance	1.0	2.0	2.0	2.0	2.0	pF
V_g input voltage	A_V = 10V/V	990±0	±60	±60	±60	±60	mV
	A_V = 0V/V	-975±0	±80	±80	±80	±80	mV
output impedance	DC	0.1	0.3	0.6	0.2	0.2	Ω
output voltage range	no load	±4.0	±3.6	±3.5	±3.7	±3.7	V
output current		±70	±40	±25	±47	±47	mA

Absolute Maximum Ratings

V_{cc}	±7.0V
I_{out}	96mA
common mode input voltage	±V_{cc}
differential input voltage	±10V
maximum junction temperature	+175°C
operating temperature range	
AJ:	-40°C to +85°C
AI:	-40°C to +85°C
A8, AM, AL:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

Recomended gain range: ±2 to ±100V/V

Notes:

* AJ,AI : 100% tested at +25°C, sample +85°C.

† AJ : Sample tested at +25°C.

† AI : 100% tested at +25°C.

* A8 : 100% tested at +25°C, -55°C, +125°C.

† A8 : 100% tested at +25°C, sample at -55°C, +125°C

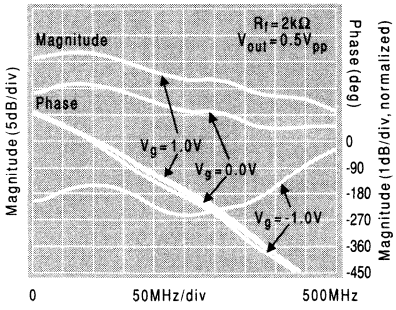
* AL, AM : 100% wafer probed +25°C to +25°C min/max specifications.

♠ SMD : Sample tested at +25°C, -55°C, +125°C.

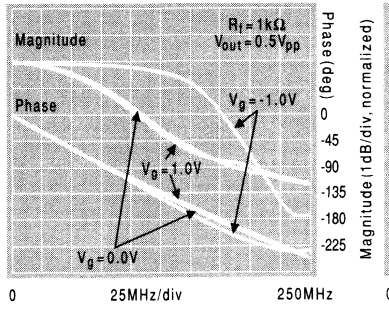
note 1) : CLC522AJE version tested and guaranteed with R_f=866Ω, R_g = 165Ω.

CLC522 Typical Performance Characteristics (T_A=25°C, V_{CC}=±5V, R_f=100Ω, R_f=1kΩ, R_f=182Ω, A_v=+10, V_o=2V)

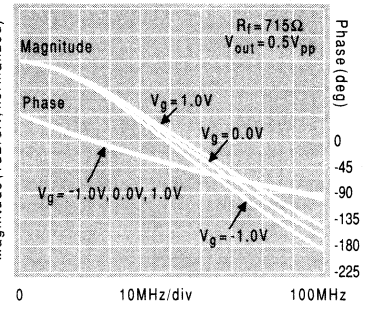
Frequency Response, A_{vmax} = +2



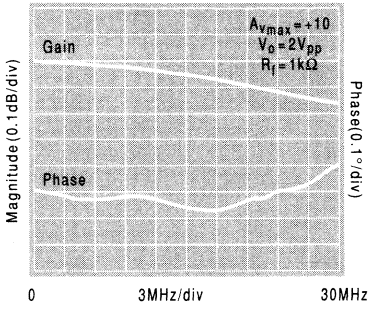
Frequency Response, A_{vmax} = +10



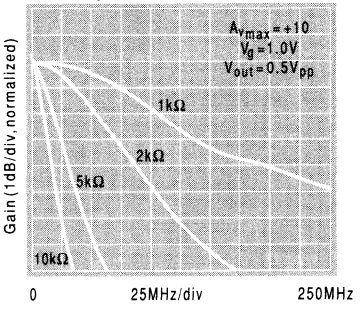
Frequency Response, A_{vmax} = +100



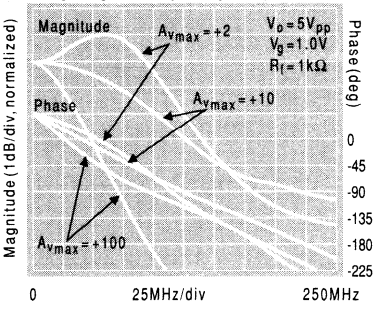
Gain Flatness & Linear Phase Deviation



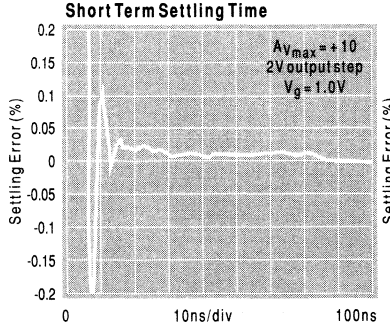
Small Signal Gain vs. R_f



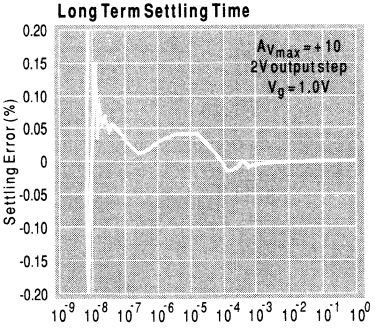
Large Signal Frequency Response



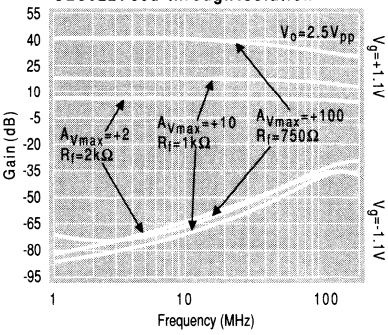
Short Term Settling Time



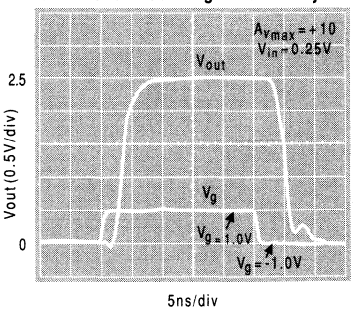
Long Term Settling Time



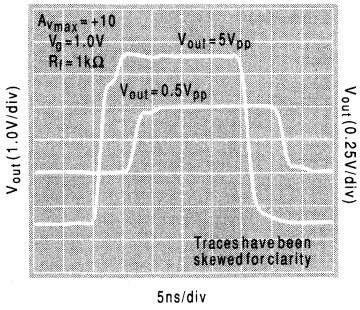
CLC522 Feed-through Isolation



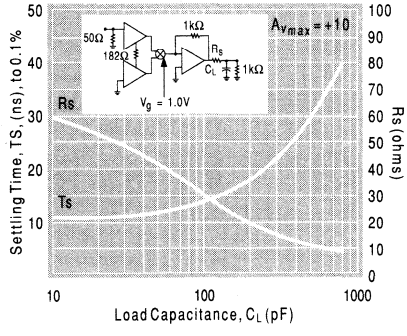
Gain Control Settling Time & Delay



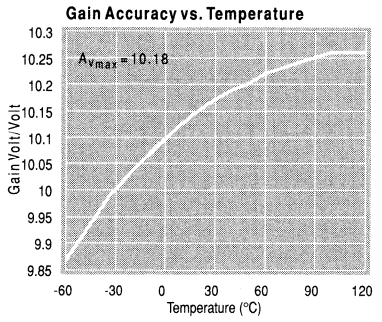
Large & Small Signal Pulse Response

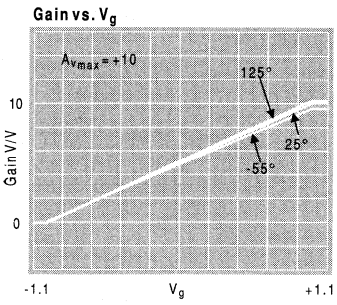


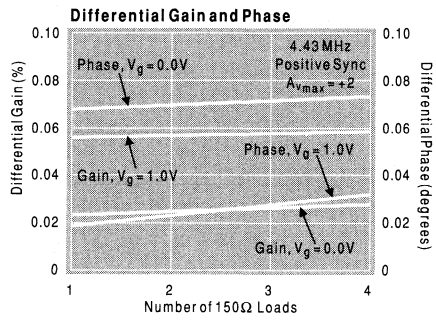
Settling Time vs. Capacitive Load

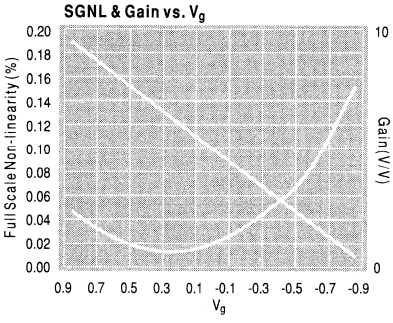


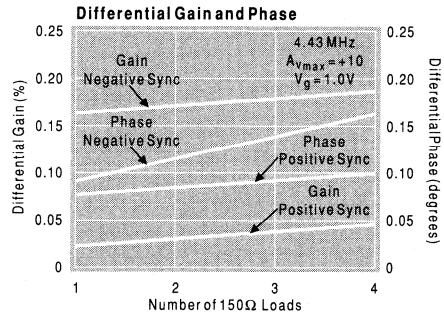
CLC522 Typical Performance Characteristics (T_A=25°C, V_{CC}=±5V, R_L=100Ω, R_f=1kΩ, R_g=182Ω, A_v=+10, V_g=+2V)











Designing with the CLC522

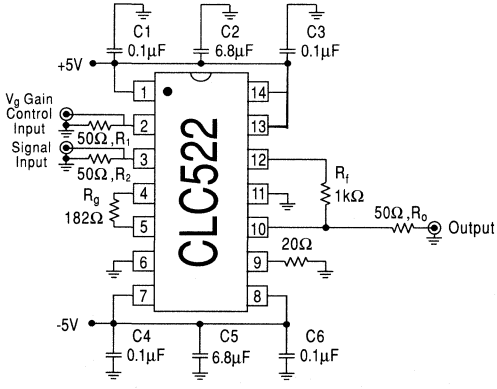


Figure 1: CLC522 typical application circuit

The CLC522 is a wideband variable gain amplifier. A voltage input signal may be applied differentially between the two inputs, or single-ended by grounding the unused differential input (see figure 1, Typical application circuit). The CLC522 input buffers convert the input voltage to a current. This current is a function of the input voltage and the value of R_g, the gain-setting resistor. A voltage-controlled two-quadrant multiplier attenuates this current. The multiplier output current is then converted to a voltage via the output amplifier. This output amplifier is a current feedback amplifier configured as a transimpedance amplifier. The transimpedance gain is the feedback resistor, R_f. The input signal, output, and gain control are all voltages.

The maximum gain is a function of the ratio, R_f/R_g, more specifically,

$$G_{max} = \frac{R_f * 1.85}{R_g + 3\Omega} \qquad \textbf{Eq. 1}$$

The maximum input voltage, V_{dmax}, which can be accommodated by the V-I conversion of the input buffers is a function of R_g,

$$V_{dmax} = (R_g + 3\Omega) * 1.35mA \qquad \textbf{Eq. 2}$$

The 1.35mA is the minimum guaranteed current available in the V-I converter. Typically this current is 1.75mA.

Comparing equations 1 and 2, it can be seen that the maximum available gain, G_{max}, is inversely proportional to R_g. The maximum input voltage for linear operation, V_{dmax}, is directly proportional to R_g. Large maximum gains with large input signals are possible when all factors affecting the CLC522 performance are understood.

The effect of R_g on both G_{max} and V_{dmax} suggests the following design procedure to get the most out of the CLC522. First, R_g is determined based on the maximum input signal. V_{dmax} is a peak voltage. Once this maximum peak input voltage is known, R_g, in ohms, is calculated:

$$R_g = \frac{V_{dmax}}{1.35mA} - 3\Omega \qquad \textbf{Eq. 3}$$

This value of R_g is then used to calculate R_f, in ohms:

$$R_f = \frac{G_{max}(R_g + 3\Omega)}{1.85} \qquad \textbf{Eq. 4}$$

Since the output amplifier is a current feedback amplifier, the value of R_f has a profound affect on the small-signal bandwidth and stability of a current feedback amp. A complete discussion of the feedback resistor's influence on the performance of current feedback amps can be found in OA-20, "Current Feedback Myths Debunked", and OA-13, "Current Feedback Loop Gain Analysis and Performance Enhancements". A first-order approximation would be that doubling the value of the recommended R_f cuts the bandwidth in half.

The value of R_f calculated from equation 4 must then be reviewed for its effect on circuit bandwidth and stability. R_f less than 1kΩ is not recommended, except for high G_{max}. This datasheet uses an R_f of 715Ω for G_{max} = 100V/V. Higher R_f will reduce bandwidth. This can be seen in the typical plots. If the resulting values of R_f and R_g reduce bandwidth excessively, the design goals must be reconsidered. R_g can be reduced if the maximum input voltage requirement is relaxed.

Typically a conflict arises in designs with large input signals and large maximum gain. An example is an input dynamic range of 40dB (V_{in}(peak) = 1V to 10mV) with a desired constant output of 1V(peak). In this case the gain must range from a minimum of 1V/V (unity gain when V_{in} = 1V) to a maximum of 100V/V (40dB for V_{in} = 10mV). In this case R_g = 738Ω, R_f = 40kΩ. A feedback resistor this large is not practical for noise reasons, and will severely limit the bandwidth of the CLC522. If the input-to-output dynamic range requirement can be reduced to 20dB (G_{max} = 10V/V), R_f is then 4kΩ. These circuit values will yield a constant output voltage of 100mV, with an approximate bandwidth of 40MHz. A constant gain-of-10V/V amplifier can follow the CLC522 for the desired final output voltage of 1V. The recommended values for G_{max} = 10V/V are R_g = 182Ω and R_f = 1kΩ. These values result in a circuit with a small-signal bandwidth of 165MHz and a maximum input voltage of 250mV(peak).

Printed Circuit Layout

A good high-frequency PCB layout including ground plane and power supply bypassing are essential for optimum performance. The amplifier is sensitive to stray capacitance to ground at the I-input (pin 12); keep trace area small and remove ground plane near the input pins. Shunt capacitance across R_f must not be used to compensate for this effect as is often done with voltage feedback op-amps. Keep in mind that ground plane beneath R_f will add undesirable shunt capacitance, as well as capacitance to ground.

Symmetric traces from R_g to pins 4 and 5 will yield the best results. Capacitance to ground can be minimized by removing ground plane from under the body of R_g.

High-frequency ceramic bypass capacitors must be used on each of the five power supply pins (1, 13, 14, 7, 8). The $-V_{CC}$ pin is particularly important in this respect. The signal gain is determined by the difference in potential between V_g (pin 2) and $-V_{CC}$ on pin 7. Any variation in the voltage on pin 7 will translate directly to a change in gain.

Parasitic or load capacitance, C_l on the output (pin 10) degrades phase margin and can lead to frequency response peaking. A small series resistor between pin 10 and C_l decouples this effect (see the plot "Settling Time vs. Capacitive Load for a Recommended R_s").

The non-inverting input of the output op-amp (pin 9) must be kept near ground potential. A 20Ω resistor to ground improves the frequency response of this amp. It does not, however, improve offsets due to bias current effects.

Adjusting Offset

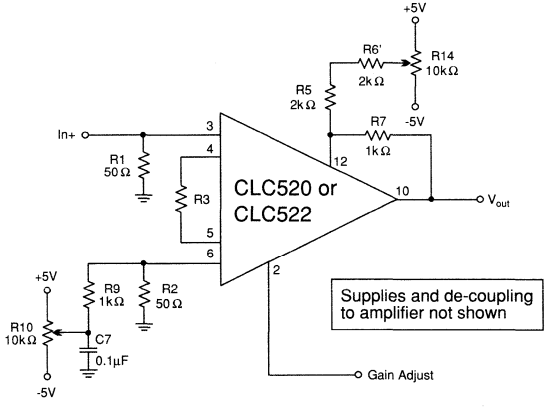


Figure 7: Input and output stage DC nulling

The output stage offset should be trimmed prior to the input stage. With the gain adjust pin set at minimum gain (maximum attenuation), the output stage offset may be nulled independently from the input stage. R14 should be adjusted to yield the desired output error voltage (typically <1mV). Having corrected for the input offset voltage and bias current errors of the output amplifier, returning the gain adjust pin to the maximum gain voltage will allow the input buffer stage DC offset errors to be corrected. With no input signal present, but with matched source impedances at each of the two buffer inputs, R10 of Figure 7 can be adjusted to bring the output to within the desired error band.

Adjusting the input and the output stage offsets at the two gain extremes will hold the output DC error at a minimum at these two points in the gain range. If a more limited gain range is anticipated, the adjustments should be made at these operating points. The non-linear DC error introduced by the multiplier core will cause a residual, gain dependent, offset to appear at the output as the gain is swept from minimum to maximum. Also, neither the input nor the output offset adjustments described here will improve temperature drift effects. For more information, contact Comlinear Corporation for the final data sheet.

Evaluation PC boards, part numbers 730029 (through-hole) and 730033 (surface mount) are available from Comlinear at minimal cost.

Design Equations : $A_{vmax} = \frac{R_f \times 1.85}{R_g + 3.0}$

$A_v = (A_{vmax}/2)(V_g+1)$

$V_{dmax} = (R_g + 3.0) \times 0.00135$

Where : $A_v = \frac{V_{out}}{(+V_{in})-(-V_{in})}$

A_{vmax} = maximum gain

R_f = feedback resistor, R_g = gain resistor

V_{dmax} = maximum differential voltage

Notes:

The recommended value of R_f is 1kΩ. It is recommended that the value of the gain setting resistor (R_g) be adjusted to change the maximum gain (A_{vmax}). The recommended range of A_{vmax} is ±2 to ±100.

The input buffers are current limited. Consequently, the maximum differential input voltage range (V_{dmax}) that is guaranteed for linear operation, is proportional to the value chosen for R_g (given in the equation above).

Unity Gain Buffer and Linear Amplifiers

Contents

Comlinear Corporation

DC to 1.1GHz Linear Amplifier

CLC104

APPLICATIONS:

- digital and wideband analog communications
- radar, IF and RF processors
- fiber optic drivers and receivers
- photomultiplier preamplifiers

FEATURES:

- -3dB bandwidth of 1.1GHz
- 325psec rise and fall times
- 14dB gain, 50Ω input and output
- low distortion, linear phase
- 1.4:1 VSWR (output, DC-1.1GHz)

DESCRIPTION

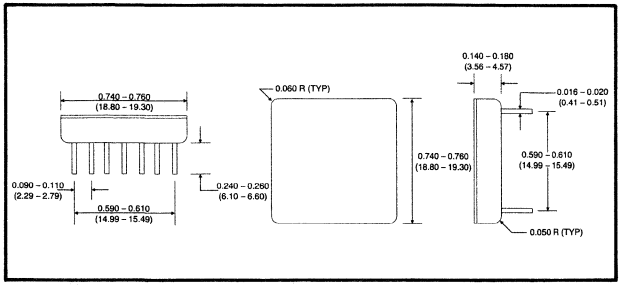
Comlinear Corporation's CLC104 Linear Amplifier represents a significant advance in linear amplifiers. Proprietary design techniques have yielded an amplifier with 14dB of gain and a −3dB bandwidth of DC to 1100MHz. Gain flatness to 750MHz of ±0.4dB coupled with excellent VSWR and phase linearity gives outstanding pulse fidelity and low signal distortion.

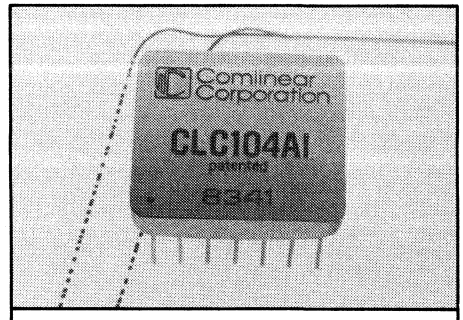
Designed for 50Ω systems, the CLC104 is very easy to use, requiring only properly bypassed power supplies for operation. This translates to time- and cost-savings in all stages of design and production.

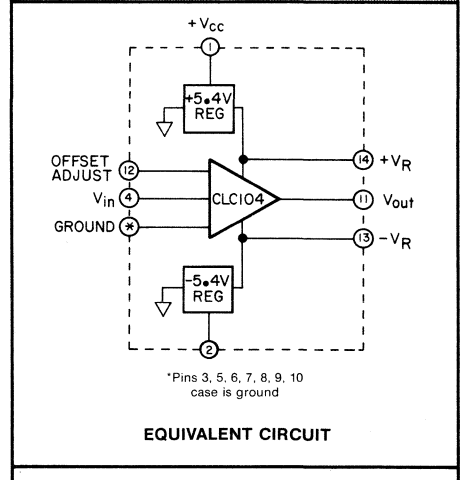
Fast rise time, low overshoot and linear phase make the CLC104 ideal for high speed pulse amplification. These properties plus low distortion combine to produce an amplifier well suited to many communications applications. With a 1.1GHz bandwidth, the CLC104 can handle the fastest digital traffic, even when the demodulation scheme or the digital coding format requires that DC be maintained. It is also ideal for traditional video amplifier applications such as radar or wideband analog communications systems.

These same characteristics make the CLC104 an excellent choice for use in fiber optics systems, on either the transmitting or receiving end of the fiber. The low group delay distortion insures that pulse integrity will be maintained. As a photomultiplier tube preamp, its fast response and quick overload recovery provide for superior system performance.

The CLC104 is constructed using thin film resistor/bipolar transistor technology. The CLC104AI is specified over a temperature range of −25°C to +85°C. The device is packaged in a 14-pin double-wide DIP package.







EQUIVALENT CIRCUIT

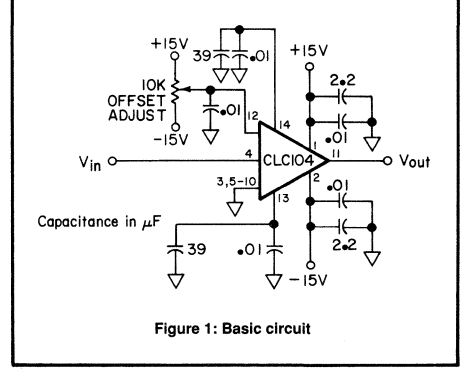


Figure 1: Basic circuit

Electrical Characteristics (at 25°C, $R_S = R_L = 50\Omega$, $V_{CC} = \pm 15V$)

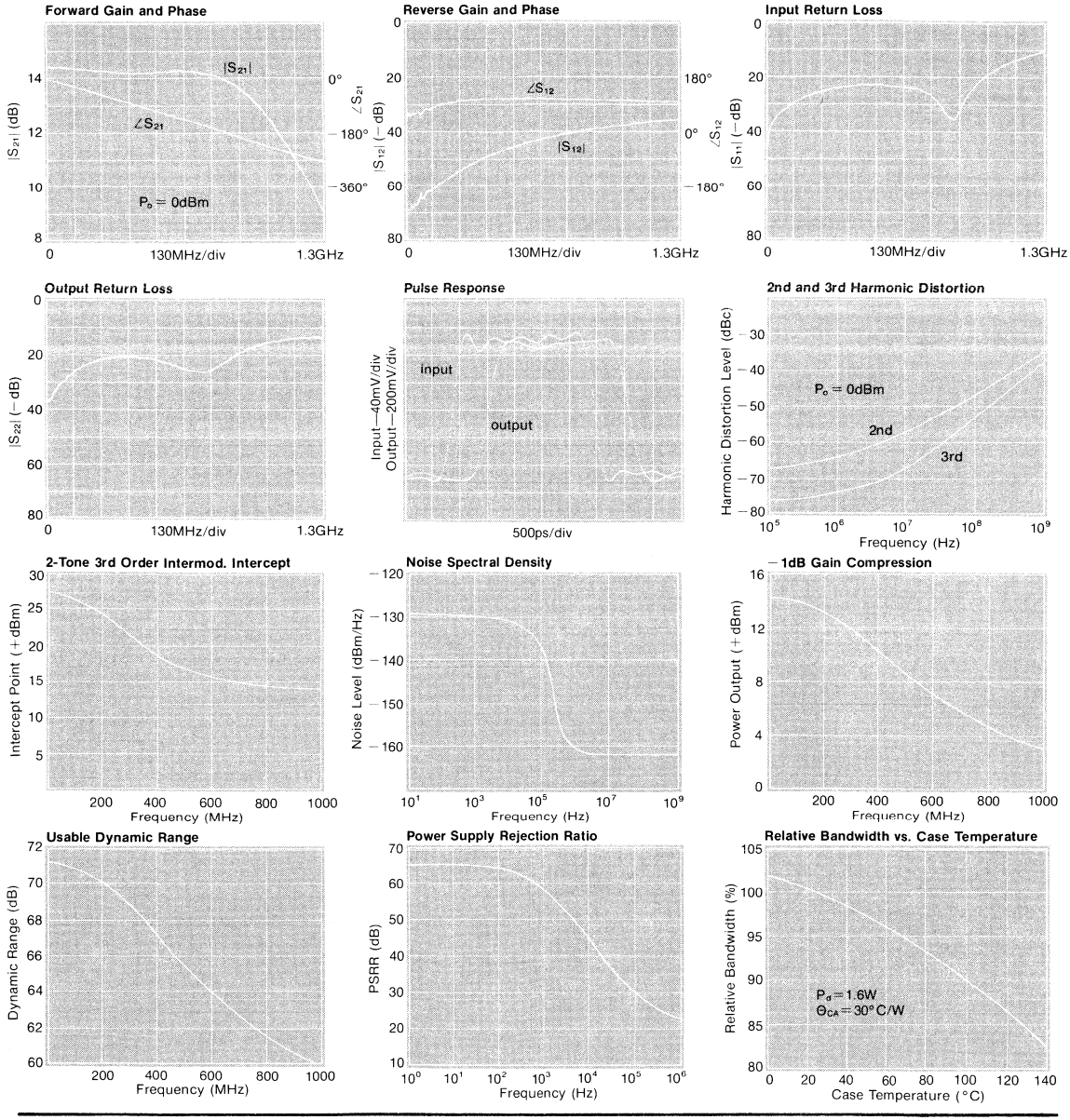
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature	CLC104AI				
FREQUENCY DOMAIN RESPONSE					
* –3dB bandwidth	0dBm out	1000	1100		MHz
–3dB bandwidth	10dBm out		1050		MHz
* non-inverting gain	at 100 MHz, note 1	13.8	14.2	14.9	dB
* gain flatness	DC - 750MHz	-.6	±.4	+.6	dB
deviation from linear phase	DC - 600MHz		1.5	3	degree
group delay			600		ps
* reverse isolation	DC - 750MHz	40	45		dB
	750MHz - 1100MHz	35	40		dB
* input VSWR	DC - 750MHz		1.2:1	1.35:1	
	750MHz - 1100MHz		1.4:1	1.6:1	
* output VSWR	DC - 750MHz		1.2:1	1.35:1	
	750MHz - 1100MHz		1.4:1	1.6:1	
TIME DOMAIN RESPONSE					
rise and fall time	1V output step		325	375	ps
(10% to 90%)	2V output step		375	450	ps
overshoot and aberrations	1V output step		3		%
settling time	to 0.8%, 1V step		1.2		ns
overload recovery	V_{inpeak} = ±0.5V		1.2	1.6	ns
DISTORTION AND NOISE PERFORMANCE					
* second/third harmonics at 100MHz	0dBm		47/53		-dBc
(see graph)	*10dBm	30/35	44/43		-dBc
third order intermodulation intercept	100MHz		26		+dBm
(two tone, 1MHz separation; see graph)	500MHz		17		+dBm
equivalent input noise voltage	10Hz to 1200MHz		55		μV_{rms}
noise figure			11		dB
usable dynamic range	100MHz		71		dB
	500MHz		65		dB
GENERAL INFORMATION					
input bias current (drift)	note 2		80(0.6)	280(2.0)	μA(μA/°C)
output offset voltage (drift)	note 3		50(375)	250(625)	mV(μV°C)
* supply current (no load)			54	60	±mA
supply rejection (at 1KHz; see graph)			55		db

Absolute Maximum Ratings

supply voltage range	±9V to 16V
input voltage	±0.5V
output current	40mA
output voltage (short circuit protection)	±3.5V
operating temperature	-25°C to 85°C
storage temperature	-65°C to 150°C
junction temperature	175°C

note 1: nominal gain only – gain variation over temperature is ±0.1dB
note 2: (input bias current) X (R_S | 50Ω) = input offset voltage
note 3: output offset can be adjusted to zero with an external potentiometer – see "Reducing DC Offset"
note 4: * = final electrical test parameter, 100% tested at 25°C

Typical Performance Characteristics (at 25° C, R_L = 50Ω, V_{cc} = ±15V)



PC Board Layout Considerations

Proper layout of printed circuit boards is important to achieve optimum performance of a circuit operating in the 1GHz frequency range. Use of microstripline is recommended for all signal-carrying paths and low resistance, low inductance signal return and bypass paths should be used. To keep the impedance of these paths low, use as much ground plane as is possible. Ground plane also serves to increase the flow of heat out of the package.

The CLC104 has three types of connections: signal paths (input and output), DC inputs (supplies and offset adjust), and grounds. 50Ω microstrip is recommended for connection to the input (pin 4) and output (pin 11). Microstrip on a double-sided PC board consists of a ground plane on one side of the board and a constant-width signal-carrying trace on the other side of the board. For 1/16" G10 or FR-4 PC board material, a 0.1" wide trace will have a 50Ω characteristic impedance. The ground plane beneath the signal trace must extend at least one trace width on either side of the trace. Also, all traces (including ground) should be kept at least one trace width from the signal carrying traces.

To keep power supply noise and oscillations from appearing at the amplifier output, all supply pins should be capacitively bypassed to ground. The power supply pins (1 and 2) are the inputs to a pair of voltage regulators whose outputs are at pins 13 and 14. It is recommended that 0.01μF or larger ceramic capacitors be connected from pins 1, 2, 13 and 14 to ground, within 0.2" of the pins. A 1μF or larger solid tantalum capacitor to ground is required within 3" of pins 1 and 2, and for good low frequency performance, solid tantalum capacitors of at least 15μF should be connected from pins 13 and 14 to ground within 3" of the pins. Use 0.025" or wider traces for the supply lines. The offset adjust pin (12) also requires bypassing; a 0.01μF or larger ceramic capacitor to ground within 0.2" of the pin is recommended.

Grounding is the final layout consideration. Pins 3 and 5-10 should all be connected to a ground plane which should cover as much of one side of the board around the amplifier as possible.

Reducing DC Offset

DC offset of the CLC104 may be adjusted by applying a DC voltage to the amplifier's offset adjust pin (12). The simplest method is shown in Figure 1. Using this method of offset adjust it is possible to vary the output offset by approximately ±400mV. This simple adjustment has no effect on the offset drift characteristics of the CLC104.

If lower offset and offset drift are required, a low frequency op amp may be used in conjunction with the CLC104 in a composite configuration. The suggested circuit appears in Figure 2. Its method of operation is to compare an attenuated version of the output signal to the input signal and apply a correcting voltage at the offset adjust pin. A compensation capacitor C_s reduces the bandwidth of the op amp correction circuit to limit the op amp's effect on the CLC104 to frequencies below f_{45}, the frequency at which the op amp has 45dB of open loop gain. Using an LM108, f_{45} is about 7Hz with $C_s = .1\mu F$. Thus the op amp can correct DC and low frequency errors below f_{45}, without affecting CLC104 performance above f_{45}. Also note that the noise performance of the op amp will dominate below f_{45}.

With an LM108 op amp in this composite configuration, input offset is typically 2mV and drift is 15μV/° C. At frequencies well below f_{45}, the composite gain is equal to $(1+49.9K/(R_a+R_b))$ and the output impedance is very low. As the signal frequency increases beyond f_{45}, the op amp loses influence and the CLC104 gain and output impedance dominate. To ensure a smooth transition and matched gain at all frequencies, adjust R_b for a minimum op amp output swing with a $0.1V_{pp}$ sine wave input (to the CLC104) at the frequency f_{45}. Since the CLC104 has a 50Ω output impedance, its output voltage is a function of the load impedance ($A_v \simeq 10R_L/(R_L+50)$), whereas the gain of the composite amplifier at low frequencies and DC is relatively independent of the load impedance, due to the high open-loop gain of the op amp. Thus, to avoid gain mismatching and phase nonlinearity, use the composite amplifier only if the load impedance is constant from DC to at least $10(f_{45})$.

Use of a composite amplifier reduces input offset voltage and its corresponding drift, but has no effect on input bias current. This current is converted to an input voltage by the resistance to ground seen at the amplifier input and the voltage appears, amplified, at the output. Typical input offset voltage due to the bias current is 2mV and input offset drift is approximately 15μV/° C.

Thermal Considerations

The CLC104 case must be maintained at or below 140° C. Note that because of the amplifier design, power dissipation remains fairly constant, independent of the load or drive level. Therefore, standard derating is not possible. There are two ways to keep the case temperature low. The first is to keep the amount of power dissipated inside the package to a minimum and the second is to get the heat out of the package quickly by reducing the thermal resistance from case to ambient.

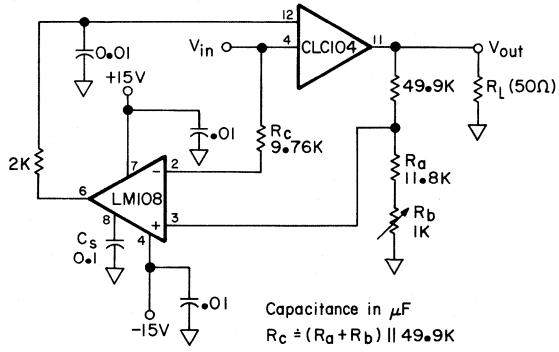


Figure 2: Composite amplifier

A large portion of the heat dissipated inside the package is in the voltage regulators. At the minimum ±9V supply level the regulators dissipate 390mW and at the maximum ±16V supply level they dissipate 1.2W.

The amplifier itself dissipates a fairly constant 600mW (55mA × 10.8V). Reducing the power dissipation of the internal regulators will go far towards reducing the internal junction temperatures without impacting the ac performance. Reducing either the input supply voltages (on pins 1 and 2) and/or shunting the regulator current through external resistors (from pins 1 to 14 and pins 2 to 13) are both effective means towards significantly reducing the internal power dissipation. A minimum voltage across the regulator of 3.6V and a minimum regulator current of 10ma will satisfy the regulator dropout voltage and current limits.

Given the maximum anticipated power supply voltages, the shunt resistor should be calculated to yield a 35mA current from that voltage to the regulated voltage of 5.4V. This will leave 10ma through the regulator at the minimum quiescent current of 45mA. The regulator input voltages may be reduced directly by dropping the voltage supplies, or, if that option is not available, using either a zener or resistive dropping element in series with the supply. If a series dropping element is used, the decoupling capacitors must appear on pins 1 and 2 of the CLC104. Figure 3 shows two possible power reduction circuits from fixed ±15V supplies.

Several methods of decreasing the thermal resistance from case to ambient are possible. With no heat paths other than still air at 25°C, the thermal resistance from case to ambient for the CLC104 is about 40° C/W. When placed in a printed circuit board with all ground pins soldered into a ground plane 1" × 1.5", the thermal resistance drops to about 30° C/W. In this configuration, the case rise will be 30°C for 9V supplies and 50°C for 16V supplies. This results in maximum allowable ambient temperatures of 110°C and 90°C, respectively. If higher operating temperatures are required, heat sinking of the package is recommended.

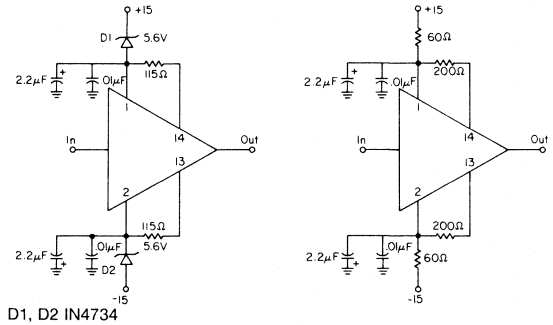


Figure 3: Reducing Power Dissipation

Comlinear Corporation

Wideband, Closed-Loop Monolithic Buffer Amplifier

CLC110

APPLICATIONS:

- ultra-fast flash A/D conversion
- line driving
- high speed communications
- impedance transformation
- power buffers
- IF processors

FEATURES:

- closed-loop, unity-gain operation
- −3dB bandwidth of 730MHz ($0.5V_{pp}$)
- 0.2% settling in 5ns
- low power, 150mW
- low distortion, −65dBc at 20MHz

DESCRIPTION:

Using a unique closed-loop design, the CLC110 buffer offers a high-fidelity, high-performance alternative to conventional open-loop buffers. For example, the −3dB bandwidth is 730MHz ($0.5V_{pp}$) and the settling time to 0.2% is typically only 5ns. Yet all this is achieved while maintaining excellent signal fidelity as demonstrated by the −65dBc harmonic distortion at 20MHz – a value unmatched by any high-speed buffer.

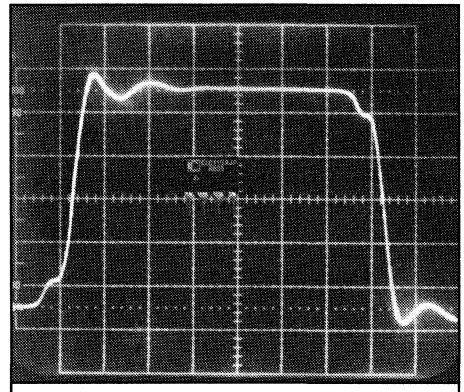
The CLC110 is an ideal choice for a wide variety of applications. With its speed and accuracy, the CLC110 offers designers the benefit of buffering signals which might otherwise go unbuffered due to performance penalties imposed by conventional buffers. For example, the CLC110 is well suited for use within closed-loop systems such as amplifier or phase locked loop systems; with its 400ps rise time, its effect on loop dynamics is usually negligible.

Ultra-fast flash A/D converter systems can also benefit from the speed of the CLC110. And, since most flash A/D's have capacitive inputs, the CLC110's dynamic performance has been characterized for various loads. In addition, the amplifier specifications are for a 100Ω load.

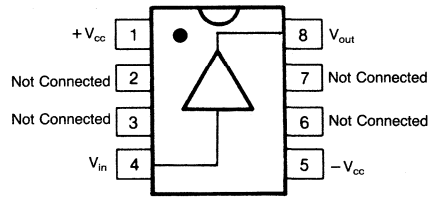
The CLC110 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC110AJP	−40°C to +85°C	8-pin plastic DIP
CLC110AJE	−40°C to +85°C	8-pin plastic SOIC
CLC110AIB	−40°C to +85°C	8-pin hermetic CERDIP
CLC110A8B	−55°C to +125°C	8-pin hermetic CERDIP, MIL-STD-883, Level B
CLC110ALC	−55°C to +125°C	dice
CLC110AMC	−55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

Contact factory for other packages. DESC SMD number, 5962-89975.

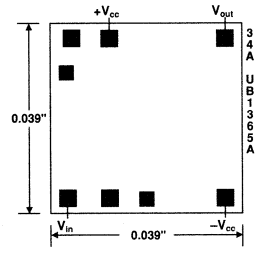


PINOUT



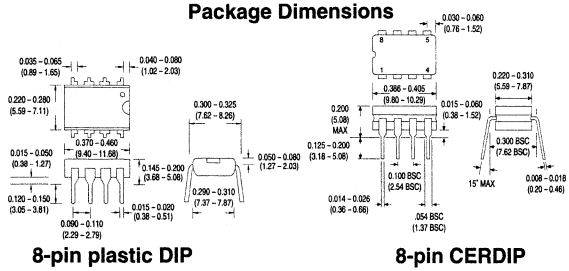
DIP and SOIC Versions

Chip Topography



Height is 0.014 inches. NOTE: Backside connected to −V_{cc}. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



8-pin plastic DIP **8-pin CERDIP**

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

DS110.04 January 1993

Electrical Characteristics ($R_L = 100\Omega$, $R_s = 50\Omega$, $V_{cc} = \pm 5V$)

PARAMETERS	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC110AJ/AI	+25°C	−40°C	+25°C	+85°C		
Ambient Temperature	CLC110A8/AM/AL	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN PERFORMANCE[1]							
−3dB bandwidth	$V_{out} < 0.5V_{pp}$	730	>400	>400	>300	MHz	SSBW
	$V_{out} < 5V_{pp}$	90	>50	>55	>50	MHz	LSBW
gain flatness[2]	$V_{out} < 0.5V_{pp}$						
† peaking	DC to 200MHz	0	<0.8	<0.5	<0.6	dB	GFPH
† rolloff	DC to 200MHz	0	<1.0	<0.8	<1.2	dB	GFRH
group delay	DC to 200MHz	0.75	<1.0	<1.0	<1.2	ns	GD
linear phase deviation	DC to 200MHz	0.7	<1.5	<1.5	<2.0	°	LPD
TIME DOMAIN PERFORMANCE[1]							
rise and fall time	0.5V step	0.4	<1.0	<1.0	<1.4	ns	TRS
(input signal rise/fall = 300ps)							
overshoot	0.5V step	0	<15	<10	<15	%	OS
(input signal rise/fall = 300ps)							
rise and fall time	5V step	4.5	<8.5	<7.5	<8.5	ns	TRL
(input signal rise/fall ≦ 1ns)							
settling time to ±0.2%	2V step	5	<10	<10	<10	ns	TSP
slew rate		800	>450	>500	>450	V/μs	SR
DISTORTION AND NOISE PERFORMANCE							
2nd harmonic distortion							
†	$2V_{pp}$, 20MHz	−65	<−48	<−55	<−55	dBc	HD2
	$2V_{pp}$, 50MHz	−60	<−48	<−55	<−55	dBc	HHD2
3rd harmonic distortion							
†	$2V_{pp}$, 20MHz	−65	<−55	<−55	<−55	dBc	HD3
	$2V_{pp}$, 50MHz	−60	<−50	<−50	<−45	dBc	HHD3
equivalent input noise							
noise floor	> 1MHz	−158	<−155	<−155	<−154	dBm(1Hz)	SNF
integrated noise	1MHz to 200MHz	40	<57	<57	<63	μV	INV
STATIC, DC PERFORMANCE							
small signal gain into 100Ω load		0.97	>0.95	>0.96	>0.95	V/V	GA
integral endpoint linearity	±2V full scale	0.2	<0.8	<0.4	<0.3	%FS	ILIN
* output offset voltage		2	<16	<8.0	<13	mV	VIO
average temperature coefficient		20	<100	—	<50	μV/°C	DVIO
* input bias current		20	<100	<50	<50	μA	IBN
average temperature coefficient		200	<700	—	<300	nA/°C	DIBN
† power supply rejection ratio		50	>45	>45	>45	dB	PSRR
* supply current	no load	15	<20	<20	<20	mA	ICC
MISCELLANEOUS PERFORMANCE							
input resistance		160	>50	>100	>200	kΩ	RIN
capacitance		1.6	<2.5	<2.2	<2.5	pF	CIN
output impedance	at DC	2	<3.5	<3.0	<3.5	Ω	RO
output voltage range	100Ω load	±4	>±3.0	>±3.2	>±3.2	V	VO
output current	−40°C to +85°C	±70	>±45	>±50	>±50	mA	IO
	−55°C to +125°C	±70	>±40	>±50	>±50	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but, maximum reliability will be obtained if I_{out} does not exceed...	70mA
input voltage	$\pm V_{cc}$
junction temperature	+175°C
operating temperature range	
AI/AJ:	−40°C to +85°C
A8/AM/AL:	−55°C to +125°C
storage temperature range	−65°C to +150°C
lead solder duration (+300°C)	10 sec

Miscellaneous Ratings

Notes:

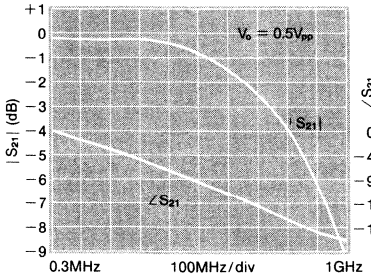
*	AI, AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested at +25°C, −55°C, +125°C.
†	A8	100% tested at +25°C, sample at −55°C, +125°C.
*	AL, AM	100% wafer probe tested at +25°C to +25°C min/max specifications.

note 1: AC performance is very dependent on layout. Specifications apply only in a 50Ω microstrip environment.

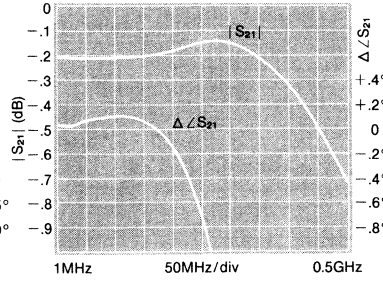
note 2: Gain flatness tests are performed from 0.1MHz to 200MHz.

Typical Performance Characteristics ($V_{cc} = \pm 5V$, $R_L = 100\Omega$, $R_s = 50\Omega$)

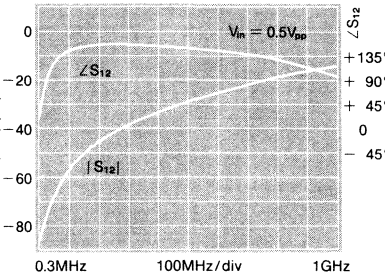
Forward Gain and Phase



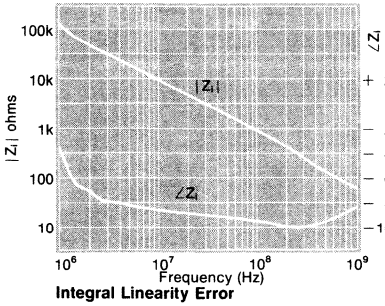
Gain Flatness & Deviation from Linear Phase



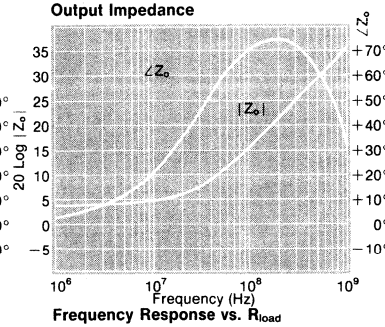
Reverse Gain and Phase



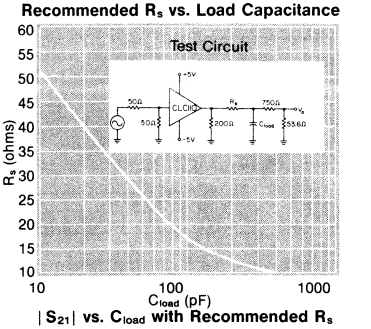
Input Impedance



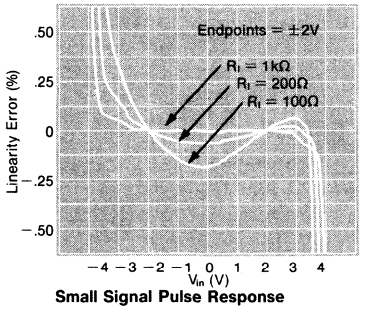
Output Impedance



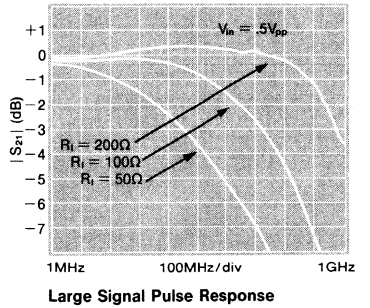
Recommended R_s vs. Load Capacitance



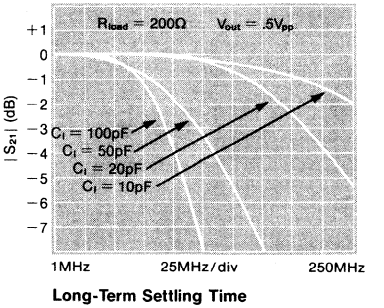
Integral Linearity Error



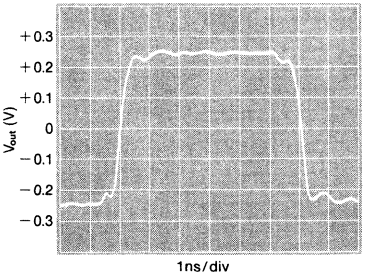
Frequency Response vs. R_{load}



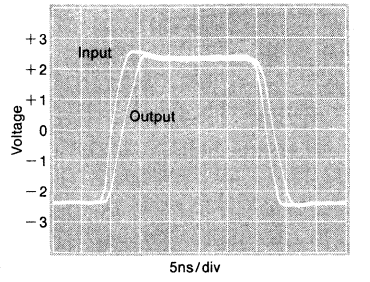
$|S_{21}|$ vs. C_{load} with Recommended R_s



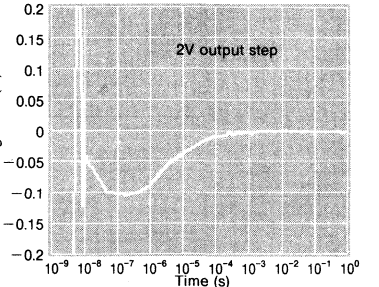
Small Signal Pulse Response



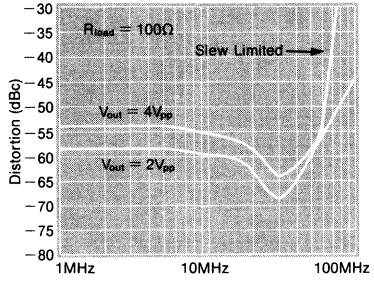
Large Signal Pulse Response



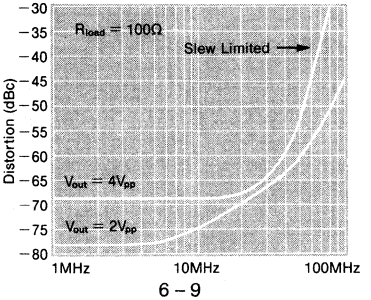
Long-Term Settling Time



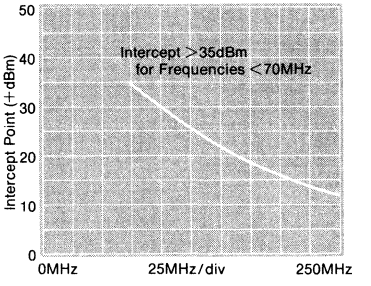
2nd Harmonic Distortion



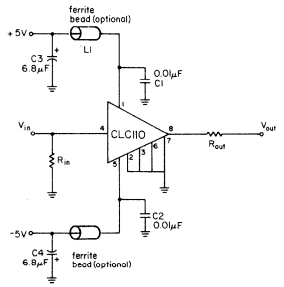
3rd Harmonic Distortion



2-Tone, 3rd Order Intermodulation Intercept



6



R_{in} is chosen for desired input impedance.

R_{out} is chosen for desired output impedance. (CLC110 $R_{out} = 2\Omega$)

Figure 1: recommended circuit and evaluation board schematic

Operation

The CLC110 is based upon a unique, patented closed-loop design, which provides the accuracy characteristics of a closed-loop amplifier, yet also has unmatched dynamic performance.

Printed Circuit Layout and Supply Bypassing

As with any high-frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the CLC110, which has a typical bandwidth of 730MHz.

To minimize capacitive feedthrough, the pins not connected internally (pins 2, 3, 6, and 7) should be connected to the ground plane. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the CLC110. On a 0.065 inch epoxy PCB material, a 50Ω transmission line (commonly called stripline) can be constructed by using a trace width of 0.1" over a complete ground plane.

Figure 1 shows recommended power supply bypassing. The ferrite beads are optional and are recommended only where additional isolation is needed from high-frequency (>400MHz) resonances of the power supply.

Parasitic or load capacitance directly on the output of the CLC110 will introduce additional phase shift in the device, which can lead to decreased phase margin and frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and the resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products), which have low parasitic reactances, were used to develop the data sheet specifications. Precision carbon composition resistors or standard spirally-trimmed RN55D metal film resistors will work, though they will cause a degradation of AC performance due to their reactive nature at high frequencies.

Evaluation Board

An evaluation board (part number 730012) is available for the CLC110 to assist in the evaluation of the CLC110. It may also be used as a guide in developing a printed circuit layout. Figure 1 shows the board's schematic; Figures 2 through 4 show the board layout.

Evaluation Board Parts List:

R_{in}	select for desired input impedance
R_{out}	select for desired output impedance
C_1, C_2	0.1μF ceramic radial lead
C_3, C_4	6.8μF (Sprague 150D series)
L_1, L_2	ferrite beads (optional) (Ferroxcube #VK 200 19/4B)

Hardware (optional)
SocketsCambion flush-mount connector jacks
(#450-2598-01-06-00)
SMA Connectors (female)
Amphenol 901-144 (straight)
Amphenol 901-143 (angled)

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly qualified applications engineers to provide technical and design assistance.

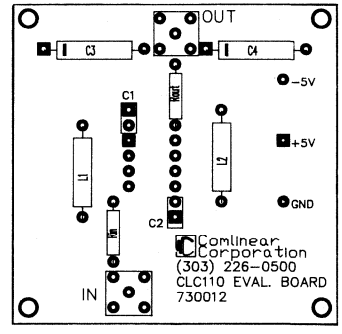


Figure 2: component placement guide

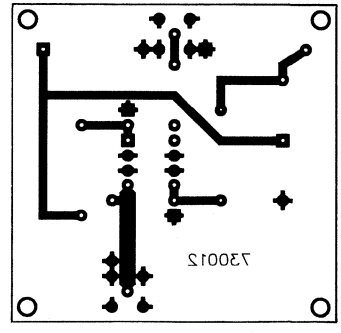


Figure 3: solder side (bottom) as viewed from component side (top)

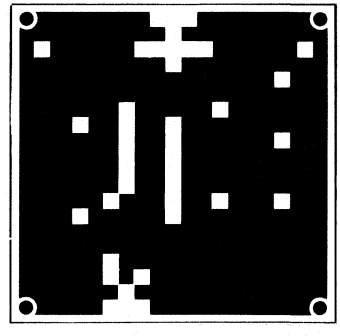


Figure 4: component side (top) showing extensive ground plane

Comlinear Corporation

Quad, Low-Power Video Buffer

CLC114

APPLICATIONS:
- video crosspoint switch driver
- video distribution buffers
- video switching buffers
- video signal multiplexing
- instrumentaion amps
- active filters

FEATURES (typical):
- closed-loop, quad buffer
- 200MHz small-signal bandwidth
- 450V/μs slew rate
- low power, 30mW per channel ($\pm$5V supplies)
- 62dB channel isolation (10MHz)
- specified for crosspoint switch loads

DESCRIPTION:

The CLC114 is a high-performance, closed-loop quad buffer intended for power sensitive applications. Requiring only 30mW of quiescent power dissipation per channel ($\pm$5V supplies), the CLC114 offers a small signal bandwidth of 200MHz ($0.5V_{pp}$) and a slew rate of 450V/μs.

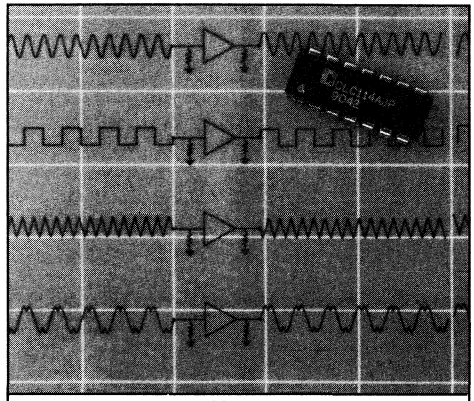
Designed specifically for high density crosspoint switch and analog multiplexer applications, the CLC114 offers excellent linearity and wide channel isolation (62dB @ 10MHz). Driving a typical crosspoint switch load, the CLC114 offers differential gain and phase performance of 0.08% and 0.1%; gain flatness through 30MHz is typically 0.1dB.

With its patented closed-loop topology, the CLC114 has significant performance advantages over conventional open-loop designs. Applications requiring low output impedance and true unity gain stability through very high frequencies (active filters, dynamic load buffering, etc.) will benefit from the CLC114's superior performance.

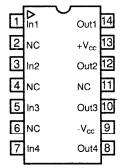
Constructed using an advanced, complementary bipolar process and Comlinear's proven high-speed architectures, the CLC114 is available in several versions to meet a variety of requirements.

CLC114 AJP	–40°C to +85°C	14-pin plastic DIP
CLC114 AJE	–40°C to +85°C	14-pin plastic SOIC
CLC114 AIB	–40°C to +85°C	14-pin hermetic CERDIP
CLC114 A8B	–55°C to +125°C	14-pin hermetic CERDIP, MIL-STD-883, Level B
CLC114 ALC	–55°C to +125°C	dice
CLC114 AMC	–55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

Contact factory for other packages. DESC SMD number 5962-92339

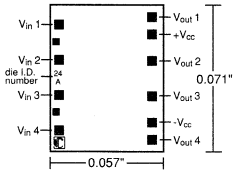


Pinout



DIP and SOIC versions

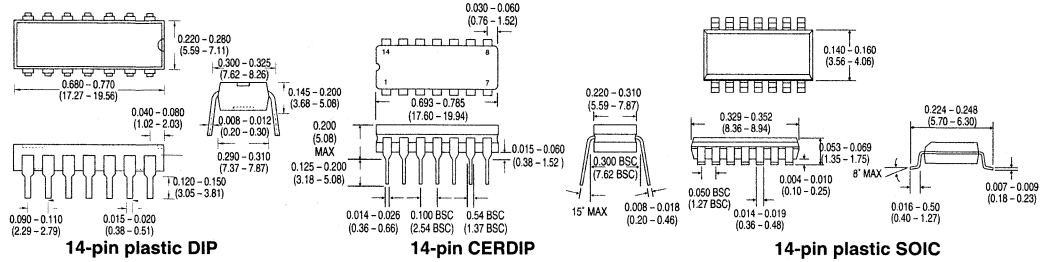
Chip Typography



Height is 0.014 inches.

NOTE: Backside connected to -V_{cc}. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

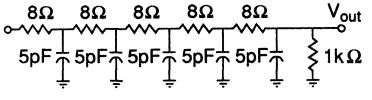
Electrical Characteristics ($V_{cc} = \pm 5V$, $R_L = 100\Omega$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC114AI/AJ	+25°C	−40°C	+25°C	+85°C		
Ambient Temperature	CLC114A8/AL/AM	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
†−3dB bandwidth	$V_{out}<0.5V_{pp}$	200	>135	>135	>120	MHz	SSBW
	$V_{out}<2V_{pp}$	95	>70	>70	>70	MHz	LSBW
gain flatness[1]	$V_{out}<0.5V_{pp}$						
† peaking	DC to 30MHz	0.0	<0.3	<0.2	<0.3	dB	GFPL
† peaking	30MHz to 200MHz	0.0	<1.3	<0.4	<0.5	dB	GFPH
† rolloff	DC to 60MHz	0.1	<0.8	<0.8	<1.0	dB	GFR
crosstalk (all hostile)	10MHz	62	>58	>58	>60	dB	XT
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	1.8	<2.8	<2.8	<3.0	ns	TRS1
	2V step	5	<7	<7	<8	ns	TRS2
settling time to 0.1%	2V step	10	<15	<15	<20	ns	TS1
to 0.01%	2V step	20	<30	<30	<40	ns	TS01
overshoot	0.5V step	3	<15	<10	<15	%	OS
slew rate		450	>180	>200	>180	V/μs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	$2V_{pp}$, 20MHz	−50	<−36	<−38	<−38	dBc	HD2
†3rd harmonic distortion	$2V_{pp}$, 20MHz	−58	<−50	<−50	<−45	dBc	HD3
equivalent noise input noise floor	>1MHz	−155	<−153	<−153	<−153	dBm_{1Hz}	SNF
STATIC, DC PERFORMANCE							
small signal gain	100Ω load	0.97	>0.95	>0.96	>0.96	V/V	GA
integral endpoint linearity	±1V, full scale	0.4	<1.0	<0.6	<0.5	%	ILIN
*output offset voltage		±0.5	<±8.2	<±5.0	<±8.0	mV	VIO
average temperature coefficient		±9.0	<±40	—	<±30	μV/°C	DVIO
*input bias current		±1.0	<±10	<±5	<±4	μA	IBN
average temperature coefficient		±6.0	<±62	—	<±25	nA/°C	DIBN
†power supply rejection ratio		56	>48	>48	>46	dB	PSRR
*supply current, total	no load, quiescent	12.0	<17.0	<16.5	<16.0	mA	ICC
MISCELLANEOUS PERFORMANCE							
input resistance		1.5	>0.3	>1.0	>2.0	MΩ	RIN
input capacitance		1.8	<3.5	<3.0	<3.5	pF	CIN
output impedance	DC	2.5	<5.0	<3.5	<3.5	Ω	RO
output voltage range	no load	±4.0	>±3.6	>±3.8	>±3.8	V	VO
output current		25	>12	>20	>25	mA	IO

Performance Driving a Crosspoint Switch

PARAMETERS	CONDITIONS	TYP	UNITS
gain flatness $V_{out}<2V_{pp}$	DC to 5MHz	±0.02	dB
$V_{out}<2V_{pp}$	DC to 30MHz	±0.1	dB
differential gain	3.58 & 4.43MHz	0.08	%
differential phase	3.58 & 4.43MHz	0.1	°
2nd harmonic distortion	5MHz, $2V_{pp}$	−60	dBc
	30MHz, $2V_{pp}$	−43	dBc
3rd harmonic distortion	5MHz, $2V_{pp}$	−58	dBc
	30MHz, $2V_{pp}$	−43	dBc
crosstalk (all hostile)	5MHz	58	dB
	10MHz	54	dB
	30MHz	42	dB

Test Load



Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	35mA
input voltage	$\pm V_{cc}$
maximum junction temperature	+175°C
operating temperature range	
AJ/AI:	−40°C to + 85°C
A8/AM/AL:	−55°C to + 125°C
storage temperature range	−65°C to + 150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

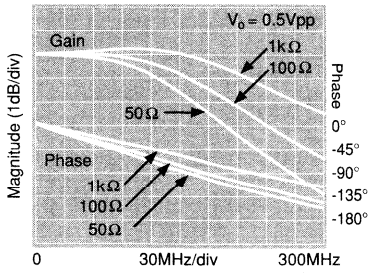
NOTES:

*	AI,AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested at +25°C, −55°C, +125°C.
†	A8	100% tested at +25°C, sample at −55°C, +125°C.
*	AL, AM	100% wafer probe tested at +25°C to +25°C specifications.

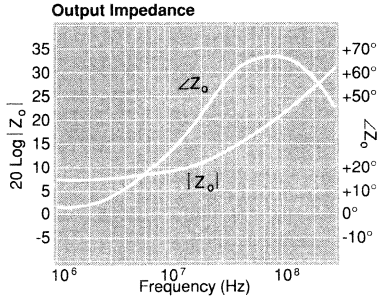
note 1: Gain flatness tests are performed from 0.1MHz.

Typical Performance Characteristics (T_A=+25°C, V_{CC}=±5V, R_L=100Ω)

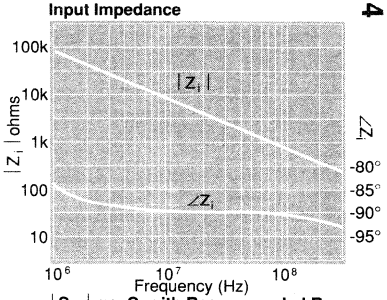
Gain and Phase vs. Load



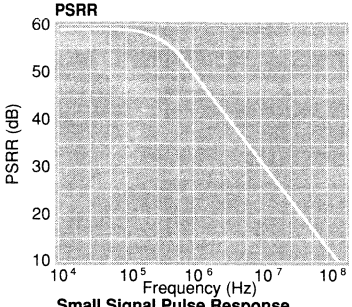
Output Impedance



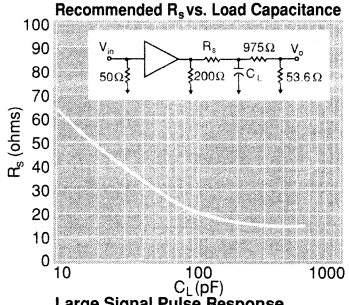
Input Impedance



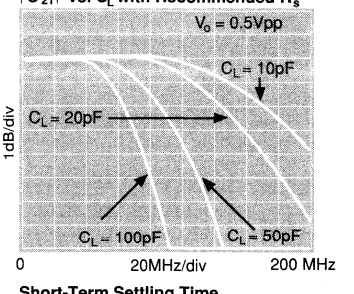
PSRR



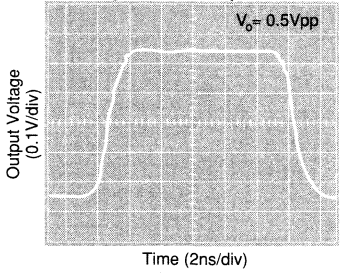
Recommended R_s vs. Load Capacitance



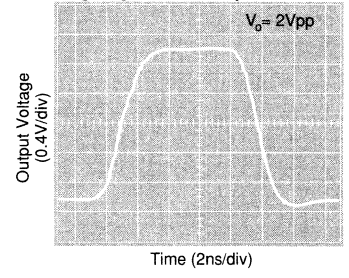
|S_{21}| vs. C_L with Recommended R_s



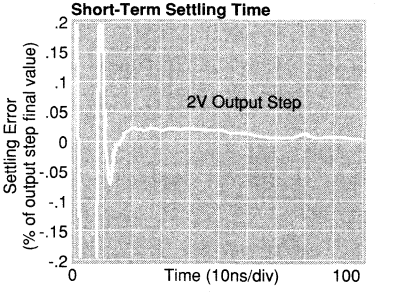
Small Signal Pulse Response



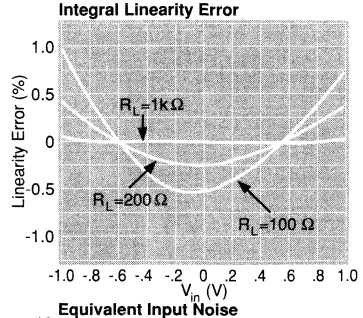
Large Signal Pulse Response



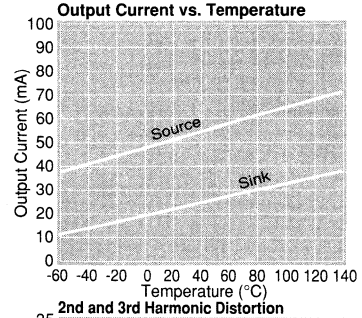
Short-Term Settling Time



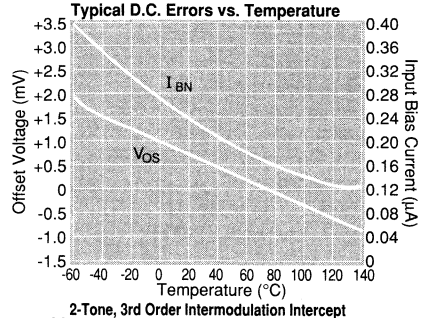
Integral Linearity Error



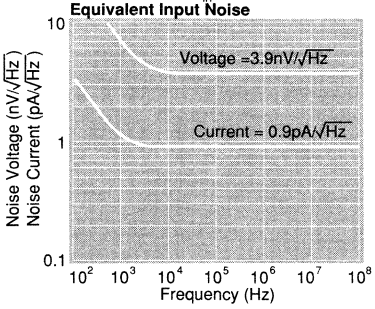
Output Current vs. Temperature



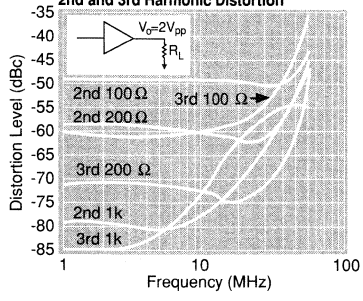
Typical D.C. Errors vs. Temperature



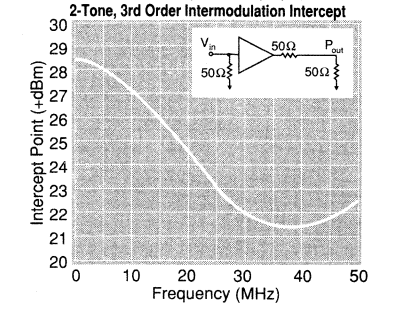
Equivalent Input Noise



2nd and 3rd Harmonic Distortion



2-Tone, 3rd Order Intermodulation Intercept



6

Operation

The CLC114 is a quad, low-power, high-speed, unity-gain buffer. The closed loop topology provides accuracy not found in open loop designs. The input stage incorporates a slew-enhancement circuit which allows low quiescent power without sacrificing ac performance.

PC Board Layout and Crosstalk

High frequency devices demand a good printed circuit board layout for optimum performance. The CLC114, with power gain to 200 MHz, is no exception. A ground plane and power supply bypassing with good high-frequency ceramic capacitors in close proximity to the supply pins is essential. Second harmonic distortion can be improved by ensuring equal current return paths for both the positive and the negative supplies. This can be accomplished by grounding the bypass capacitors at the same point in the ground plane while keeping the power supply side of the bypass capacitors within 0.1" of the CLC114 supply pins.

Crosstalk (undesired signal coupling between buffer channels) is strongly dependent on board layout. Closely spaced signal traces on the circuit board will degrade crosstalk due to intertrace capacitance. For this reason it is recommended that unused package pins (2, 4, 6, 11) be connected to the ground plane for better channel isolation at the device pins. Similarly, crosstalk can be improved by using a grounded guard trace between signal traces. This will reduce the distributed capacitance between signal lines.

Following are two graphs depicting the effects of crosstalk. All-hostile crosstalk is measured by driving three of the four buffers simultaneously while observing the fourth, undriven, channel. Figure 2, "All-Hostile Crosstalk Isolation", shows this effect as a function of input signal frequency. R_L is the resistive load for each driven channel. Figure 3, "Most Susceptible Channel-to-Channel Pulse Coupling", describes one effect of crosstalk when one channel is driven with a 2Vpp step (tr = 5ns) while the output of the undriven channel is measured. From Figure 2 it can be observed that crosstalk decreases as the signal frequency is reduced. Similarly, the pulse coupling crosstalk will decrease as the rise time increases.

Evaluation Board

An evaluation board for the CLC114 is available. This board may be ordered as part #730023.

Unused Buffers

It is recommended that the inputs of any unused buffers be tied to ground through 50Ω resistors.

Differential Gain and Phase

The CLC114 was designed to minimize differential gain and phase errors when driving the distributed capacitance of a video crosspoint switch. Refer to the section "Performance Driving a Crosspoint Switch" for typical values.

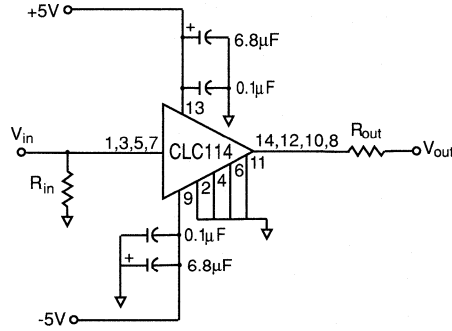


Figure 1: Recommended Circuit

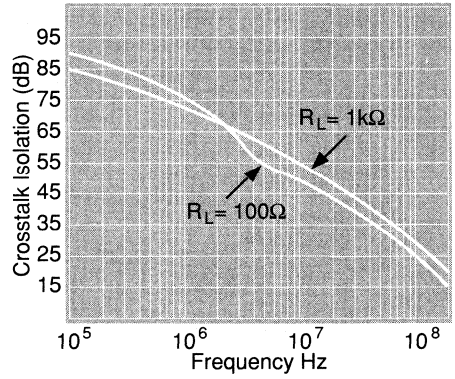


Figure 2: All-Hostile Crosstalk Isolation

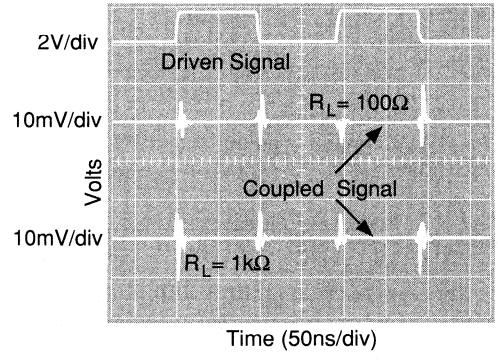


Figure 3: Most Susceptible Channel-to-Channel Pulse Coupling

Comlinear Corporation

Quad, Closed-Loop Monolithic Buffer

CLC115

APPLICATIONS:
- multi-channel video distribution
- video switching buffers
- high-speed analog multiplexing
- channelized EW
- high-density buffering
- instrumentation amps
- active filters

FEATURES (typical):
- closed-loop quad buffer
- 700MHz small-signal bandwidth
- 2700V/µs slew rate
- 0.08%/0.04° differential gain/phase
- 60dB channel isolation (10MHz)
- – 62dBc 2nd and 3rd harmonics at 20MHz
- 60mA current output per channel

DESCRIPTION:

The CLC115 is a high performance, closed-loop, quad buffer designed for high density applications requiring a low-cost-per-channel solution to buffering high-frequency signals. The CLC115's high performance includes a 700MHz small signal bandwidth (0.5Vpp) and a 2700V/µs slew rate while requiring only 11mA quiescent current per channel. Signal fidelity is maintained with low harmonic distortion (– 62dBc 2nd and 3rd harmonics at 20MHz), and wide channel separation (60dB crosstalk at 10MHz).

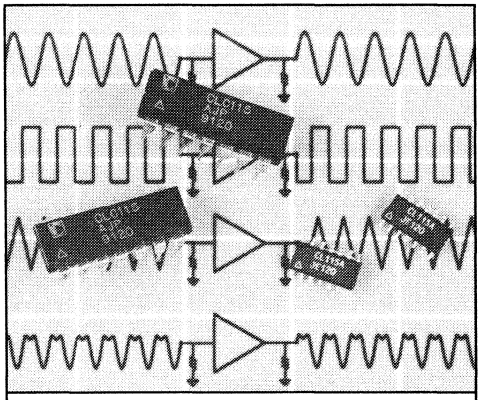
Featuring a unique closed-loop design, the CLC115 offers true unity-gain stability and very low output impedance plus a 60mA per channel output drive capability. The CLC115 is ideally suited for buffering video signals with its 0.08%/0.04° differential gain and phase performance at 3.58MHz. Applications such as analog multiplexing and high-speed A/D converters will benefit from the CLC115's high signal fidelity.

The CLC115 offers a low-cost-per-channel solution to high-speed buffering with four high-performance, closed-loop buffers integrated in one 14-pin package.

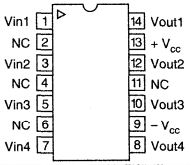
Constructed using an advanced, complimentary bipolar process and Comlinear's proven current feedback architectures, the CLC115 is available in several versions to meet a variety of requirements.

CLC115AJP	– 40°C to + 85°C	14-pin plastic DIP
CLC115AJE	– 40°C to + 85°C	14-pin plastic SOIC
CLC115AID	– 40°C to + 85°C	14-pin side-brazed ceramic DIP
CLC115A8D	– 55°C to + 125°C	14-pin side-brazed ceramic DIP, MIL-STD-883, Level B
CLC115ALC	– 55°C to + 125°C	dice
CLC115AMC	– 55°C to + 125°C	dice qualified to Method 5008, MIL-STD-883, Level B

Contact factory for other packages and DESC SMD number.

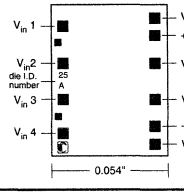


Pinout



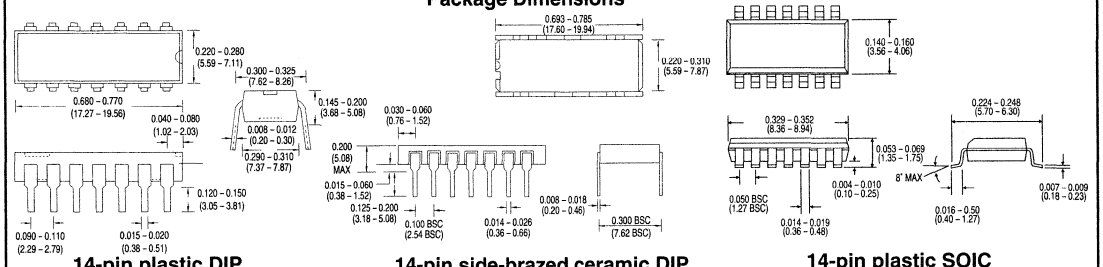
DIP and SOIC versions

Chip Topography



Height is 0.014 inches.
NOTE: Backside connected to – V_{cc}. It is not necessary to electrically connect the backside to the minus supply. Contact Comliner for complete die information.

Package Dimensions



Electrical Characteristics (V_{cc} = ±5V; R_L = 100Ω)

PARAMETERS	CONDITIONS	TYP	MAX AND MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC115AJ/AI	+ 25°C	– 40°C	+ 25°C	+ 85°C		
Ambient Temperature	CLC115A8/AM/AL	+ 25°C	– 55°C	+ 25°C	+ 125°C		
FREQUENCY DOMAIN RESPONSE							
– 3dB bandwidth	V_{out} < 0.5V_{pp}	700	400	400	300	MHz	SSBW
	V_{out} < 4V_{pp}	270	200	200	150	MHz	LSBW
gain flatness	V_{out} < 0.5V_{pp}						
flatness	DC to 30MHz[1]	± 0.0	± 0.1	± 0.1	± 0.1	dB	GFL
† peaking	30MHz to 200MHz	0.4	1.4	1.0	1.0	dB	GFPH
† rolloff	30MHz to 200MHz	0.0	0.5	0.5	0.5	dB	GFRH
differential gain	4.43MHz, 150Ω load	0.08	0.25	0.15	0.15	%	DG
differential phase	4.43MHz, 150Ω load	0.04	0.08	0.08	0.08	°	DP
crosstalk (all hostile)	10MHz	60	57	57	57	dB	XT
TIME DOMAIN RESPONSE							
rise and fall time	4V step	1.4	2.0	2.0	2.4	ns	TRS
settling time to 0.1%	2V step	12	17	17	17	ns	TS
overshoot	4V step input t_{rise} < 4ns	5	15	12	12	%	OS1
	input t_{rise} > 4ns	0	2	2	2	%	OS2
slew rate		2700	2200	2200	1800	V/µs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	2V_{pp}, 20MHz	– 62	– 45	– 47	– 47	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 20MHz	– 62	– 53	– 53	– 50	dBc	HD3
equivalent noise input							
noise floor	>1MHz	– 157	– 155	– 155	– 154	dBm_{1Hz}	SNF
STATIC DC PERFORMANCE							
small signal gain	no load	0.995	0.97	0.99	0.99	V/V	GA
integral endpoint linearity	± 2V, full scale	0.2	1.4	0.5	0.5	%	ILIN
*output offset voltage		± 2	± 17	± 9	± 9	mV	VIO
average temperature coefficient		± 25	± 100	–	± 50	µV/°C	DVIO
*input bias current		± 8	± 35	± 20	± 20	µA	IBN
average temperature coefficient		± 66	± 187	—	± 125	nA/°C	DIBN
†power supply rejection ratio		54	46	48	46	dB	PSRR
*supply current	total, no load	45	61	61	61	mA	ICC
MISCELLANEOUS PERFORMANCE							
input resistance		750	100	450	450	kΩ	RIN
input capacitance		1.6	2.2	2.2	2.2	pF	CIN
output resistance	DC	1.1	4.5	2.0	2.0	Ω	RO
output voltage range	no load	± 4.0	± 3.8	± 3.9	± 3.9	V	VO
output voltage range	R_L = 100Ω	± 3.7	± 2.2	± 3.4	± 3.0	V	VOL
output current		± 60	± 25	± 48	± 30	mA	IO

Absolute Maximum Ratings

V_{cc}	± 7V
I_{out} output is short circuit protected to ground, however, maximum reliability is obtained if I_{out} does not exceed...	96mA
input voltage	± V_{cc}
maximum junction temperature	+ 175°C
operating temperature range	
AJ/AI:	– 40°C to + 85°C
A8/AM/AL	– 55°C to + 125°C
storage temperature range	– 65°C to + 150°C
lead temperature (soldering 10 sec)	+ 300°C

Miscellaneous Ratings

NOTES:

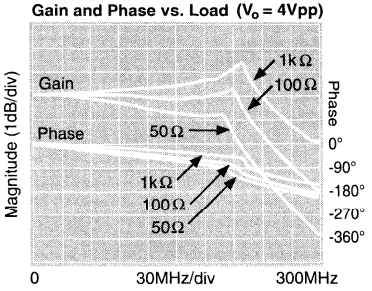
*	AI, AJ	100% tested at + 25°C, sample at + 85°C.
†	AJ	Sample tested at + 25°C.
†	AI	100% tested at + 25°C.
*	A8	100% tested at + 25°C, – 55°C, + 125°C.
†	A8	100% tested at + 25°C, sample at – 55°C, + 125°C.
*	AL, AM	100% wafer probed at + 25°C to + 25°C specifications.

note 1: Specification is guaranteed for (50Ω ≤ R_L ≤ 200Ω).

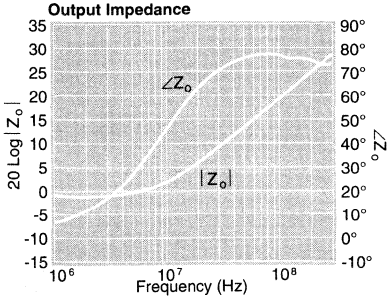
Comlinear reserves the right to change specifications without notice.

Typical Performance Characteristics (T_A = +25° C, V_{CC} = ±5V, R_L = 100Ω)

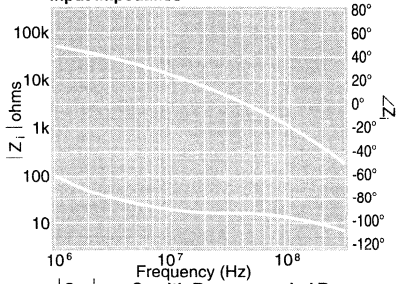
Gain and Phase vs. Load (V_o = 4Vpp)



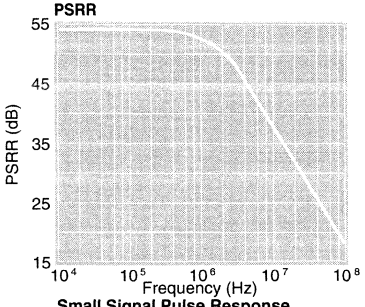
Output Impedance



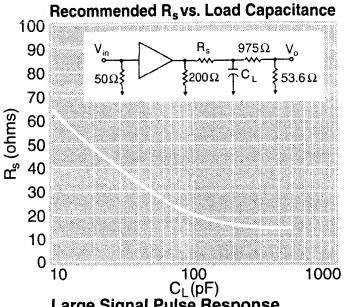
Input Impedance



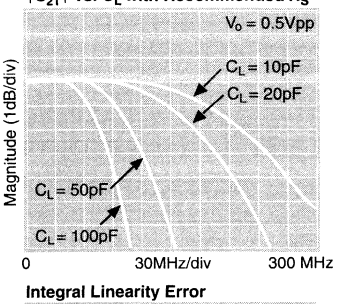
PSRR



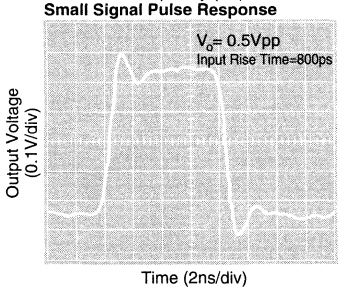
Recommended R_s vs. Load Capacitance



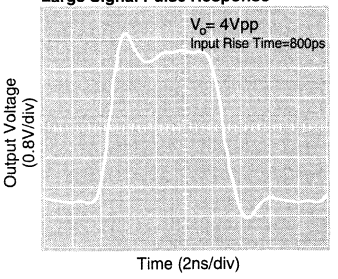
$|S_{21}|$ vs. C_L with Recommended R_S



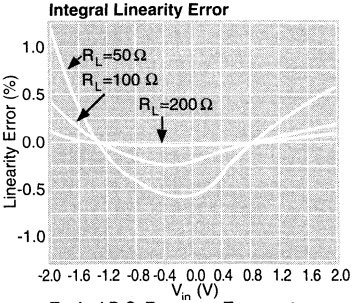
Small Signal Pulse Response



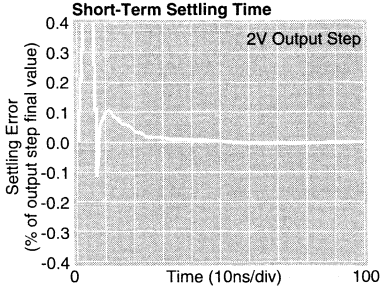
Large Signal Pulse Response



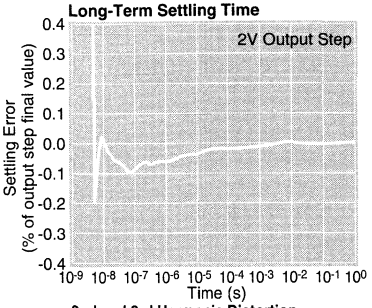
Integral Linearity Error



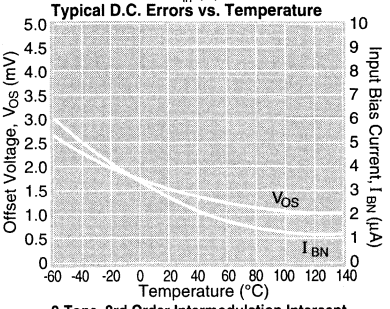
Short-Term Settling Time



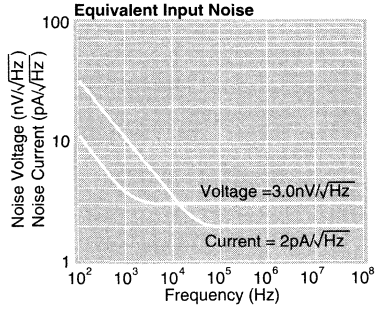
Long-Term Settling Time



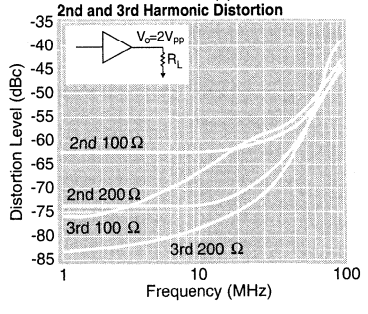
Typical D.C. Errors vs. Temperature



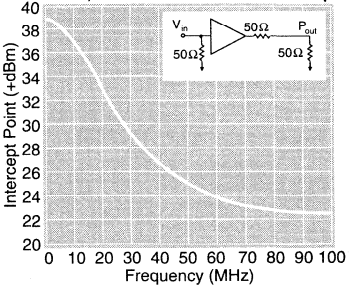
Equivalent Input Noise



2nd and 3rd Harmonic Distortion



2-Tone, 3rd Order Intermodulation Intercept



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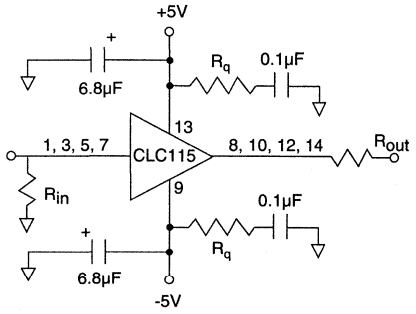


Figure 1: recommended circuit

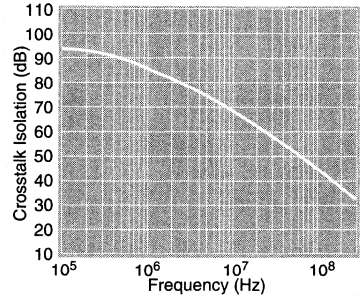


Figure 3: all-hostile crosstalk isolation

PC Board Layout and Circuit Design

For optimum performance, high frequency devices demand a good printed circuit board layout. A ground plane and power supply bypassing with good high-frequency ceramic capacitors in close proximity to the supply pins is essential. Second harmonic distortion can be improved by ensuring equal current return paths for both the positive and negative supplies.

The dominant pole, i.e. the high-frequency compensation of the CLC115, is set by the load resistance, R_L. Ideally, each buffer of the CLC115 should see a 100Ω load at high frequency to ensure stability. An unterminated channel is undercompensated and will exhibit gain at several hundred megahertz. Signal coupling may occur between channels through the common power supply connections. Any resonance in the power supply can lead to oscillations in the unterminated or undercompensated channel.

In order to compensate and to guarantee the stability of the four CLC115 channels, each must be terminated with a 100Ω resistance to ground. If a dc load is not desired, a two picofarad capacitor can be inserted between the 100Ω load resistor and ground, as shown in Figure 2.

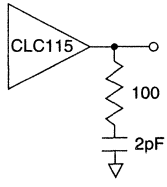


Figure 2: AC load

If the above load conditions are not feasible for your design, the power supply resonance must be addressed. Chip capacitors have less parasitic inductance than leaded ceramic capacitors. The use of 0.1µF chip capacitors mounted immediately adjacent to the power supply pins eliminates the resonance which can lead to oscillations. If chip capacitors are not used, then the only other means to eliminate the possibility of oscillation caused by power supply resonance is to 'de-Q' the resonant structure. 'De-Q'ing is particularly necessary while using leaded capacitors and can be achieved by inserting a 10Ω resistor, R_q, in series with the 0.1µF bypass capacitor, as shown in Figure 1. The insertion of the 'de-Q'ing resistor will reduce frequency response peaking as well as the tendency toward oscillation when driving a load resistance greater than 100Ω, but will increase harmonic distortion by approximately 2dB.

Crosstalk is strongly dependent on board layout. Closely spaced signal traces on the circuit board will degrade crosstalk due to intertrace capacitance. It is recommended that unused package pins (2,4,6,11) be connected to the ground plane for better isolation at the device pins. Similarly, crosstalk can be improved by using a grounded guard-trace between signal lines. This will reduce the distributed capacitance between signal lines.

Two graphs show the effects of crosstalk. All-hostile crosstalk is measured by driving three of the four buffers simultaneously while observing the fourth, undriven channel. Figure 3, "All-Hostile Crosstalk Isolation", shows this effect as a function of input signal frequency. The load for all four channels of the CLC115 is 100Ω. Figure 4, "Most Susceptible Channel-to-Channel Pulse Coupling", describes one effect of crosstalk when one channel is driven with a $4V_{pp}$ step (tr=5ns) while the output of the undriven channel is measured. From Figure 3 it can be seen that crosstalk improves as the signal frequency is reduced. Similarly, the pulse coupling crosstalk will improve as the time increases.

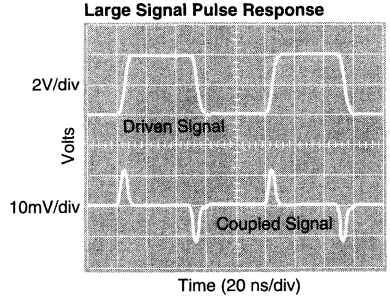


Figure 4: most susceptible channel-to-channel pulse coupling

Unused Buffers

The output of any unused buffers must be terminated in 100Ω to ground, as discussed above. It is recommended that unused buffer inputs be terminated in 50Ω to ground.

Evaluation Board

An evaluation board for the CLC115 is available. This board may be ordered as part #730023.

Modular/Encased Amplifiers

Contents

Comlinear Corporation

DC to 500MHz Linear Amplifier

CLC100

APPLICATIONS:

- pulse amplifiers
- baseband and video communications
- photodiode - photomultiplier preamps

FEATURES:

- extremely flat gain and linear phase response
- low distortion and excellent pulse fidelity
- instant recovery from overload signal levels

electrical characteristics V_{cc} ±5 to ±15, $R_L = R_S = 50$ Ohms, $T_A = 25°C$

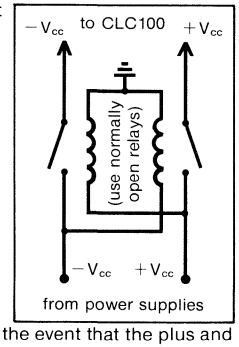
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
−3dB Bandwidth		475	500		MHz
Gain (non-inverting)	DC to 300MHz		20		dB
Gain Flatness	DC to 300MHz		0 ± .05	0 ± .15	dB
Group Delay	DC to 500MHz		1.4 ± .07		ns
Third Order Intermodulation Intercept (two tone)	1Hz to 100MHz 100 to 500 MHz	28 20	30		dBm dBm
Second Harmonic Distortion Third Harmonic Distortion	0dBm out, 1Hz to 500MHz		−60 −60	−50 −50	dBc dBc
Input and Output Impedance	see Note 1		50		ohms
Power Output	at −1dB gain compression	12			dBm
Equivalent Input Noise Noise Figure Dynamic Range	10Hz to 500MHz Bandwidth		20 6 72		uV dB dB
Rise and Fall Times	10 to 90%, 2V step		600	750	ps
Overshoot and Aberrations	duration not to exceed 2ns			10	%
Settling Time	to .4%, 2V step (Note 2)			5	ns
Overload Recovery Time	V_{in} peak = ±.5V		2		ns
DC Offset	input or output (adjustable)		±5		mV
Output Voltage Temp. Coeff. (Referenced to input)			20		uV/°C
Current Consumption			40		mA

Note 1: Input impedance is dependent upon load impedance and output impedance is dependent upon source impedance. If the external termination impedance at one port varies up or down, the amplifier impedance at the opposite port will likewise change up or down. For example, with $R_S = 50$ and $R_L \infty$, $R_{in} = 100$ and $R_{out} = 50$. With $R_S = R_L = 75$, $R_{in} = R_{out} = 65$ approximately. Gain flatness and other specifications are typically the same in a 75 ohm system as they are in a 50 ohm system.

Note 2: Thermally induced drift will cause post settling drift of 2mV after 200us and 10mV after several seconds.

maximum ratings

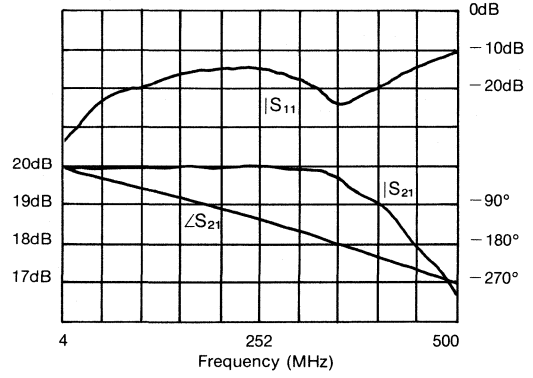
CAUTION: The positive and negative power supplies should come on and go off within one second of each other in order to prevent excessive power dissipation from damaging some internal components. If this requirement cannot be met, the following circuit should be used:



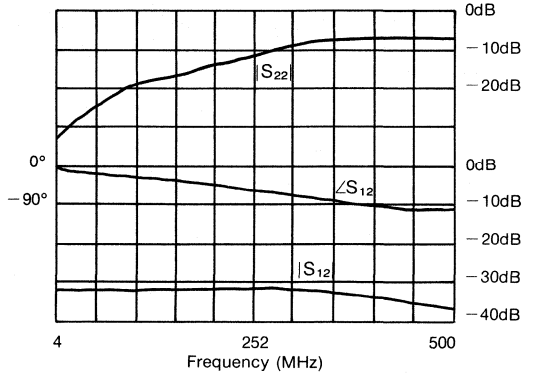
PARAMETER	CONDITION	RATING
V_{source} or V_{load}	Short to voltage source at input or output	±1.5V
I_{source}	Short to current source at input	±100mA
I_{load}	Short to current source at output	±20mA
$\pm V_{cc}$		16V
Operating Temperature Range		0°C to 70°C
Storage Temperature Range		−25°C to +85°C

Both $\pm V_{cc}$ supply voltage inputs are diode clamped to ground to prevent damage to the amplifier in the event that the plus and minus supplies are interchanged. The supply current should be limited to 1 amp maximum in the event.

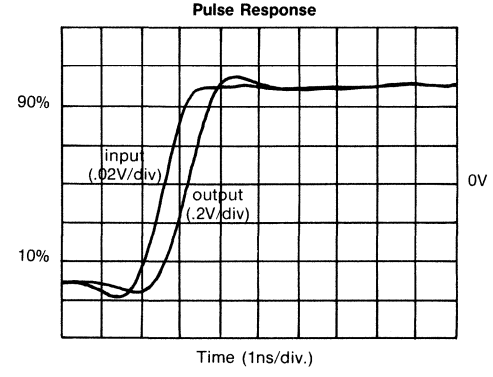
Forward Gain [S_{21}] and Input Return Loss [S_{11}]



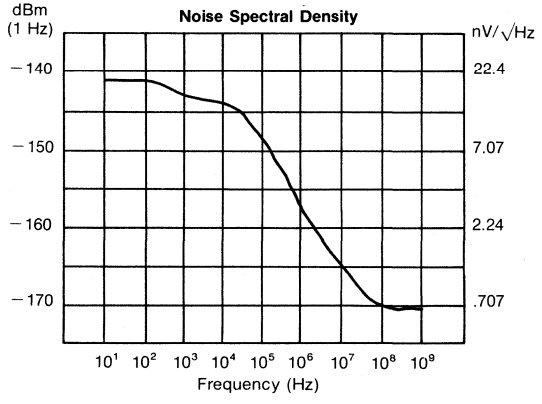
Reverse Isolation [S_{12}] and Output Return Loss [S_{22}]

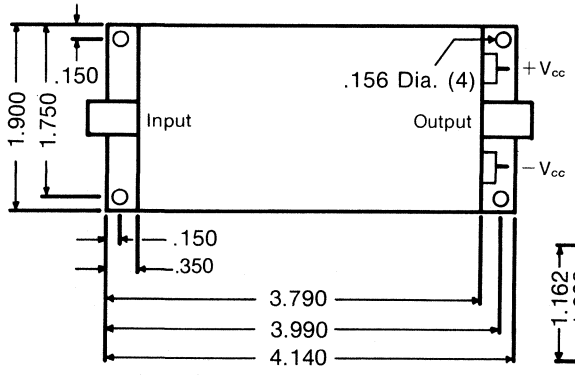


Pulse Response



Noise Spectral Density

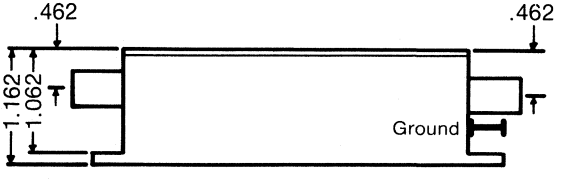




Case Dimensions (in inches)

Mass: 170 grams

BNC connectors are standard
SMA connectors are available



U.S. Patent 4,358,739, 4502020

Comlinear Corporation

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Comlinear Corporation

DC to 250MHz, Linear High Power Amplifier

CLC102

APPLICATIONS:

- coaxial cable line driver
- baseband and video communications
- pulse amplifiers

FEATURES:

- drives up to $12V_{pp}$ into 50 ohm loads
- very low distortion, low offset drift, and low overshoot
- extremely linear phase and wide dynamic range

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gain (inverting)	DC to 100MHz, $P_O \leq 24dBm$		15		dB
−3dB Bandwidth	$18dBm \leq P_O \leq 24dBm$ $P_O < 18dBm$	200	220 275		MHz MHz
Input and Output Impedance	see Note 2		50		ohms
Group Delay	DC to 200MHz		2.3 ± .08		ns
−1dB Gain Compression	at 100MHz		26		dBm
Rise and Fall Times	10% to 90%, 10V step		1.6	1.75	ns
Overshoot Aberrations	duration not to exceed 10 ns		2%	5%	
Settling Time	to .4%, 10V step		150		ns
Slew Rate			5000		V/us
Third Order Intermodulation Intercept (two tone)	at 20MHz at 100MHz		43 36		dBm dBm
Second/Third Order Harmonic Distortion	$P_O = 24dBm$, $R_L = 50$, at 10KHz at 20MHz at 100MHz $V_O = 20V_{pp}$, $R_L = \infty$, 10KHz		64/64 52/40 39/29 66/66		−dBc −dBc −dBc −dBc
Equivalent Input Noise Noise Figure Dynamic Range	10Hz to 300 MHz Bandwidth at 100MHz		46 15.5 85		uV dB dB
DC Offset Voltage	Input Output		<8 <30		mV mV
Output Voltage Temperature Coefficient (Referenced to Input)	Over 0°C to 70°C		15		uV/°C
Supply Current			140		mA

Note 1: All parameters measured at $T_A = 25°C$ with $R_L = R_S = 50\Omega$, using ±15V supplies. Min/max parameters guaranteed over the operating temperature range.

absolute maximum ratings

Voltage at input: ±2V peak

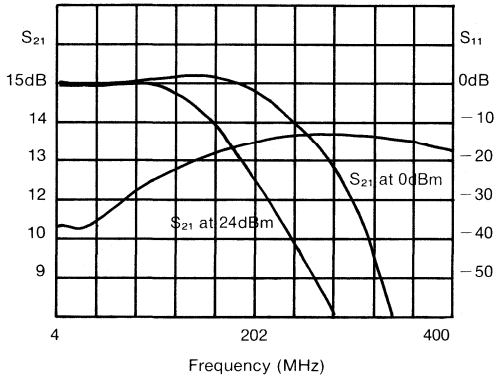
Storage Temperature: −25°C to +85°C

Operating Temperature: 0°C to 70°C

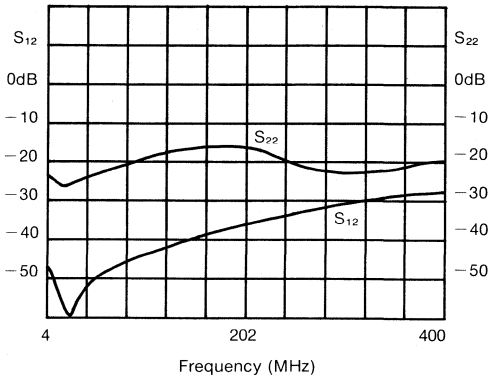
Supply Voltage: ±16V

Output will withstand short circuit to 0V indefinitely.

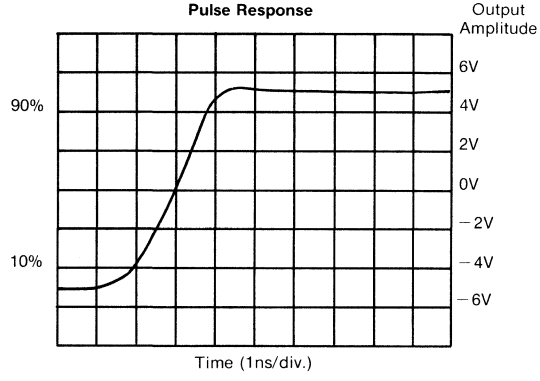
Forward Gain [S_{21}] and Input Return Loss [S_{11}]



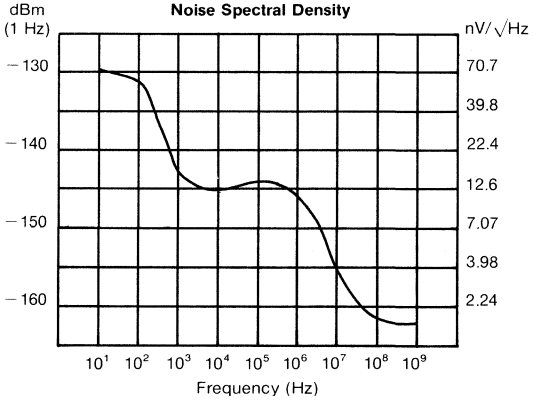
Reverse Isolation [S_{12}] and Output Return Loss [S_{22}]

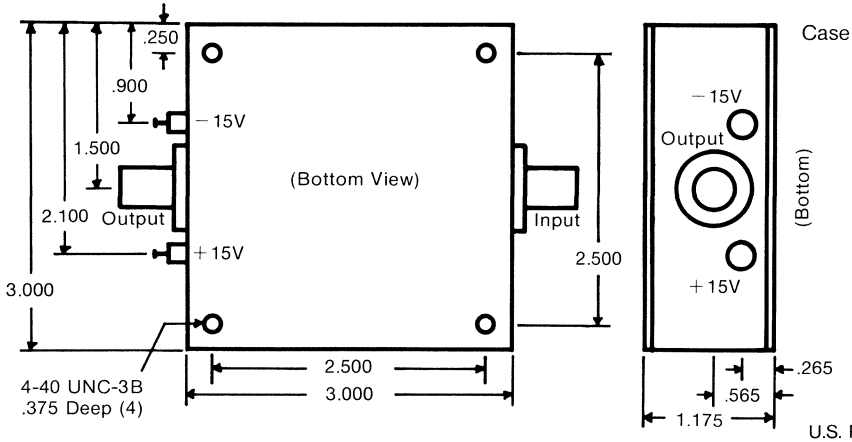


Pulse Response



Noise Spectral Density





Case Dimensions (in inches)

Connector Options
CLC 102-BNC
CLC 102-SMA

Mass: 245 grams

U.S. Patent 4,358,739, 4502020

Comlinear Corporation

Comlinear Corporation

Modular Series Amplifiers

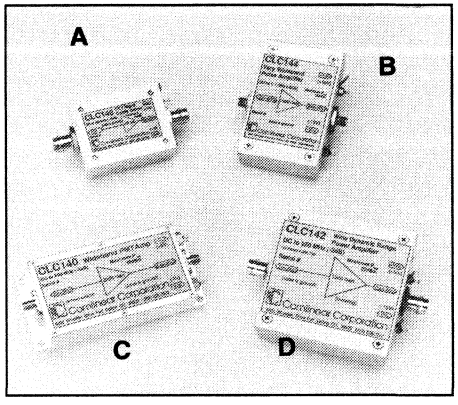
Modular Series

Applications:
- IF/HF tranceivers
- PMT amplifiers
- coax cable drivers
- signal generator post amps
- general purpose bench-top amps
- video distribution amps

Features:
- true DC-coupling
- 160MHz to 1.1GHz bandwidths
- fixed or flexible gain & I/O impedance
- BNC or SMA female connectors
- 10dBm to 27dBm max. power outputs
- −25°C to +85°C operating range

Description:
Comlinear's Modular Series of amplifiers builds on an extensive line of high performance, DC-coupled amplifiers to offer off-the-shelf application specific products. Designed for bench-top or system use, the Modular Series contains a mix of flexible definition and fixed definition amplifiers that provide a broad selection of features.

The fixed definition amplifiers have been optimized for specific applications such as PMT amps and wide dynamic range IF amplifiers, while the flexible definition amplifiers allow a choice of gain and I/O impedances. Packaged in the case styles shown here, these wideband linear amplifiers come ready to use with the addition of bipolar DC power supplies.



Package Dimensions: (Length × Width × Height)

Type A:	2.25"	X	1.75"	X	0.9"
Type B:	2.0"	X	3.0"	X	1.0"
Type C:	4.14"	X	1.9"	X	0.925"
Type D:	3.0"	X	3.0"	X	1.175"

Modular Series Fixed Gain Amplifiers
Tuned for optimum performance for a variety of applications, these amplifiers are nominally specified for ±15V power supplies and intended for use in 50Ω matched impedance systems, although some offer optional 75Ω input and/or output impedances. Ordering information requires the identification of one or more of these parameters: either BNC or SMA connector type, input impedance (Z_i) and/or output impedance (Z_o).

CLC140: Wide Band PMT Amp
Offers excellent high speed pulse response and low noise required of Photo-Multiplier Tube applications.
- DC to 500MHz bandwidth (P_o = 10dBm)
- 0.1dB flatness thru 300MHz
- fixed 20dB non-inverting gain (+10V/V)
- 600ps rise time
- excellent 50Ω I/O VSWR
- low 6dB noise figure
- ±5V to ±15V power supplies
- package type C
- Ordering Information: CLC140-SMA (no BNC)

CLC142: Wide Dynamic Range Power Amp
Combines excellent distortion performance with wide full-power bandwidth.
- DC to 250MHz bandwidth (18dBm)
- fixed 15dB inverting gain (−5.62V/V)
- 50dBm 3rd order intercept (10MHz)
- excellent 50Ω I/O VSWR
- 5000V/μs slew rate
- output short circuit protected
- 27dBm maximum output power
- package type D
- Ordering Information: CLC142-(SMA/BNC)

CLC143: High Fidelity Pulse Amp
Offers very low overshoot large signal pulse response with excellent pulse edge rates.
- 0% overshoot with 5V step (2% max.)
- 5000 V/μs slew rate
- 1.8ns rise and fall time 5V step
- DC to 220MHz bandwidth (18dBm)
- fixed 15dB inverting gain (−5.62V/V)
- 50Ω I/O impedance
- package type D
- Ordering Information: CLC143-(SMA/BNC)

CLC144: Very Wideband Pulse Amp
Offers the widest band DC-coupled pulse amplifier available from Comlinear.
- DC to 1.1GHz bandwidth (P_o = 12dBm)
- fixed 14dB non-inverting gain (+5V/V)
- <400ps rise times
- 1.2ns overdrive recovery
- excellent phase linearity (1.5° to 750MHz)
- excellent 50Ω I/O VSWR
- package type B
- Ordering Information: CLC144-SMA (no BNC)

CLC146: FET Input Cable Driver
Offers a high input impedance, very low bias current, buffer, with either 50 or 75Ω output impedance, achieving unity gain when driving a matched load.
- DC to 220MHz bandwidth (P_o = 10dBm)
- fixed 0dB gain into matched load
- low distortion
- low input noise
- excellent 50Ω or 75Ω output VSWR
- package style A
- Ordering Information: CLC146-(SMA/BNC)-Z_o

Modular Series Flexible Definition Amplifiers
Intended to satisfy user specific applications, these parts offer a broad range of non-inverting gains and I/O impedances with each part emphasizing a particular performance parameter. Overall, these parts cover the +2 to +40 (unterminated output) gain range with 50Ω to 1kΩ I/O impedances. All are intended for ±15V power supplies. Ordering information requires the identification of connector type: either BNC or SMA, input impedance (Z_i), output impedance (Z_o) and the voltage gain (A_v) with an unterminated output. The actual voltage gain to a resistive load, Z_L, will be $A_v \cdot (Z_L/(Z_o+Z_L))$.

CLC160: High Power Driver Amp
Offers the highest load power for ±15V supplies with output impedance matching capability.
- DC to 160MHz bandwidth (A_v = 10, P_{out} = 18dBm)
- maximum P_{out} = 24dBm
- gain range (A_v): +5 to +20
- input impedance (Z_i): 50Ω to 1kΩ
- output impedance (Z_o): 50Ω to 200Ω
- output short circuit protected
- package type A
- Ordering information: CLC160-(SMA/BNC)-Z_i-Z_o-A_v

CLC162: Low Distortion, Low Gain Amplifier
Very low harmonic distortion for low gain applications.
- DC to 220MHz bandwidth (A_v = 2, V_o = $2V_{pp}$)
- <−64dBc harmonics ($1V_{pp}$, 20MHz, Z_o = Z_L = 50Ω)
- gain range (A_v): +2 to +5
- input impedance (Z_i): 50Ω to 1kΩ
- output impedance (Z_o): 50Ω to 1kΩ
- package type B
- Ordering information: CLC162-(SMA/BNC)-Z_i-Z_o-A_v

CLC163: Low Distortion, High Gain Amplifier
Very low harmonic distortion for higher gain applications.
- DC to 125MHz bandwidth (A_v = 20, V_o = $2V_{pp}$)
- <−70dBc harmonics ($1V_{pp}$, 20MHz, Z_o = Z_L = 50Ω)
- gain range (A_v): +5 to +40
- input impedance (Z_i): 50Ω to 1kΩ
- output impedance (Z_o): 50Ω to 1kΩ
- output short circuit protected
- package type A
- Ordering information: CLC163-(SMA/BNC)-Z_i-Z_o-A_v

CLC166: Low DC Offset, Wideband Amplifier
A general purpose wideband amplifier with lower input offset voltage.
- DC to 150MHz bandwidth (A_v = 20, V_o = $2V_{pp}$)
- less than ±2mV input offset voltage (typ)
- gain range (A_v): +10 to +40
- input impedance (Z_i): 50Ω to 200Ω
- output impedance (Z_o): 50Ω to 1kΩ
- package type B
- Ordering information: CLC166-(SMA/BNC)-Z_i-Z_o-A_v

CLC167: Low DC Offset, High Power Output Amplifier
A wide full power bandwidth amplifier with low input offset voltage.
- DC to 150MHz bandwidth (A_v = 20, V_o = $4V_{pp}$)
- DC to 60MHz bandwidth (A_v = 20, V_o = $20V_{pp}$)
- less than ±2mV input offset voltage (typ)
- gain range (A_v): +10 to +40
- input impedance (Z_i): 50Ω to 200Ω
- output impedance (Z_o): 50Ω to 1kΩ
- package type B
- Ordering information: CLC167-(SMA/BNC)-Z_i-Z_o-A_v

Typical Specifications — Absolute Maximum Ratings – 25°C to + 85°C

Model	Gain (matched load) (dB)	bandwidth, P_{out} (MHz, dBm)	input impedance (Ω)	output impedance (Ω)	V_{out}, I_{out} (matched load) (V,mA)	power supply range (V)	output current (mA)	input voltage (V)
CLC140	20	500, 10	50	50	±1.25, ±15	±5 to ±16	±20	±0.5
CLC142	15 (inv.)	250, 18	50	50	±10, ±250	±12 to ±16	±250	±2
CLC143	15 (inv.)	220, 18	50	50	±10, ±250	±12 to ±16	±250	±2
CLC144	14	1100, 12	50	50	±1.5, ±35	±12 to ±16	±40	±0.5
CLC146	0	220, 10	FET	50 or 75	±5, ±100	±10 to ±16	±150	±V_{cc}

Model	Gain (open load) (V_o/V_i)	bandwidth, P_{out} (MHz, dBm)	input impedance (Ω)	output impedance (Ω)	V_{out}(open load) I_{out} (V,mA)	power supply range (V)	output current (mA)	input voltage (V)
CLC160	5 to 20	170, 18	50 to 1k	50 to 200	±10, ±200	±10 to ±16	±250	±V_{cc}
CLC162	2 to 5	250, 10	50 to 1k	50 to 1k	±10, ±100	±5 to ±16	±150	±6
CLC163	5 to 40	170, 10	50 to 1k	50 to 1k	±10, ±100	±5 to ±16	±150	note 1
CLC166	10 to 40	170, 10	50 to 200	50 to 1k	±10, ±50	±5 to ±16	±75	note 1
CLC167	10 to 40	150, 10	50 to 200	50 to 1k	±10, ±200	±10 to ±16	±200	note 1

note 1: The output must not be overdriven for these parts. Therefore the maximum ±V_{in} will be ±(|V_{cc}| −4V)/A_v

Comlinear Corporation

E Series Encased Amplifiers

E SERIES

DESCRIPTION:

Comlinear's E Series Amplifiers are designed to take full advantage of Comlinear's high-performance DC-coupled operational and video amplifiers in an easy-to-use, encased form. This format makes the E Series Amplifiers an excellent choice for use on the bench, in a test station, or in other environments needing both high performance and ease of use.

The op amp-based E Series amplifiers (shown in the table below) provide a wide selection of features as well as the ability to customize parameters such as voltage gain and output impedance to the application.

E200....general purpose (−3dB BW of 95MHz)
E201....general purpose (−3dB BW of 95MHz)
E220....high bandwidth (−3dB BW of 190MHz), lower output current (50mA)
E221....high bandwidth (−3dB BW of 170MHz), lower output current (50mA)
E103....high output current (200mA)
E203....high output current (200mA), better settling performance
E231....designed for low-gain applications ($A_V = \pm 1$ to ± 5)

The E104 is an encased version of the CLC104AI, a DC to 1.1GHz linear amplifier with a fixed gain of 14dB and 50Ω input and output impedances. These features, coupled with excellent distortion and VSWR characteristics, make the E104 ideal for applications in wideband analog and high-speed digital communications, radar, and fiber optics transmitters and receivers.

E104....DC to 1.1GHz, fixed 14dB gain, low distortion

Complete specifications for the E104 and the op amp-based amplifiers are shown on the next page.

ORDERING INFORMATION:

E104

Since gain and input and output impedances are fixed on the E104, simply designate the connector type required by: E104-BNC or E104-SMA.

E103, E200, E201, E203, E220, E221, and E231

Due to the flexibility possible with these amplifiers, the user must specify several parameters when ordering:

The full part number is Ennn-p-con-Z_i-Z_o-A_V
nnn: specify 103, 200, 201, 203, 220, 221, or 231
p: specify N (non-inverting) or I (inverting)
con: specify BNC or SMA connectors or NDC for no case
Z_i: specify input impedance in ohms
Z_o: specify output impedance in ohms
A_V: specify voltage gain with **output unterminated** (ie: $Z_{load} = \infty$) (see example)

Select Z_i, Z_o, and A_V within the following constraints:

parameter	103	200, 201	220, 221, 203	231
A_V	± 1 to ± 40	± 1 to ± 50	± 1 to ± 50	± 1 to ± 5
maximum Z_{in} inverting	$\frac{1500}{A_V}$	$\frac{2000}{A_V}$	$\frac{1500}{A_V}$	$\frac{250}{A_V}$
non-inverting	10k	10k	10k	10k
minimum Z_{out}	0	0	0	0

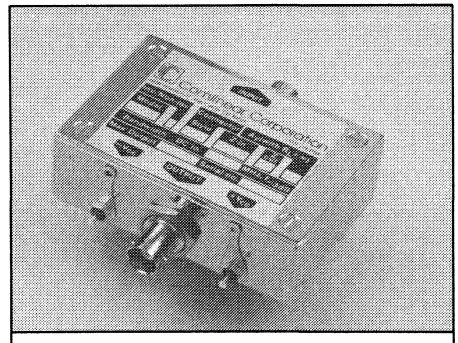
Example: E200-N-BNC-75-50-20 means an E200 with a non-inverting gain, BNC connectors, 75Ω input impedance, 50Ω output impedance, and a voltage gain of 20 volts/volt (unterminated output). (When driving a realistic load, the actual gain is reduced by the factor $Z_{load} / (Z_{load} + Z_o)$ due to the resistive divider action of the output impedance, Z_o, and the load connected to the amplifier, Z_{load}. The unterminated voltage gain, A_V, should be selected with this in mind.)

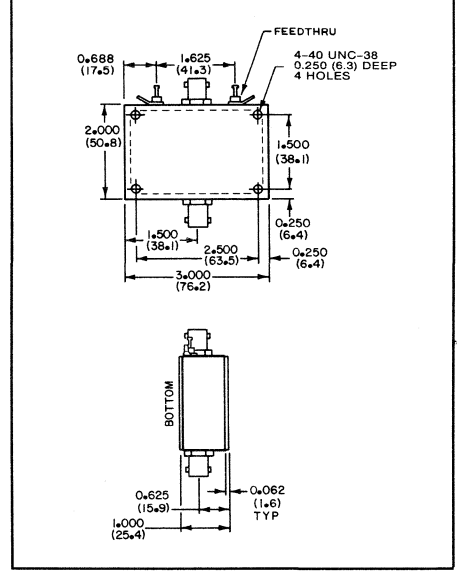
APPLICATIONS:

- for use on the bench or in a test station as a video amp, pulse amp, line driver, etc.
- "drop in" units for radar and communication systems
- simplifies evaluation of Comlinear amplifiers

FEATURES:

- wide bandwidth, fast settling, high slew rate
- low distortion and overshoot
- linear phase
- easy-to-use encased form





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Typical Specifications (note 1) Absolute Maximum Ratings

Model	−3dB bandwidth (MHz)	settling time (ns, %)	slew rate (V/μs)	V_{out}, I_{out} (V, mA) (note 2)	V_{cc} (V)	power dissipation (W@25°C)	derate above 25°C mW/°C	output current (mA)	input voltage (V)	$T_{operating}$ (°C)	$T_{storage}$ (°C)
general purpose											
E200	95	18, 0.1	4000	±12, ±100	5–17	1.8	10	100	note 3	−25 to +85	−65 to +150
E201	95	18, 0.1	4000	±12, ±100	5–17	1.8	10	100	note 3	−25 to +85	−65 to +150
wide bandwidth											
E220	190	8, 0.1	7000	±12, ±50	5–17	1.5	5	50	note 3	−25 to +85	−65 to +150
E221	170	15, 0.1	6500	±12, ±50	5–17	1.5	5	50	note 3	−25 to +85	−65 to +150
high output current											
E103	150	10, 0.4	6000	±11, ±200	9–17	2.0	10	200	note 3 & 4	−25 to +85	−65 to +150
E203	160	15, 0.2	6000	±11, ±200	9–17	2.0	10	200	note 3	−25 to +85	−65 to +150
low gain											
E231	165	12, 0.1	3000	±11, ±100	5–17	1.8	10	100	note 3	−25 to +85	−65 to +150
ultra-wide bandwidth											
E104	1100	1.2, 0.8	4500	±1.6, ±40	9–17	1.8	na	40	±0.5	−25 to +85	−65 to +150

note 1: nominal configuration
V_{cc}: ±15V E103, E104, E200, E201, E220, E221, E231 Load: 100Ω E103, E203, E231; 200Ω E200, E201, E220, E221; 50Ω E104 A_V: +20 E103, E200, E201, E203, E220, E221; +2 E231

note 2: When the amplifier is configured with an output impedance (Z_{out}) >0, the maximum output voltage swing (at the load) is reduced by the factor $Z_{load}/(Z_{load} + Z_{out})$. See the example on the previous page.

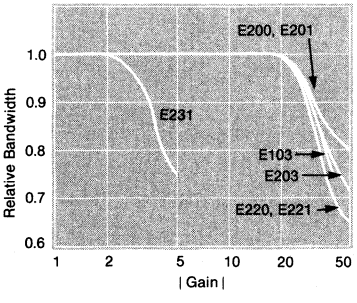
note 3: These amplifiers must be kept out of saturation; in other words, the output voltage (determined by V_{in} and A_v) must be kept away from the supply voltage $\left(|V_{in}| < \frac{|V_{cc}| - 2.5}{|A_v|}\right)$.

note 4: In the non-inverting configuration, the input voltage to the E103 must not exceed ±5V.

DISCUSSION:

The performance specified above is that typically seen for a nominally-configured E Series amplifier; performance for different configurations can be determined using the graphs below. Other parameters not shown can be approximated by referring to the individual hybrid data sheets.

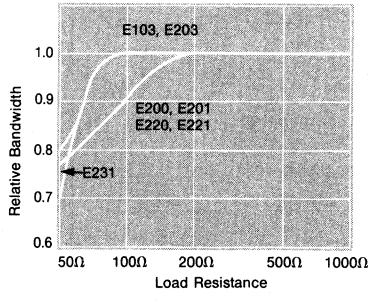
Relative Bandwidth vs. Gain



Relative Bandwidth vs. Gain

At the nominal gain setting of +20 (+2 for the E231), the amplifiers will typically provide 100% of the specified bandwidth; higher gains will reduce the bandwidth somewhat as shown above.

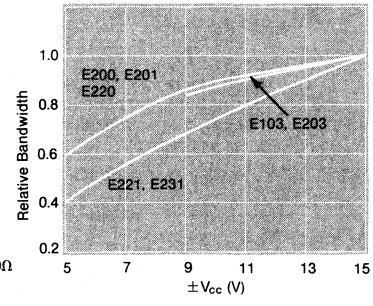
Relative Bandwidth vs. Load



Relative Bandwidth vs. Load

Listed under the typical specifications table are the nominal loads at which the amplifiers will typically provide 100% of the specified bandwidth. Heavier loads decrease the bandwidth as the plot above indicates. (The total load on the amplifier is the sum of the output impedance, Z_o, and the load connected external to the amplifier, Z_{load}).

Relative Bandwidth vs. V_{cc}



Relative Bandwidth vs. V_{cc}

All of the E Series amplifiers are designed to operate on ±15V supplies. The user may elect, however, to use lower supplies but at some sacrifice in performance as shown above.

Analog Multiplexers
Contents

Comlinear Corporation

High-Speed 2:1 Analog Multiplexer

CLC532

APPLICATIONS:

- infrared system multiplexing
- CCD sensor signals
- radar I/Q switching
- high definition video HDTV
- test and calibration

FEATURES (typical):

- 12-bit settling (0.01%) - 17ns
- low noise - 32µVrms (dc to 100MHz)
- high isolation - 80dB @ 10MHz
- low distortion - 80dBc @ 5MHz
- Adjustable noise bandwidth

DESCRIPTION:

The CLC532 is a high-speed 2:1 multiplexer with active input and output stages. The CLC532 also employs a closed-loop design which dramatically improves accuracy. This monolithic device is constructed using an advanced high-performance bipolar process.

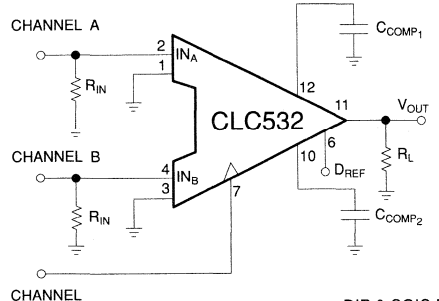
The CLC532 has been specifically designed to provide settling times of 17ns to 0.01%. This, coupled with the adjustable noise-bandwidth, makes the CLC532 an ideal choice for infrared and CCD imaging systems. Channel-to-channel isolation is better than 80dB @ 10MHz. Low distortion (80dBc) and spurious signal levels make the CLC532 a very suitable choice for both I/Q processors and receivers.

The CLC532 is offered over both the industrial and military temperature ranges. The Industrial versions, CLC532AJP\AJE\AID, are specified from -40°C to +85°C and are packaged in 14-pin plastic DIP's, 14-pin SOIC's and 14-pin Side-Brazed packages. The extended temperature versions, CLC532A8B/A8D/A8L-2, are specified from -55°C to +125°C and are packaged in a 14-pin hermetic DIP and 20-terminal LCC packages. (Contact factory for LCC and Cerdip availability.)

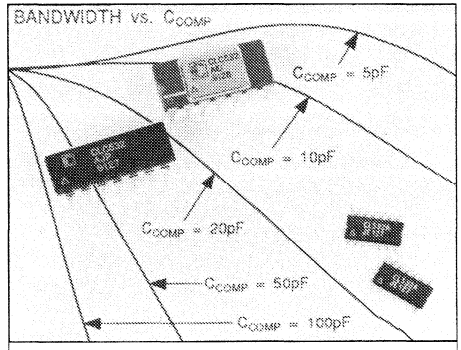
Ordering Information ...

CLC532AJP	-40°C to +85°C	14-pin plastic DIP
CLC532AJE	-40°C to +85°C	14-pin plastic SOIC
CLC532AIB	-40°C to +85°C	14-pin Cerdip
CLC532AID	-40°C to +85°C	14-pin Side-Brazed
CLC532A8B	-55°C to +125°C	14-pin Cerdip; MIL-STD-883
CLC532A8D	-55°C to +125°C	14-pin Side-Brazed; MIL-STD-883
CLC532A8L-2A	-55°C to +125°C	20-terminal LCC; MIL-STD-883

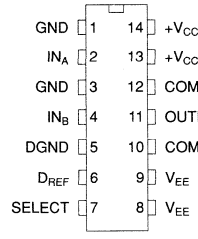
Functional Diagram



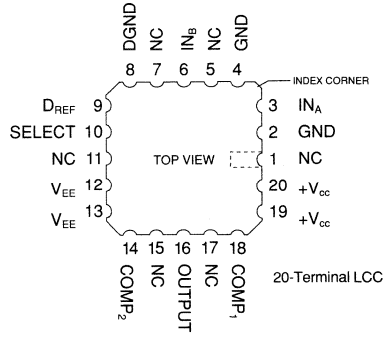
DIP & SOIC Pinout



Pinouts



14-Pin DIP and SOIC



20-Terminal LCC

Electrical Characteristics ($+V_{CC}$=+5.0V; $-V_{EE}$=-5.2V; R_M=50Ω; R_L=500Ω; C_{COMP}=10pF; ECL Mode, pin 6 = NC)

PARAMETER[1]	CONDITIONS	TYP	MAX & MIN RATINGS[2]			UNITS	SYMBOL
Case Temperature	CLC532A8B/A8D/A8L-2A	+25°C	-55°C	+25°C	+125°C		
Case Temperature	CLC532AJP/AJE/AIB/AID	+25°C	-40°C	+25°C	+85°C		
FREQUENCY DOMAIN PERFORMANCE							
† -3dB bandwidth	V_{OUT}<0.1Vpp	190	140	140	110	MHz	SSBW
-3dB bandwidth	V_{OUT}=2Vpp	45	35	35	30	MHz	LSBW
† gain flatness	V_{OUT}<0.1Vpp						
peaking	0.1MHz to 200MHz	0.2	0.7	0.7	0.8	dB	GFP
rolloff	0.1MHz to 100MHz	1.0	1.8	1.8	2.6	dB	GFR
linear phase deviation	dc to 100MHz	2.0				deg	LPD
differential gain	C_{COMP} = 5pF; R_L=150Ω	0.05				%	DG
differential phase	C_{COMP} = 5pF; R_L=150Ω	0.01				deg	DP
crosstalk rejection	2Vpp, 10MHz	80	75	75	74	dB	CT10
	2Vpp, 20MHz	74	69	69	68	dB	CT20
	2Vpp, 30MHz	68	63	63	62	dB	CT30
TIME DOMAIN PERFORMANCE							
rise and fall time	0.5V step	2.7	3.3	3.3	3.8	ns	TRS
	2V step	10	12.5	12.5	14.5	ns	TRL
settling time 2V step; from 50% V_{OUT}	±0.0025%	35				ns	TS14
	±0.01%	17	24	24	27	ns	TSP
	±0.1%	13	18	18	21	ns	TSS
overshoot	2.0V step	2	5	5	6	%	OS
slew rate		160	130	130	110	V/µs	SR
SWITCH PERFORMANCE							
channel to channel switching time	50% SELECT to 10%V_{OUT}	5	7	7	8	ns	SWT10
(2V step at output)	50% SELECT to 90%V_{OUT}	15	20	20	23	ns	SWT90
switching transient		30				mV	ST
DISTORTION AND NOISE PERFORMANCE							
† 2nd harmonic distortion	2Vpp, 5MHz	80	67	67	67	dBc	HD2
† 3rd harmonic distortion	2Vpp, 5MHz	86	68	68	68	dBc	HD3
equivalent input noise							
spot noise voltage	>1MHz	3.1				nV/√Hz	SNF
integrated noise	1MHz to 100MHz	32	42	42	46	µVrms	INV
spot noise current		3				pA/√Hz	SNC
STATIC AND DC PERFORMANCE							
* analog output offset voltage		1	6.5	3.5	5.5	mV	VOS
temperature coefficient		15	90		20	µV/°C	DVIO
analog output offset voltage matching		TBD				mV	VOSM
* analog input bias current		50	250	120	120	µA	IBN
temperature coefficient		0.3	2.0		0.8	µA/°C	DIBN
analog input bias current matching		TBD				µA	IBNM
analog input resistance		200	90	120	120	kΩ	RIN
analog input capacitance		2	3.0	2.5	2.5	pF	CIN
* gain accuracy	±2V	0.998	0.975	0.975	0.975	V/V	GA
gain matching	±2V	TBD				V/V	GAM
integral endpoint non-linearity	±1V (full scale)	0.02	0.05	0.03	0.03	%FS	ILIN
output voltage	no load	±3.4	2.4	2.8	2.8	V	VO
output current		45	20	30	30	mA	IO
output resistance	dc	1.5	4.0	2.5	2.5	Ω	RO
DIGITAL INPUT PERFORMANCE							
ECL mode (pin 6 floating)							
input voltage logic HIGH			-1.1	-1.1	-1.1	V	VIH1
input voltage logic LOW			-1.5	-1.5	-1.5	V	VIL1
input current logic HIGH		14	50	30	30	µA	IIH1
input current logic LOW		50	270	110	110	µA	IIL1
TTL mode (pin 6 = +5V)							
input voltage logic HIGH			2.0	2.0	2.0	V	VIH2
input voltage logic LOW			0.8	0.8	0.8	V	VIL2
input current logic HIGH		14	50	30	30	µA	IIH2
input current logic LOW		50	270	110	110	µA	IIL2
POWER REQUIREMENTS							
* supply current (+V_{CC} = +5.0V)	no load	23	30	28	25	mA	ICC
* supply current (-V_{EE} = -5.2V)	no load	24	31	30	26	mA	IEE
nominal power dissipation	no load	240				mW	PD
* power supply rejection ratio		73	60	64	64	dB	PSRR

Recommended Operating Conditions

positive supply voltage ($+V_{CC}$)	+5V
negative supply voltage ($-V_{EE}$)	-5.2V or -5.0V
differential voltage between any two GND's	10mV
analog input voltage range	±2V
SELECT input voltage range (TTL mode)	0.0V to +3.0V
SELECT input voltage range (ECL mode)	-2.0V to 0.0V
C_{COMP} range[2]	0pF to 100pF

thermal data	θ_{JC}(°C/W)	θ_{CA}(°C/W)
14-pin plastic		75
14-pin Cerdip	35	75
14-pin Side-Brazed		75
14-pin SOIC		100
20-terminal LCC		

Absolute Maximum Ratings[3]

positive supply voltage ($+V_{CC}$)	-0.5V to +7.0V
negative supply voltage ($-V_{EE}$)	+0.5V to -7.0V
differential voltage between any two GND's	200mV
analog input voltage range	$-V_{EE}$ to $+V_{CC}$
digital input voltage range	$-V_{EE}$ to $+V_{CC}$
output short circuit duration (output shorted to GND)	Infinite
junction temperature	+175°C
operating temperature range	
CLC532AJP/AJE/AIB/AID	-40°C to +85°C
CLC532A8B/A8D/A8L-2A	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec

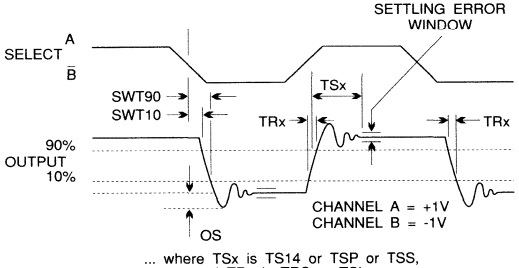
Note 1: Test levels are as follows:

*	AI, AJ	: 100% tested at +25°C, sample at +85°C.
†	AJ	: Sample tested at +25°C.
†	AI	: 100% tested at +25°C.
*	A8	: 100% tested at +25°C, -55°C, +125°C.
†	A8	: 100% tested at +25°C, sample at -55°C, +125°C

Note 2: The CLC532 does not require external C_{COMP} capacitors for proper operation.

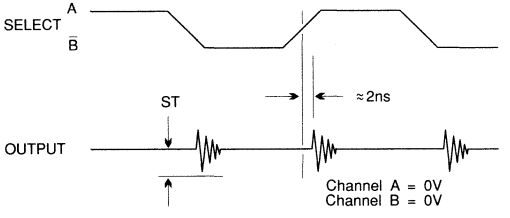
Note 3: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

System Timing Diagram

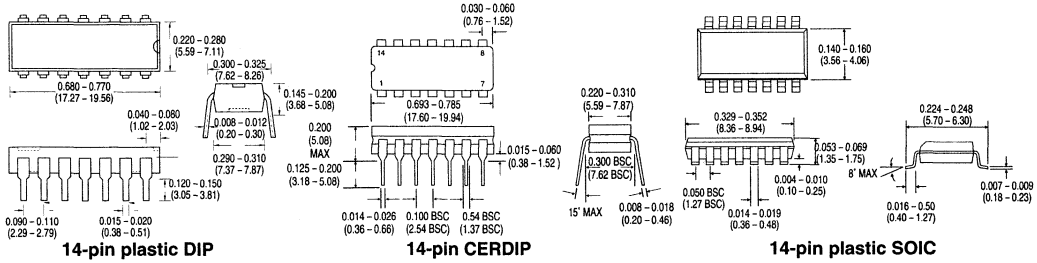


... where TSx is TS14 or TSP or TSS, and TRx is TRS ro TSL.

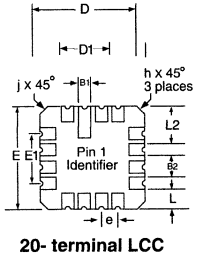
Switching Transient Timing Diagram



Package Dimensions



14-pin plastic DIP | **14-pin CERDIP** | **14-pin plastic SOIC**

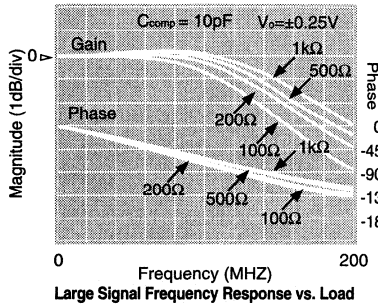


20- terminal LCC

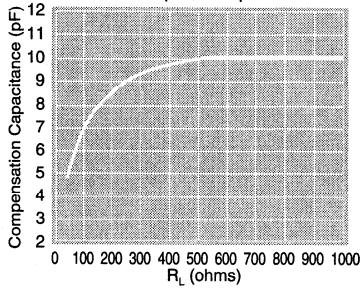
Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A1	0.050	0.088	1.27	2.23
B1	0.022	0.028	0.56	0.71
B2	0.072 REF		1.83 REF	
D,E	0.342	0.358	8.69	9.09
D1,E1	0.200 BSC		5.08 BSC	
e	0.050 BSC		1.27 BSC	
h	0.040 REF		1.02 REF	
j	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41

Typical Performance Characteristics (+25°C unless otherwise specified)

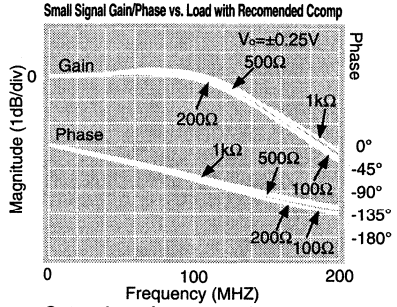
Small Signal Gain/Phase vs. Load



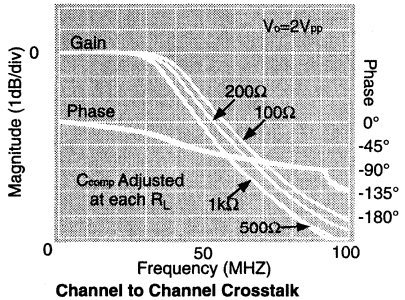
Recommended Compensation Capacitance vs. Load



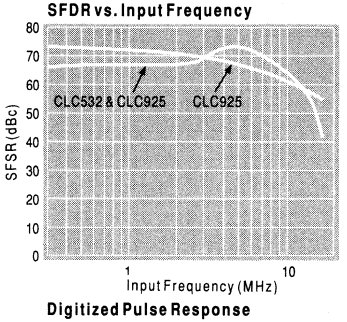
Small Signal Gain/Phase vs. Load with Recomended Ccomp



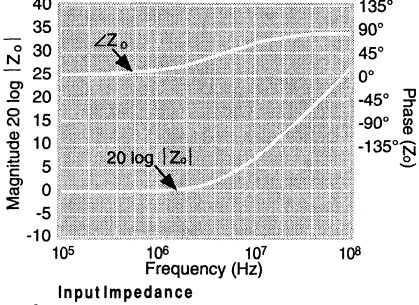
Large Signal Frequency Response vs. Load



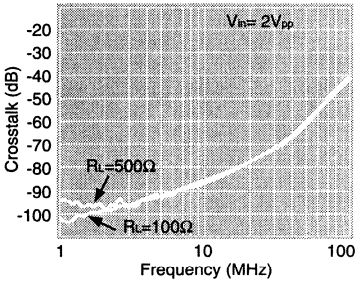
SFDR vs. Input Frequency



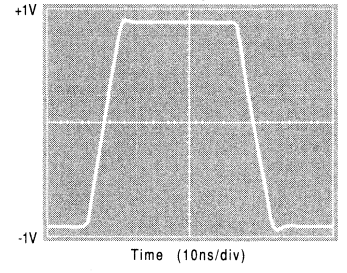
Output Impedence



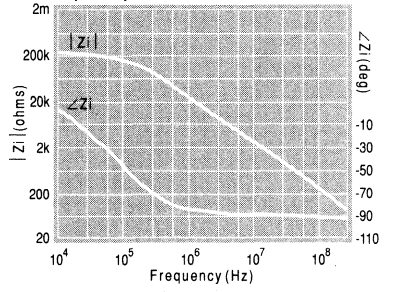
Channel to Channel Crosstalk



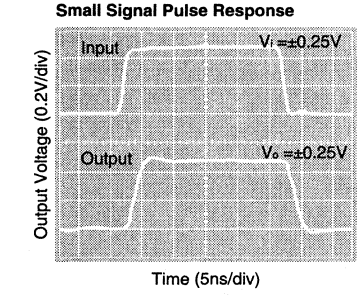
Digitized Pulse Response



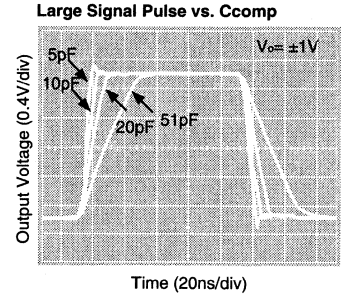
Input Impedance



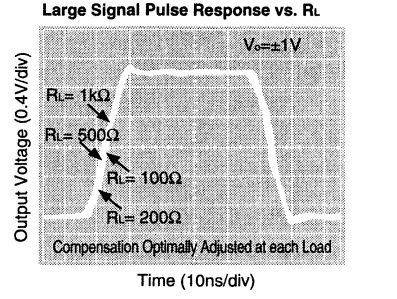
Small Signal Pulse Response



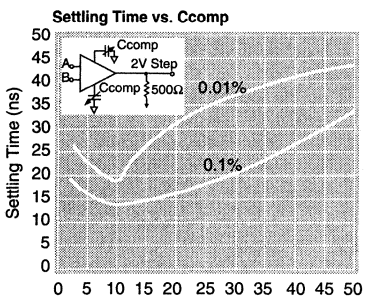
Large Signal Pulse vs. Ccomp



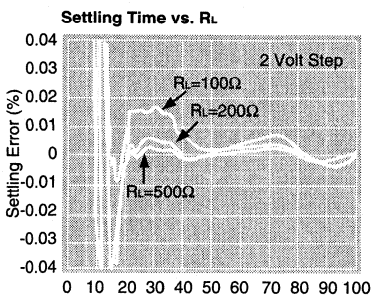
Large Signal Pulse Response vs. RL



Settling Time vs. Ccomp

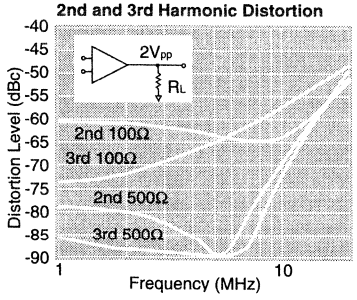


Settling Time vs. RL

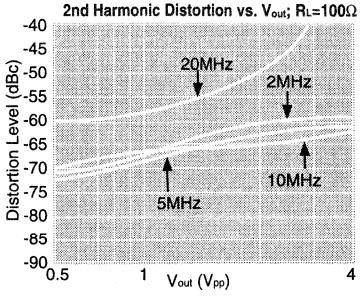


Typical Performance Characteristics (+25°C unless otherwise specified)

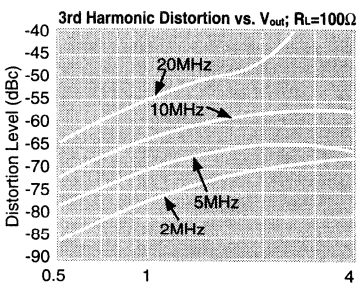
2nd and 3rd Harmonic Distortion



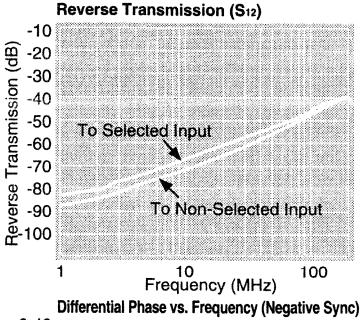
2nd Harmonic Distortion vs. V_{out}; R_L=100Ω



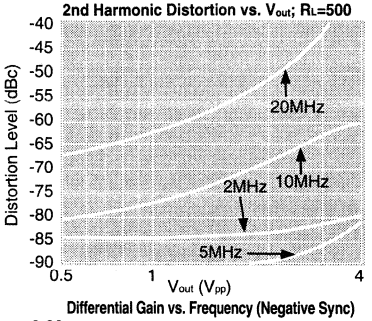
3rd Harmonic Distortion vs. V_{out}; R_L=100Ω



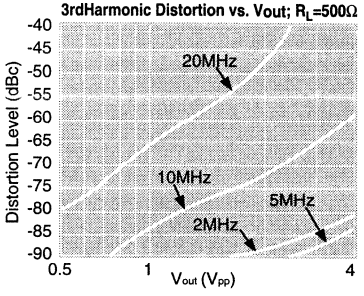
Reverse Transmission (S_{12})



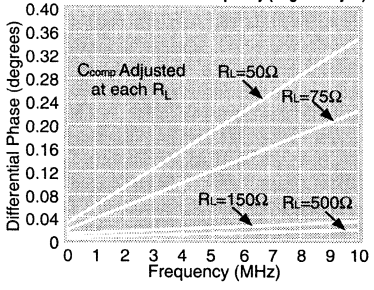
2nd Harmonic Distortion vs. V_{out}; R_L=500



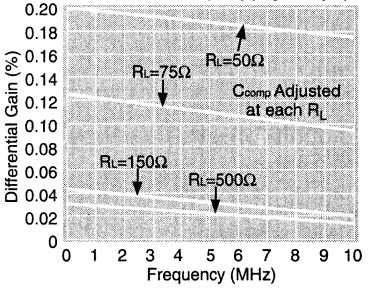
3rdHarmonic Distortion vs. Vout; R_L=500Ω



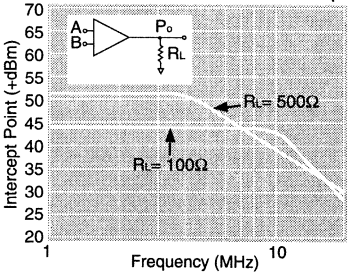
Differential Phase vs. Frequency (Negative Sync)



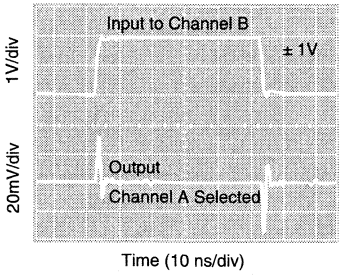
Differential Gain vs. Frequency (Negative Sync)



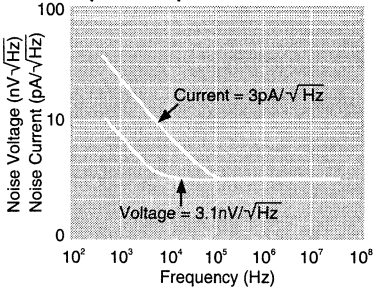
2-Tone, 3rd Order Intermodulation Intercept



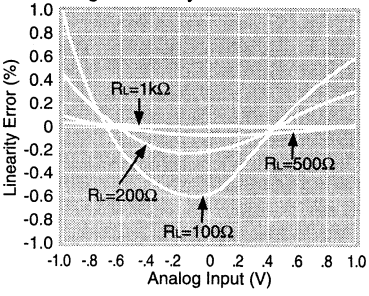
Transient Isolation



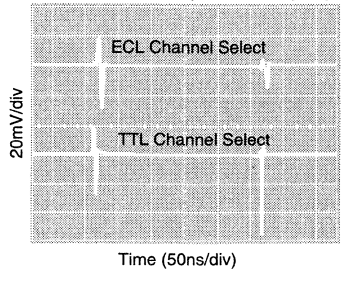
Equivalent Input Noise



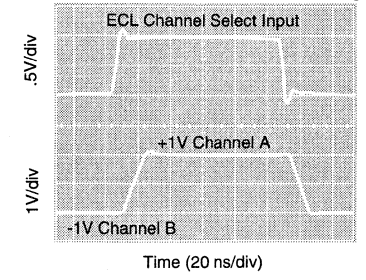
Integral Linearity Error



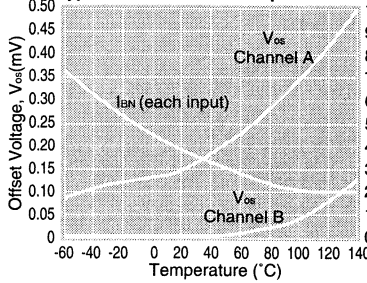
Switching Transient (Grounded Inputs)



Large Signal Channel-to-Channel Switching



Typical DC Errors vs. Temperature



8

Operation

The CLC532 is a 2:1 analog multiplexer with high-impedance buffered inputs, and a low-impedance, low-distortion, output stage. The CLC532 employs a closed-loop design, which dramatically improves accuracy. The channel SELECT control (Figure 1) determines which of the two inputs (IN_A or IN_B) is present at the OUTPUT. Beyond the basic multiplexer function, the CLC532 offers compatibility with either TTL or ECL logic families, as well as adjustable bandwidth.

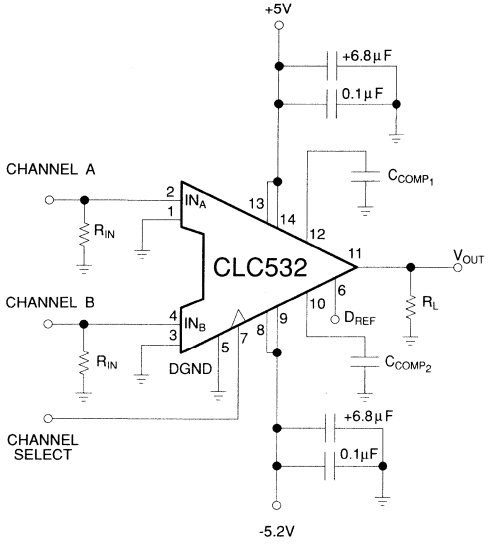


Figure 1: Standard CLC532 Circuit Configuration

Digital Interface and Channel SELECT

The CLC532 functions with ECL, TTL and CMOS logic families. D_{REF} controls logic compatibility. In normal operation, D_{REF} is left floating, and the channel SELECT responds to ECL level signals, Figure 2. For TTL or CMOS level SELECT inputs (Figure 3), D_{REF} should be tied to +5V (the CLC532 incorporates an internal 2300Ω series isolation resistor for the D_{REF} input). For TTL or CMOS operation, the channel SELECT requires a resistor input network to prevent saturation of the channel select circuitry. Without this input network, channel SELECT logic levels above 3V will cause internal junction saturation and slow switching speeds.

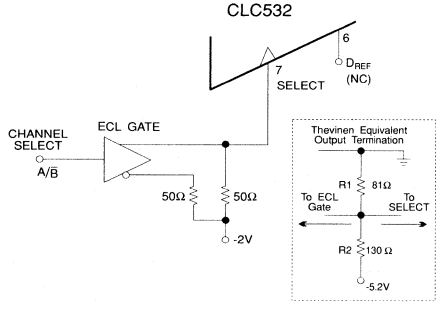


Figure 2: ECL Level Channel SELECT Configuration

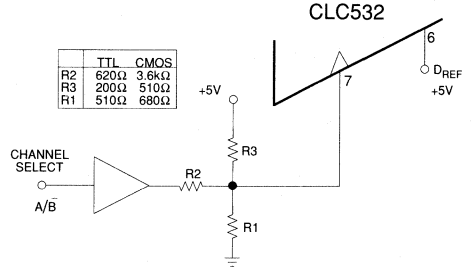


Figure 3: TTL/CMOS Level Channel SELECT Configuration

Compensation

The CLC532 incorporates compensation nodes that allow both its bandwidth and its settling time/slew rate to be adjusted. Bandwidth and settling time/slew adjustments are linked, meaning that lowering the bandwidth also lowers slew rate and lengthens settling time. Proper adjustment (compensation) is necessary to optimize system performance. Time Domain applications should generally be optimized for lowest RMS noise at the CLC532 output, while maintaining settling time and slew rates at adequate levels to meet system needs. Frequency Domain applications should generally be optimized for maximally flat frequency response.

Figure 4 below describes the basic relationship between bandwidth and R_S for various values of load capacitance, C_L, where C_{COMP} = 10pF.

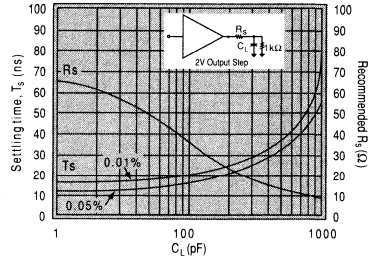


Figure 4: Settling Time and R_S vs. C_L

Figure 5 shows the resulting changes in bandwidth and slew rate for increasing values of C_{COMP}. The RMS noise at the CLC532 output can be approximated as:

$$OUTPUT_{NOISE_{RMS}} = (n_V)(\sqrt{1.57 * BW_{-3dB}})$$

where... n_V = input spot noise voltage;
BW_{-3dB} = Bandwidth is from figure 5.

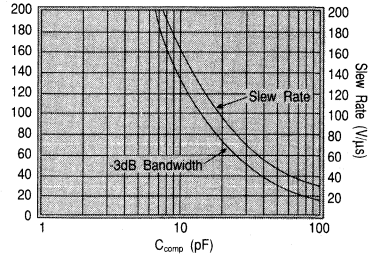


Figure 5: C_{COMP} for Maximally Flat Frequency Response

Power Supplies and Grounding

Proper power supply bypassing and grounding is essential to the CLC532's operation. A 0.1μF to 0.01mF ceramic chip capacitor should be located as close as possible to the individual power supply pins. Larger +6.8μF tantalum capacitors should be used within a few inches of the CLC532. The ground connections for these larger by-pass capacitors should be very symmetrically located relative the CLC532 output load ground connection. Harmonic distortion can be heavily influenced by non-symmetric decoupling capacitor grounding. The smaller chip capacitors located directly at the power supply pins are not particularly susceptible to this effect.

Separation of analog and digital ground planes is not recommended. In most cases, a single low-impedance ground plane will provide the best performance. In those special cases requiring separate ground planes, the following table indicates the signal and supply ground connections.

Pin	Functions	Ground Return
1,3	Shield /Supply Returns	Supplies and Inputs
5	D_{REF} Ground	D_{REF} Currents Only

Input Shielding

The CLC532 has been designed for use in high-speed wide-dynamic range systems. Guard-ring traces and the use of the ground pins separating the analog inputs are recommended to maintain high isolation (Figure 6). Likely sources of noise and interference that may couple onto the inputs, are the logic signals and power supplies to the CLC532. Other types of clock and signal traces should not be overlooked, however.

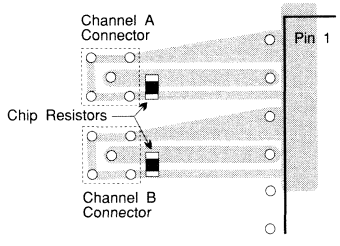


Figure 6: Alternate Layout Using Guard Ring

The general rule in maintaining isolation has two facets, minimize the primary return ground current path impedances back to the respective signal sources, while maximizing the impedance associated with common or secondary ground current return paths. Success or failure to optimize input signal isolation can be measured directly as the isolation between the input channels with the CLC532 removed from circuit. The channel-to-channel isolation of the CLC532 can never be better than the isolation level present at its inputs.

Special attention must be paid to input termination resistors. Minimizing the return current path that is common to both of the input termination resistors is essential. In the event that a ground return current from one input termination resistor is able to find a secondary path back to its signal source (which also happens to be common with either the primary or secondary return path for the second input termination resistor), a small voltage can appear across the second input termination resistor. The small voltage seen across the second input termination resistor will be highly correlated with the signal generating the initial return currents. This situation will severely degrade channel-to-channel isolation at the input of the CLC532, even if the CLC532 were removed from circuit. Poor isolation at the input will be transmitted directly to the output.

Use of "small" value input termination resistors will also improve channel-to-channel isolation. However, extremely low values (<25Ω) tend to stress the driving source's ability to provide a high-quality input signal to the CLC532. Higher values tend to aggravate any layout dependent crosstalk. 75Ω to 50Ω is a reasonable target, but the lower the better.

Combining Two Signals in ADC Applications

The CLC532 is applicable in a wide range of circuits and applications. A classic example of this flexibility is combining two or more signals for digitization by an analog-to-digital converter (ADC). A clear understanding of both the multiplexer and the ADC's operation is needed to optimize this configuration.

To obtain the best performance from the combination, the output of the CLC532 must be an accurate representation of the selected input during the ADC conversion cycle. The time at which the ADC samples the input varies with the type of ADC that is being used.

Subranging ADCs usually have a Track-and-Hold (T/H) at their input. For a successful combination of the multiplexer and the ADC, the multiplexer timing and the T/H timing must be compatible. When the ADC is given a convert command, the T/H transitions from Track mode to Hold mode. The delay between the convert command and this transition is usually specified as Aperture Delay or as Sampling Time Offset.

To maximize the time that the multiplexer output has to settle, and that the T/H has to acquire the signal, the multiplexer should begin its transition from one input to the other immediately after the T/H transition into HOLD mode. Unfortunately it is during the initial portion of the HOLD period that a subranging ADC performs analog processing of the sampled signal. High slew rate transitions on the input during this time may have a detrimental effect on the conversion accuracy.

To minimize the effects of high input slew rates, two strategies that can employed. Strategy one applies when the sample rate of the system is below the rated speed of the ADC. Here the CLC532 SELECT timing is delayed until after the multiplexer transition takes place, and after the A/D has completed one conversion cycle and is waiting for the next convert command. As an example, if a CLC935 (15MSPS) ADC is being used at 10MSPS, the conversion takes place in the first 67ns after the CONVERT command. The next 33ns are spent waiting for the next CONVERT command, and would be an ideal place to switch the multiplexer from one channel to the next.

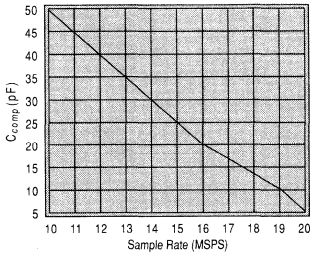


Figure 7: Recommended C_{COMP} vs. ADC Sample Rate

The second optimization strategy involves lowering the slew rate at the input of the ADC so that fewer high frequency components are available to feed through to the hold capacitor during HOLD

mode. The CLC532 output signal can be slew limited by using its compensation capacitors. This approach also has the advantage of limiting the excess noise passed through the CLC532 and on to the ADC. Figure 7 shows the recommended C_{COMP} values as a function of ADC Sample rate. Since the optimal values will change from one ADC to the next, this graph should be used as a starting point for C_{COMP} selection. Both C_{COMP} capacitors should be the same value to maintain output symmetry.

Flash ADCs are similar to subranging ADCs in that the sampling period is very brief. The primary difference is that the acquisition time of a flash converter is much shorter than that of a subranging ADC. With a flash ADC, the transition of the CLC532 output should be after the sampling instant ("Aperture Delay" after the CONVERT command). It is only during this period that a flash converter is susceptible to interference from a rapidly changing analog input signal.

Gain Selection for an ADC

In many applications, such as RADAR, the dynamic range requirements may exceed the accuracy requirements. Since wide dynamic range ADCs are also typically highly accurate ADCs, this often leads the designer into selecting an ADC which is a technical overkill and a budget buster. By using the CLC532 as a selectable-gain stage, a less expensive ADC can be used. As an example, if an application calls for 80dB of dynamic Range and 0.05% accuracy, rather than using a 14-bit converter, a 12-bit converter combined with the circuit in figure 8 will meet the same objective. The CLC532 is used to select between the analog input signal and a version of the input signal attenuated by 12dB. This circuit affords 14-bit dynamic range, 12-bit accuracy and 12-bit ease of implementation.

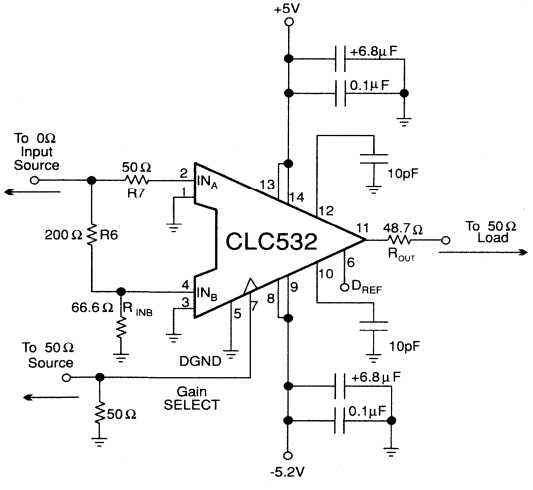


Figure 8: Selectable Gain Stage Improves ADC Dynamic Range

Full Wave Rectifier Circuit

The use of a diode rectifier provides significant distortion for signals that are small compared to the forward bias voltage. Accordingly, when low distortion performance is needed, standard diode based circuits do not work well. The CLC532 can be configured to provide a very low distortion full wave rectifier. The circuit in figure 9 is used to select between an analog input signal and an inverted version of the input signal. The resulting output exhibits very little distortion for small scale signals up to several hundred kilohertz.

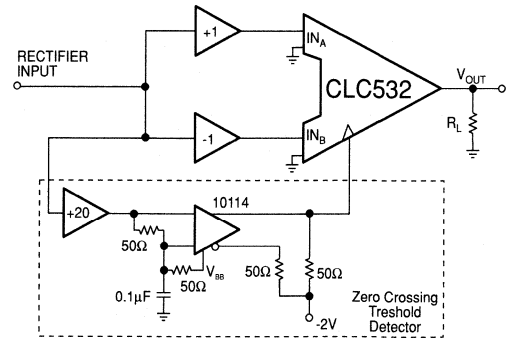


Figure 9: Low Distortion Full Wave Rectifier

Use of the CLC532 as a Mixer.

A double balanced mixer, such as is shown in figure 10, operates by multiplying the RF input by the LO input. This is done by using the LO to select one of two paths through a diode bridge depending upon the LO sign. The result is an output where IF=RF when LO>0 and IF=-RF if LO<0. This same result can be obtained with the circuit shown in figure 11. The CLC532 based circuit uses a digital LO making system design easier in those cases where the LO is digitally derived. One advantage of the CLC532 based approach is excellent isolation between all three ports. Also see the *RF design awards* article by Thomas Hack in the January 1993 issue of *RF Design*.

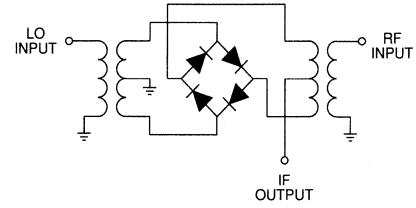


Figure 10: Typical Double-Balanced Mixer

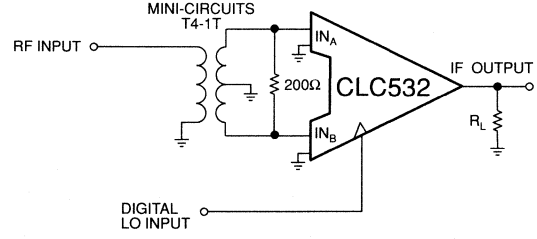


Figure 11: High-Isolation Mixer Implementation

Evaluation Board

An evaluation board (part number 730028) for the CLC532 is available. This board can be used for fast, trouble-free, evaluation and characterization of the CLC532. Additionally, this board serves as a template for layout and fabrication information. The CLC532 evaluation board data sheet is available from Comlinear.

Comlinear Corporation

High-Speed 4:1 Analog Multiplexer

CLC533

APPLICATIONS:

- infrared system multiplexing
- CCD sensor signals
- radar I/Q switching
- high definition video HDTV
- test and calibration

FEATURES (typical):

- 12-bit settling (0.01%) - 17ns
- low noise - 42μVrms (dc to 100MHz)
- isolation - 80dB @ 10MHz
- low distortion - 80dB @ 5MHz
- adjustable bandwidth

DESCRIPTION:

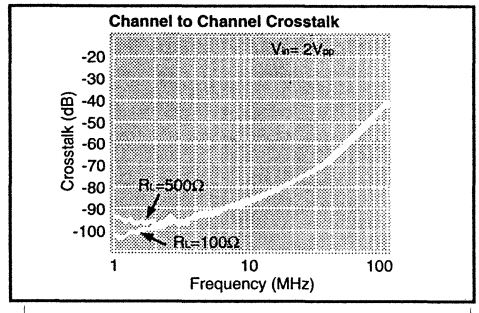
The CLC533 is a high-speed 4:1 multiplexer employing active input and output stages. The CLC533 also employs a closed-loop design which dramatically improves accuracy over conventional analog multiplexer circuits. This monolithic device is constructed using an advanced high-performance bipolar process.

The CLC533 has been specifically designed to provide a 24ns settling time to 0.01%. This coupled with the adjustable bandwidth, makes the CLC533 an ideal choice for infrared and CCD imaging systems, with channel-to-channel isolation of 80dB @ 10MHz. Low distortion and spurious signal levels (-80dBc) make the CLC533 a very suitable choice for I/Q processors in Radar receivers.

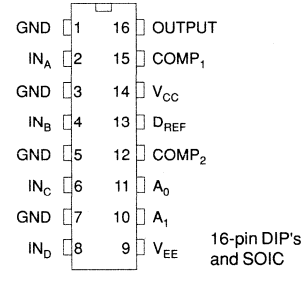
The CLC533 is offered over both the industrial and military temperature ranges. The Industrial versions, CLC533AJP\AJE\AIB, are specified from -40°C to +85°C and are packaged in 16-pin plastic DIPs, SOIC's and CERDIP packages. The extended temperature versions, CLC533A8B/A8L-2A, are specified from -55°C to +125°C and are packaged in 16-pin CERDIP and 20-terminal LCC packages.

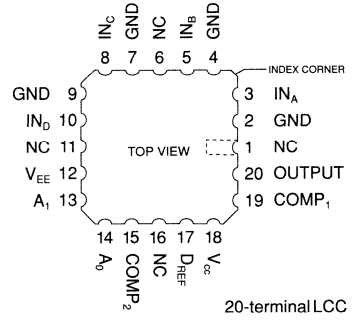
Ordering Information ...

CLC533AJP	-40°C to +85°C	16-pin plastic DIP
CLC533AJE	-40°C to +85°C	16-pin plastic SOIC
CLC533AIB	-40°C to +85°C	16-pin CERDIP
CLC533A8B	-55°C to +125°C	16-pin CERDIP, MIL-STD-883
CLC533A8L-2A	-55°C to +125°C	20-terminal LCC, MIL-STD-883



Pinouts

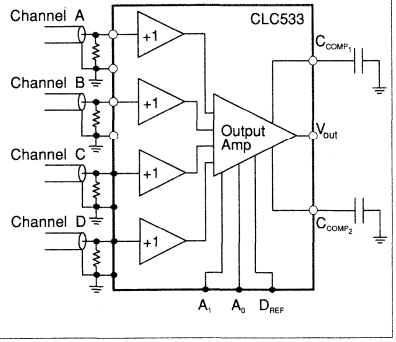




Functional Diagram

A_1	A_0	OUT
0	0	A
0	1	B
1	0	C
1	1	D

ECL Mode - D_{REF}=open
TTL Mode - D_{REF}=+5V



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DS533.00(Preliminary)
January 1993

Electrical Characteristics ($+V_{CC}$=+5.0V; $-V_{EE}$=-5.2V; R_{IN}=50Ω; R_L=500Ω; C_{COMP}=8pF; ECL Mode, pin 13 = NC)

PARAMETER[1]	CONDITIONS	TYP	MAX & MIN RATINGS[2]			UNITS	SYMBOL
Ambient Temperature	CLC533A8B/A8L-2A	+25°C	-55°C	+25°C	+125°C		
Ambient Temperature	CLC533AJP/AJE/AIB	+25°C	-40°C	+25°C	+85°C		
FREQUENCY DOMAIN PERFORMANCE							
†-3dB bandwidth	V_{OUT}<0.1Vpp	180	130	130	110	MHz	SSBW
-3dB bandwidth	V_{OUT}=2Vpp	45	35	35	30	MHz	LSBW
†gain flatness	V_{OUT}<0.1Vpp						
peaking	dc to 200MHz	0.2	0.5	0.5	0.5	dB	GFP
rolloff	dc to 100MHz	1.0	2.0	2.0	3.0	dB	GFR
linear phase deviation	dc to 100MHz	2.0				deg	LPD
differential gain	C_{COMP} = 5pF; R_L=150Ω	TBD				%	DG
differential phase	C_{COMP} = 5pF; R_L=150Ω	TBD				deg	DP
crosstalk rejection - 1 channel	2Vpp, 10MHz	80	74	74	74	dB	CT10
	2Vpp, 20MHz	74	68	68	68	dB	CT20
	2Vpp, 30MHz	68	62	62	62	dB	CT30
crosstalk rejection - 3 channels	2Vpp, 10MHz	80	74	74	74	dB	3CT10
	2Vpp, 20MHz	74	68	68	68	dB	3CT20
	2Vpp, 30MHz	68	62	62	62	dB	3CT30
TIME DOMAIN PERFORMANCE							
rise and fall time	0.5V step	2.7	3.3	3.3	3.8	ns	TRS
	2V step	10	12.5	12.5	14.5	ns	TRL
settling time[2] 2V step	±0.01%	17	24	24	27	ns	TSP
	±0.1%	13	18	18	21	ns	TSS
overshoot	2.0V step	2	5	5	6	%	OS
slew rate		160	130	130	110	V/µs	SR
SWITCH PERFORMANCE							
channel to channel switching time	50% SELECT to 10%V_{OUT}	6	8	8	9	ns	SWT10
(2V step at output)	50% SELECT to 90%V_{OUT}	16	21	21	24	ns	SWT90
switching transient		30				mV	ST
DISTORTION AND NOISE PERFORMANCE							
†2nd harmonic distortion	2Vpp, 5MHz	80	67	67	67	dBc	HD2
†3rd harmonic distortion	2Vpp, 5MHz	86	67	67	67	dBc	HD3
equivalent input noise							
spot noise voltage	>1MHz	4.2				nV/√Hz	SNF
integrated noise	1MHz to 100MHz	42	54		51	µVrms	INV
spot noise current		5				pA/√Hz	SNF
STATIC AND DC PERFORMANCE							
*analog output offset		1	12	3.5	4.5	mV	VOS
temperature coefficient		15	90		20	µV/°C	DVIO
analog output offset matching		TBD					
*analog input bias current		50	280	120	120	µA	IBN
temperature coefficient		0.3	2.0		0.8	µA/°C	DIBN
analog input bias current matching		TBD					
analog input resistance		200	90	120	120	kΩ	RIN
analog input capacitance		2	3.0	2.5	2.5	pF	CIN
*gain accuracy	±2V	0.994	0.988	0.988	0.988	V/V	GA
gain matching		TBD					
integral endpoint linearity	±1V (full scale)	0.02	0.05	0.03	0.03	%FS	ILIN
output voltage	no load	±3.4	2.4	2.8	2.8	V	VO
output current		45	20	50	50	mA	IO
output resistance	dc	1.5	4.0	2.5	2.5	Ω	RO
DIGITAL INPUT PERFORMANCE							
ECL mode (D_{REF} floating)							
input voltage logic HIGH			-1.1	-1.1	-1.1	V	VIH1
input voltage logic LOW			-1.5	-1.5	-1.5	V	VIL1
input current logic HIGH		200	220	80	80	µA	IIH1
input current logic LOW		200	220	80	80	µA	IIL1
TTL mode (D_{REF} = +5V)							
input voltage logic HIGH			2.0	2.0	2.0	V	VIH2
input voltage logic LOW			0.8	0.8	0.8	V	VIL2
input current logic HIGH		200	220	80	80	µA	IIH2
input current logic LOW		200	220	80	80	µA	IIL2
POWER REQUIREMENTS							
*supply current (+V_{CC} = +5.0V)	no load	28	38	36	36	mA	ICC
*supply current (-V_{EE} = -5.2V)	no load	28.5	39	37	37	mA	IEE
nominal power dissipation	no load	288				mW	PD
*power supply rejection ratio			-53	-60	-60	dB	PSRR

Comlinear reserves the right to change specifications without notice.

Recommended Operating Conditions

positive supply voltage ($+V_{CC}$)	+5.0V
negative supply voltage ($-V_{EE}$)	-5.2V
differential voltage between any two GND's	10mV
analog input voltage range	±2V
A_X input voltage range (TTL mode)	0V to +5.0V
A_X input voltage range (ECL mode)	0V to -2.0V
C_{COMP} range	5pF to 100pF

thermal data	θ_{JC}(°C/W)	θ_{JA}(°C/W)
16-pin plastic		75
16-pin Cerdip	35	75
16-pin SOIC		100
20-terminal LCC		

Absolute Maximum Ratings[3]

positive supply voltage ($+V_{CC}$)	-0.5V to +7.0V
negative supply voltage ($-V_{EE}$)	+0.5V to -7.0V
differential voltage between any two GND's	200mV
analog input voltage range	$-V_{EE}$ to $+V_{CC}$
digital input voltage range	$-V_{EE}$ to $+V_{CC}$
output short circuit duration (output shorted to GND)	Infinite
junction temperature	+175°C
operating temperature range	
CLC533AJP/AJE/AIB	-40°C to +85°C
CLC533A8B/A8L-2A	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec

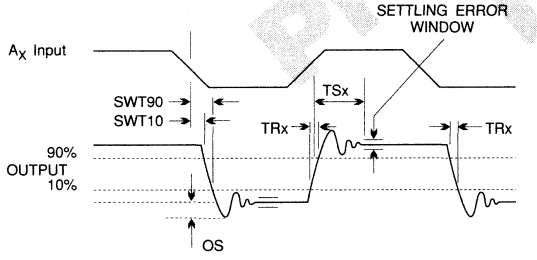
Note1: Test levels are as follows:

*	AI/AJ	: 100% tested at +25°C, sample at +85°C.
†	AJ	: Sample tested at +25°C.
†	AI	: 100% tested at +25°C.
*	A8	: 100% tested at +25°C, -55°C, +125°C.
†	A8	: 100% tested at +25°C, sample at -55°C, +125°C

Note 2: Settling time measured from the 50% analog output transition.

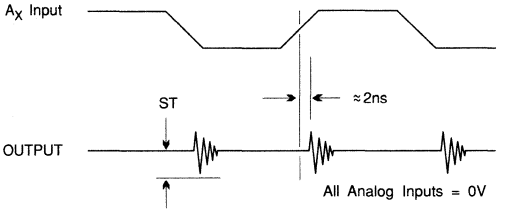
Note 3: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

System Timing Diagram

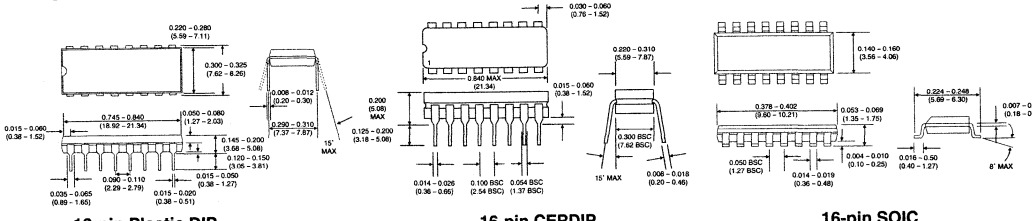


... where TSx is TS14 or TSP or TSS, and TRx is TRS ro TSL.

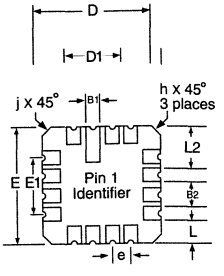
Switching Transient Timing Diagram



Package Dimensions



16-pin Plastic DIP | 16-pin CERDIP | 16-pin SOIC

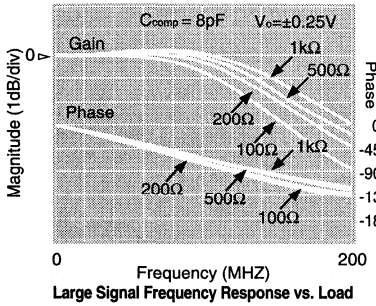


20- terminal LCC

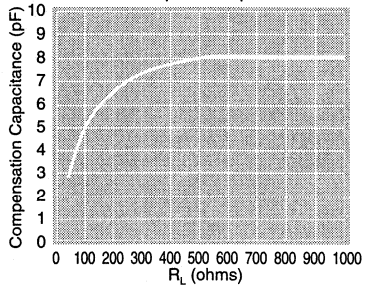
Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A1	0.050	0.088	1.27	2.23
B1	0.022	0.028	0.56	0.71
B2	0.072 REF		1.83 REF	
D,E	0.342	0.358	8.69	9.09
D1,E1	0.200 BSC		5.08 BSC	
e	0.050 BSC		1.27 BSC	
h	0.040 REF		1.02 REF	
j	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41

Typical Performance Characteristics (+25°C unless otherwise specified)

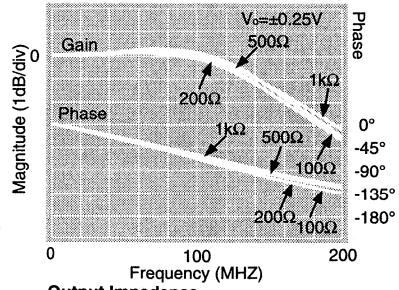
Small Signal Gain/Phase vs. Load



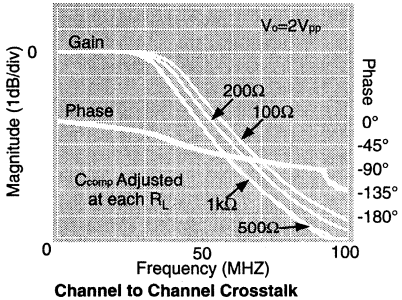
Recommended Compensation Capacitance vs. Load



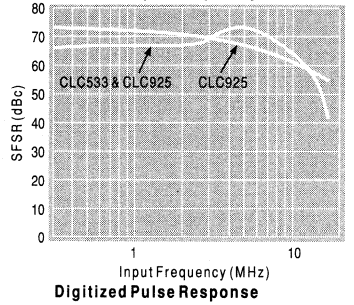
Small Signal Gain/Phase vs. Load with Recomended Ccomp



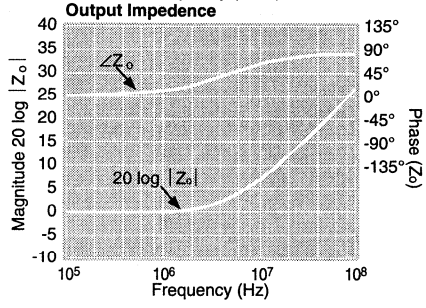
Large Signal Frequency Response vs. Load



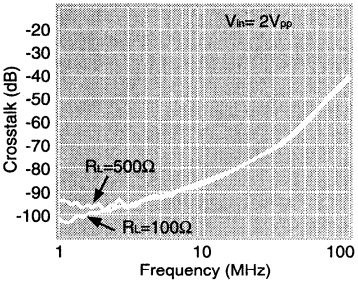
SFDR vs. Input Frequency



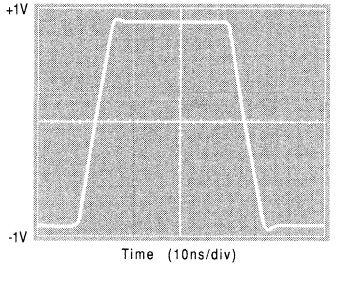
Output Impedence



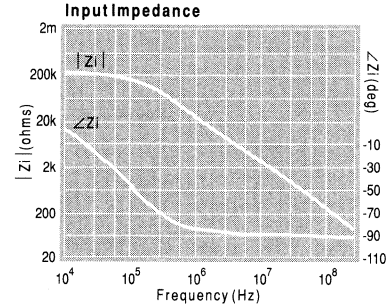
Channel to Channel Crosstalk



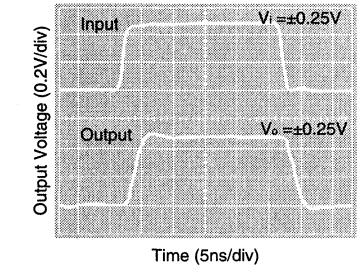
Digitized Pulse Response



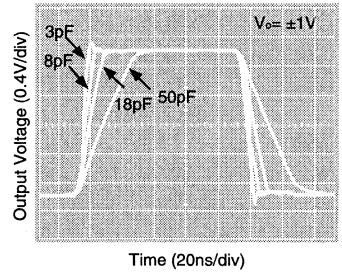
Input Impedance



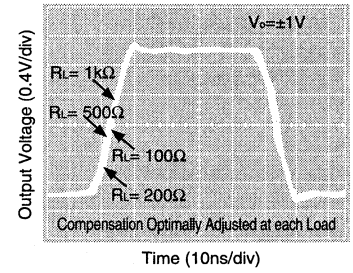
Small Signal Pulse Response



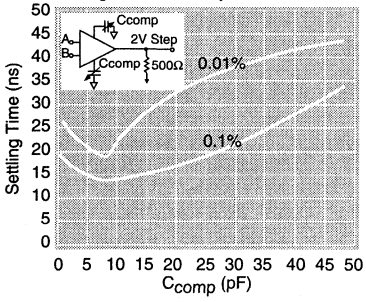
Large Signal Pulse vs. Ccomp



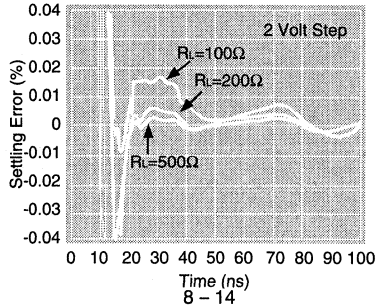
Large Signal Pulse Response vs. RL



Settling Time vs. Ccomp

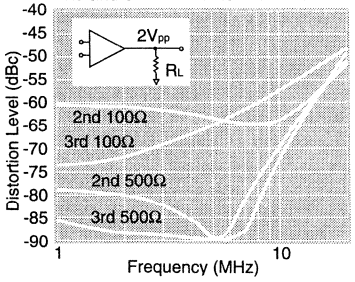


Settling Time vs. RL

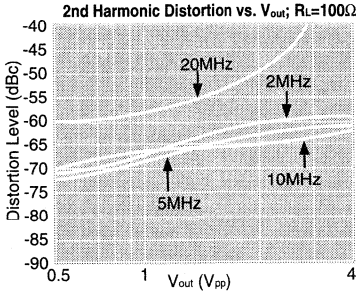


Typical Performance Characteristics (+25°C unless otherwise specified)

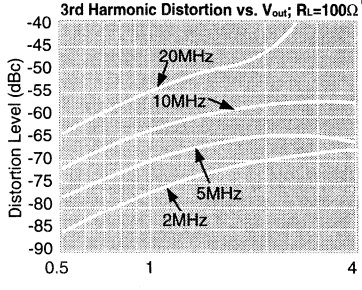
2nd and 3rd Harmonic Distortion



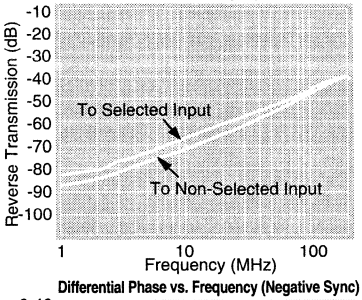
2nd Harmonic Distortion vs. V_{out}; R_L=100Ω



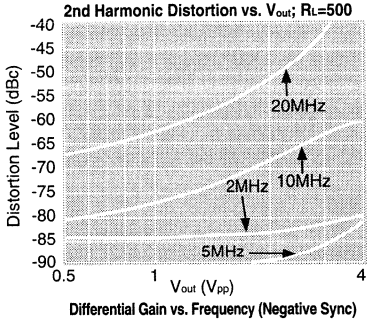
3rd Harmonic Distortion vs. V_{out}; R_L=100Ω



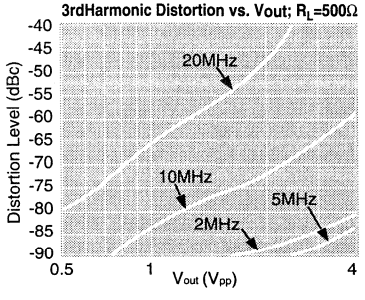
Reverse Transmission (S_{12})



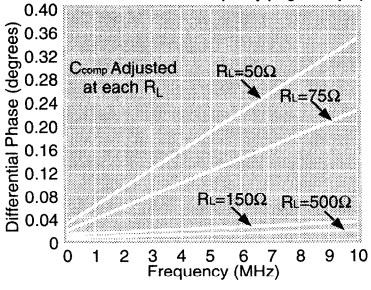
2nd Harmonic Distortion vs. V_{out}; R_L=500



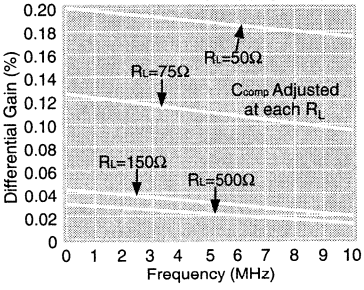
3rdHarmonic Distortion vs. Vout; R_L=500Ω



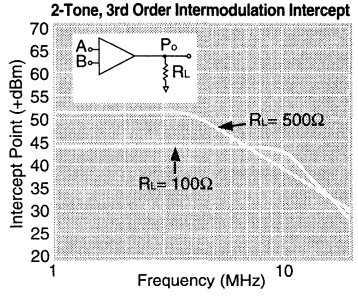
Differential Phase vs. Frequency (Negative Sync)



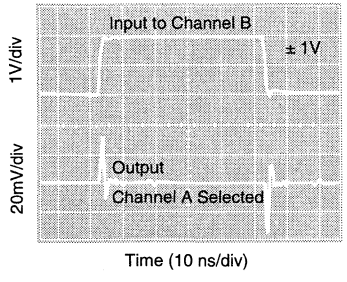
Differential Gain vs. Frequency (Negative Sync)



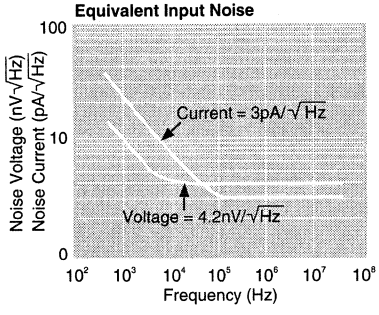
2-Tone, 3rd Order Intermodulation Intercept



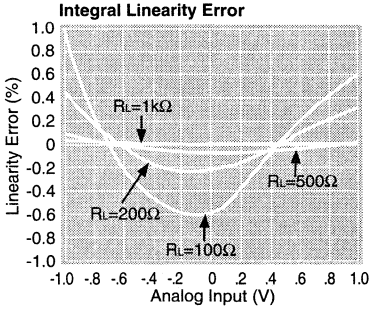
Transient Isolation



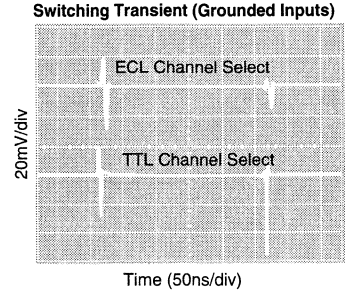
Equivalent Input Noise



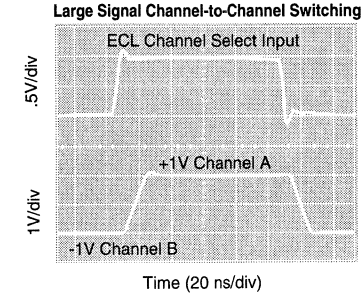
Integral Linearity Error



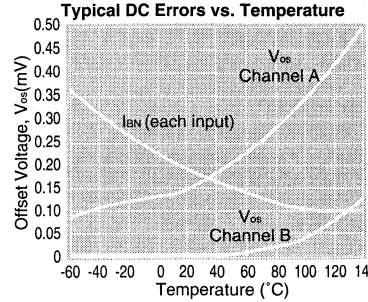
Switching Transient (Grounded Inputs)



Large Signal Channel-to-Channel Switching



Typical DC Errors vs. Temperature



8

OPERATION

The CLC533 is a 4:1 analog multiplexer with high-impedance buffered inputs, and a low-impedance, low-distortion, output stage. The CLC533 employs a closed-loop design, which dramatically improves accuracy. The channel select controls (A_0 and A_1) determine which of the four inputs (IN_A thru IN_D) is present at the OUTPUT. Beyond the basic multiplexer function, the CLC533 offers compatibility with either TTL/CMOS or ECL logic families, as well as adjustable bandwidth.

Digital Interface and Channel SELECT

The CLC533 functions with ECL, TTL and CMOS logic families. D_{REF} controls logic compatibility. In normal operation, D_{REF} is left floating, and the channel select controls (A_0 and A_1) respond to ECL level signals, Figure 1. For TTL or CMOS level SELECT inputs (Figure 2), D_{REF} should be tied to +5V (the CLC533 incorporates an internal 2300Ω series isolation resistor for the D_{REF} input).

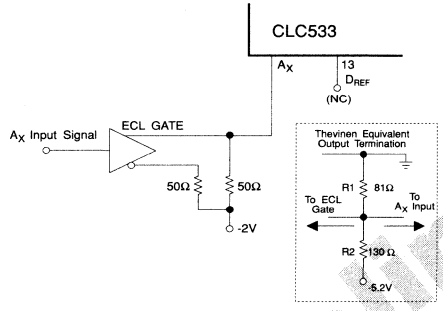


Figure 1: ECL Level Channel SELECT Configuration

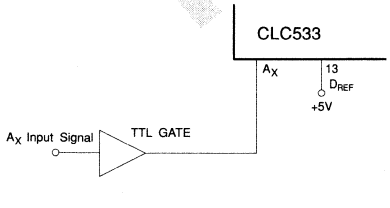


Figure 2: TTL/CMOS Level Channel SELECT Configuration

Power Supplies and Grounding

Proper power supply bypassing and grounding is essential to the CLC533's operation. A 0.1µf to 0.01µf ceramic chip capacitor should be located as close as possible to the individual power supply pins. Larger +6.8µf tantalum capacitors should be used in the immediate area of the CLC533. The ground connections for these larger by-pass capacitors should be very symmetrically located relative the CLC533 output load ground connection. Harmonic distortion can be heavily influenced by non-symmetric decoupling capacitor grounding. The smaller chip capacitors located directly at the power supply pins are not particularly susceptible to this effect.

Separation of analog and digital ground planes is not recommended. In most cases, a single low-impedance ground plane will provide the best performance.

Input Shielding

The CLC533 has been designed for use in high-speed wide-dynamic range systems. Guard-ring traces and the use of the ground pins separating the analog inputs is required to maintain high isolation (Figure 3). Likely sources of noise and interference that may couple onto the inputs, are the logic signals and power supplies to the CLC533. Other types of clock and signal traces should not be overlooked, however.

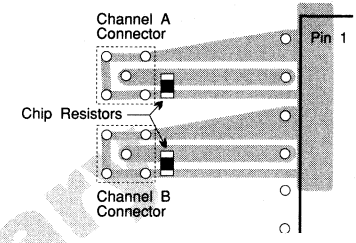


Figure 3: Analog Input Using Guard Ring

The general rule in maintaining isolation has two facets, minimize the primary return ground current path impedances back to the respective signal sources, while maximizing the impedance associated with common or secondary ground current return paths. Success or failure to optimize input signal isolation can be measured directly as the isolation between the input channels with the CLC533 removed from circuit. The channel-to-channel isolation of the CLC533 can never be better than the isolation level present at its inputs.

Special attention must be paid to input termination resistors. Minimizing the return current path that is common to both of the input termination resistors is essential. In the event that ground return current from one input termination resistor is able find a secondary path back to its signal source (which also happens to be common with either the primary or secondary return path for the second input termination resistor), a small voltage will appear at the second input which is completely dependent on the first input signal. This situation will severely degrade channel-to-channel isolation at the input of the CLC533, even if the CLC533 were removed from circuit. Poor isolation at the input will be transmitted directly to the output.

Use of "small" value input termination resistors will also improve channel-to-channel isolation. Extremely low values, <25Ω, tend to stress the driving source's ability to provide a high-quality input signal to the CLC533. Higher values tend to aggravate any layout dependent crosstalk. 75Ω to 50Ω is a reasonable target, but the lower the better.

Evaluation Board

An evaluation board (part number 730035 for DIP's and 730039 for SOIC's) for the CLC533 is available. This board can be used for fast, trouble-free, evaluation and characterization of the CLC533. Additionally, this board serves as a template for layout and fabrication information. The CLC533 evaluation board data sheet is available from Comlinear.

Track and Hold Amplifiers

Contents

Comlinear Corporation

Fast Sampling, Wideband Track and Hold Amplifier

CLC940

APPLICATIONS:

- flash A/D driving
- high-resolution, subranging A/D driving
- signal deglitching (as in CCD or D/A systems)
- communication systems
- radar and IF processors

FEATURES (typical):

- 10ns hold-to-track acquisition time
- 12ns track-to-hold settling time
- 1ps aperture jitter
- 150MHz small signal bandwidth
- 74dB feedthrough rejection
- ECL or TTL control signals

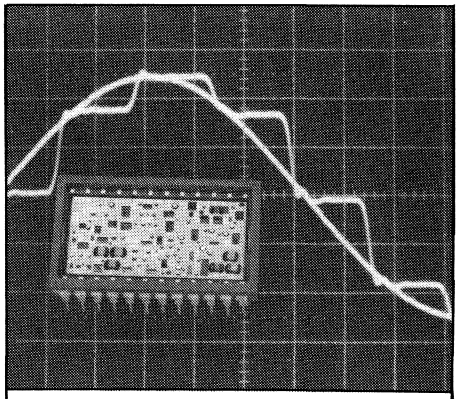
DESCRIPTION

The CLC940 Flash-Track™ is a fast sampling, wideband track and hold amplifier which offers 12ns switching performance plus an unprecedented array of supporting specifications. This combination ensures that the accuracy indicated by the switching specifications is fully realized.

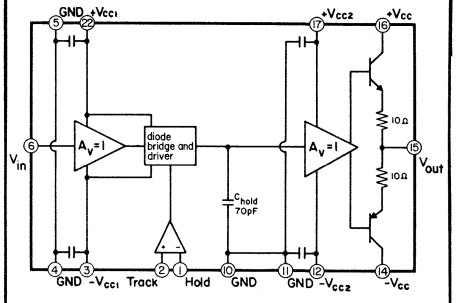
The Flash-Track is an ideal device for driving flash A/Ds–especially those configured in high resolution, subranging architectures. The very fast 10ns hold-to-track acquisition time and 12ns track-to-hold settling time permit the high sampling rates needed in applications such as radar and communications. Other specifications, such as the 1ps aperture jitter, 2mV pedestal offset, and –57dB harmonic distortion are similarly supportive of A/D system performance goals. The CLC940 is fully compatible with demanding flash A/D input requirements as demonstrated by its ±2.2V output range and its ability to drive up to 90pF loads at full performance.

Ease of use and functionality are also characteristics of the Flash-Track; for example, the device needs only ±15V supplies and can accept either ECL or TTL control signals. In addition, conservative specifications and 100% testing assure dependable, consistent insystem performance.

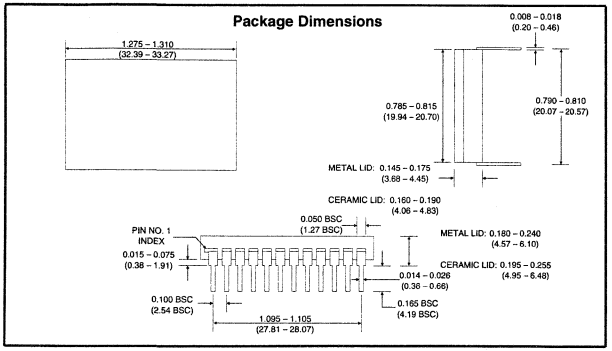
The CLC940 is constructed using thin film resistor/bipolar transistor technology. The CLC940AI is specified over a temperature range of –25°C to +85°C, while the CLC940AM is specified over a range of –55°C to +125°C and is screened to Comlinear's M Standard for high reliability applications. Both devices are packaged in 24-pin, 800 mil wide, ceramic DIPS.



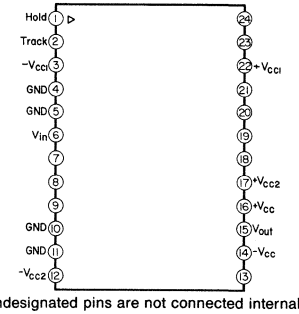
Equivalent Circuit



Package Dimensions



Pin Out



Undesignated pins are not connected internally.

Electrical Characteristics ($R_L = 100\Omega$, $V_{cc} = \pm 15V$)

PARAMETERS[1]	CONDITIONS	TYP	MIN & MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC940AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC940AI	+25°C	−25°C	+25°C	+85°C		
TRACK-MODE DYNAMICS							
* −3dB bandwidth		150	>140	>140	>100	MHz	SSBW
slew rate		470	>440	>440	>390	V/μs	SR
2nd harmonic distortion	$2V_{pp}$, 20MHz, $R_L = 1k\Omega$	−57	<−51	<−51	<−47	dBc	HD2
3rd harmonic distortion	$2V_{pp}$, 20MHz, $R_L = 1k\Omega$	−60	<−54	<−54	<−54	dBc	HD3
HOLD-MODE DYNAMICS							
* droop rate		20	<250	<50	<2000	μV/μs	DR
* feedthrough rejection	20MHz, $V_{in} = 2V_{pp}$	74	>70	>70	>70	dB	FTR
TRACK-TO-HOLD SWITCHING							
* effective aperture delay		2.5	<3.3	<3.0	<3.0	ns	TA
* aperture jitter		1	<1.4	<1.4	<1.6	ps_{rms}	UHD
* pedestal offset		2	<8	<5	<8	mV	PO
temperature coefficient	end point average	25	<60	<60	<60	μV/°C	DPO
sensitivity to supply voltage		—	<0.5	<0.5	<0.5	mV/V	PORR
switching transient (peak-to-peak	amplitude) $f_s = 2MHz$	25	<50	<30	<40	mV_{pp}	HTA
track-to-hold settling time	to 1mV	12	<18	<14	<14	ns	HTS
HOLD-TO-TRACK SWITCHING							
acquisition time to 1.0%	$V_i = 2V_{pp}$, $R_L = 1k\Omega$	10	<15	<12	<12	ns	ATS
to 0.1%		16	<22	<18	<22	ns	ATSP
DC ACCURACY							
* gain	1kHz, $4V_{pp}$, no load	0.98	>0.96	>0.96	>0.96	V/V	G
temperature coefficient		20	<30	<30	<30	ppm/°C	DG
non-linearity		0.02	<0.025	<0.025	<0.025	%	GNL
* offset voltage		20	<75	<60	<60	mV	VIO
temperature coefficient	end point average	30	<140	<140	<140	μV/°C	DVIO
* power supply rejection ratio		40	>36	>36	>36	dB	PSRR
DIGITAL INPUTS							
differential input threshold	$\lvert V_{track} - V_{hold} \rvert$	—	<300	<300	<300	mV	VDIF
input bias current (track mode)	high	25	<100	<50	<50	μA	IIH
	low	1	<10	<5	<5	μA	IIL
ANALOG INPUT							
input voltage range[2]		—	±2.2	±2.2	±2.2	V	VI
input resistance		20	>15	>15	>15	kΩ	RIN
input capacitance		3	<4	<4	<4	pF	CIN
* input bias current		30	<90	<60	<60	μA	IB
ANALOG OUTPUT							
* output resistance	at 1kHz	10	<12	<12	<13	Ω	RO
POWER REQUIREMENTS							
* supply current	$V_{in} = 0$, track mode, no load	55	<65	<60	<60	mA	ICC
power dissipation	$V_{in} = 0$, track mode, no load	1.65	<1.95	<1.80	<1.80	W	PD

Recommended Operating Conditions

supply voltage	
$\pm V_{cc1}$ and $\pm V_{cc2}$	±15V (±13.5V min.)
$\pm V_{cc}$	±15V (±5V min.)
ambient temperature	AI: −25°C to +85°C
	AM: −55°C to +125°C
minimum digital input slew rate	20V/μs
maximum differential digital input voltage	±2.5V
digital input voltage	$\pm(V_{cc1} - 11V)$

Absolute Maximum Ratings

analog input voltage	±5V
differential digital input voltage	±3.5V
digital input voltage	$\pm(V_{cc1} - 9V)$
output current	±50mA continuous
supply voltage (V_{cc}, V_{cc1}, and V_{cc2})	±20V
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating case temperature	AI: −25°C to +85°C
	AM: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

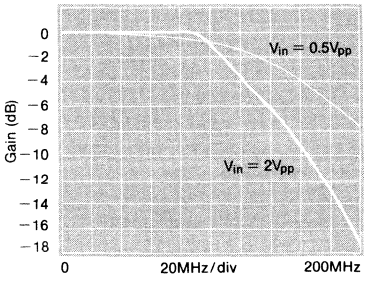
note 1: Parameters preceded by an * are the final electrical test parameters and are 100% tested. AM units are tested at -55°C +25°C, and +125°C. AI units are tested only at +25°C although their performance is guaranteed at -25°C and +85°C as indicated above.

note 2: For optimum performance the differential voltage between the input and output should not exceed 3V in HOLD mode.

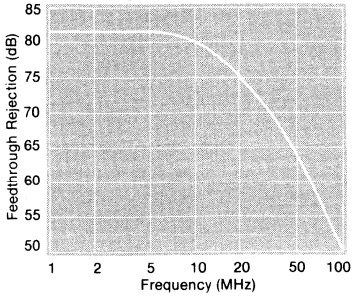
note 3: Absolute Maximum Ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Typical Performance Characteristics ($T_A = 25°C$, $R_L = 100\Omega$, $V_{cc} = \pm 15V$)

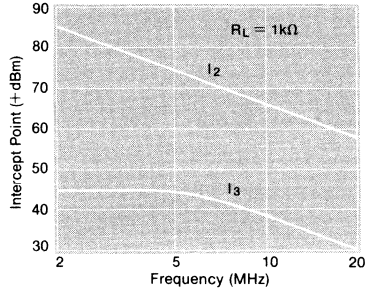
Gain vs. Frequency



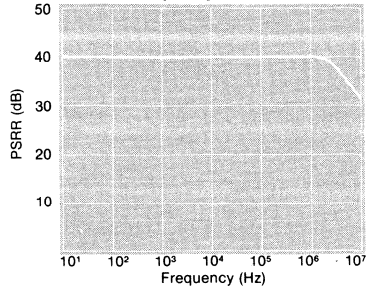
Feedthrough Rejection vs. Frequency



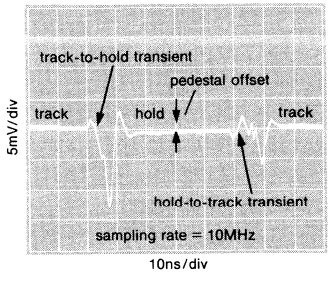
2nd and 3rd Harmonic Distortion Intercepts



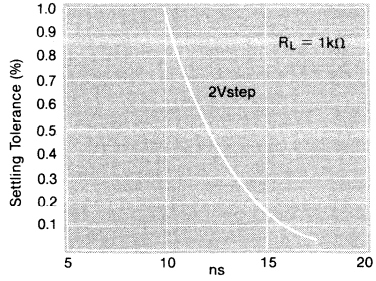
Power Supply Rejection Ratio vs. Frequency



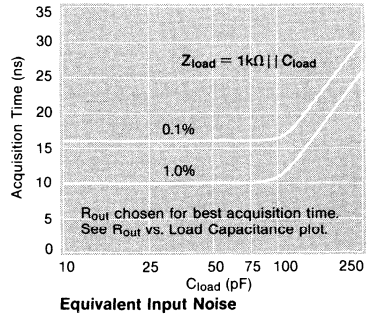
Switching Transients and Pedestal



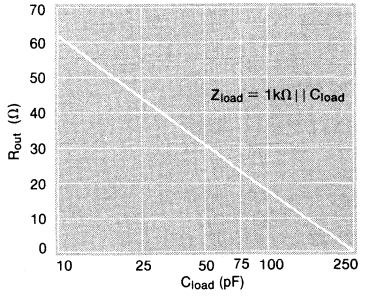
Settling Tolerance vs. Acquisition Time



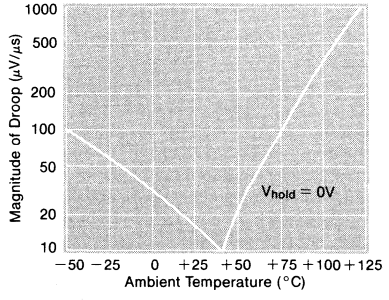
Acquisition Time vs. Load Capacitance



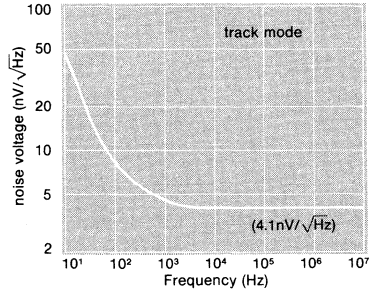
Recommended R_{out} vs. Load Capacitance



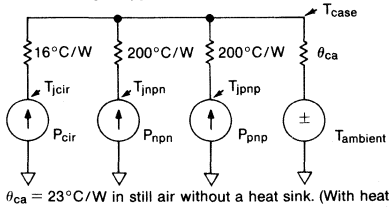
Droop Rate Magnitude vs. Temperature



Equivalent Input Noise



Thermal Model



θ_{ca} = 23°C/W in still air without a heat sink. (With heat sinking or air flow, θ_{ca} will be lower.)

Thermal Model Calculations

$P_{cir} = I_{cc1}[+V_{cc1} - (-V_{cc1})] + I_{cc2}[V_{cc2} - (-V_{cc2})]$
I_{cc1} is the supply current to $\pm V_{cc1}$ (pins 22 and 3).
I_{cc2} is the supply current to $\pm V_{cc2}$ (pins 17 and 12).
Typical values are $\pm V_{cc1} = \pm 15V$, $I_{cc1} = 34mA$, $\pm V_{cc2} = \pm 12V$, $I_{cc2} = 15mA$.
So $P_{cir} = (34mA)(30V) + (15mA)(24V) = 1.38W$

$P_{XXX} = [\pm V_{cc} - V_{out} - I_{col}(R_{col} + 10)]\, I_{col}$ (% duty cycle that XXX is on)
P_{XXX} is the power in either the npn or pnp output transistor.
For $V_{out} > 0$, the power is in the npn and $\pm V_{cc} = +V_{cc}$.
For $V_{out} < 0$, the power is in the pnp and $\pm V_{cc} = -V_{cc}$.
$I_{col} = V_{out}/R_{load}$ or 4mA whichever is greater.
R_{col} is the external resistor between the XXX collector and $\pm V_{cc}$.

Example: $V_{out} = +1V$, 30% duty cycle
$V_{out} = -2V$, 70% duty cycle
$R_{col} = 33\Omega$, $R_{load} = 100\Omega$

$$P_{npn} = \left[15V - 1V - \left(\frac{1V}{100\Omega}\right)\left(33\Omega + 10\Omega\right) \right] \left(\frac{1V}{100\Omega}\right)\left(30\%\right) = 0.041W$$

$$P_{pnp} = \left[-15V - (-2V) - \left(\frac{-2V}{100\Omega}\right)\left(33\Omega + 10\Omega\right) \right] \left(\frac{-2V}{100\Omega}\right)\left(70\%\right) = 0.170W$$

$T_{case} = P_{total}\,\theta_{ca} + T_{ambient} = (P_{cir} + P_{npn} + P_{pnp})\,\theta_{ca} + T_{ambient}$
$T_{cir} = P_{cir}(16°C/W) + T_{case}$
$T_{jnpn} = P_{npn}(200°C/W) + T_{case}$
$T_{jpnp} = P_{pnp}(200°C/W) + T_{case}$

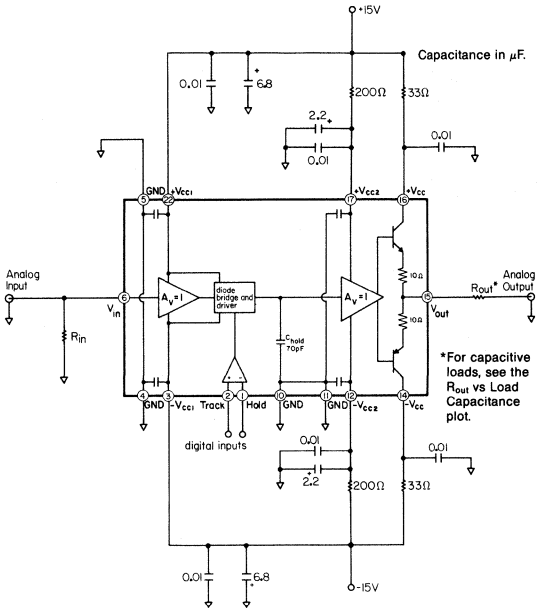


Figure 1: recommended circuit

Layout Considerations

For optimum performance from any precision high-speed track and hold, such as the CLC940, a good printed circuit board layout is necessary. First, provide a ground return path for signal current loops. One such loop is formed between the signal source and the termination resistor at the analog input of the track and hold. Another is formed between the source of the digital sample command and the termination resistors at the digital inputs of the track and hold. In the third such loop, current from the power supplies flows through the track and hold output amplifier to the load and then through the ground return and supply decoupling capacitors to the power supply. Ideally, the input, output, and digital input signals should be transmitted via properly-terminated controlled-impedance transmission lines, such as microstrip or stripline, which work very well on standard printed circuit boards. When a capacitive or high-impedance load makes transmission lines unattractive, just be sure to keep the load within an inch or two of the CLC940 output and provide a wide strip of ground plane for the signal current to return to the decoupling capacitors.

Second, be sure that the ground return paths mentioned above do not cross with themselves or any other ground return on your printed circuit board. Otherwise, signals will be coupled and they will degrade the track and hold precision. For example, to maintain the feedthrough rejection specification, the ground connections of the decoupling capacitors should be kept at least 0.25" away from the signal terminations (such as the ground side of R_{in}).

Third, keep the stray reactance of the decoupling capacitors and termination resistors low. Use surface-mounted multilayer 0.01μF capacitors right at the power supply pins of the CLC940 if possible. If radial lead capacitors are used, be sure that low-loss types with very short leads are used.

Sockets are not recommended, though some low-profile, "bucket"-type sockets work well (see the parts list in Figure 5). Wire wrap methods and boards should not be used. To assist the designer in evaluating the CLC940, an evaluation board is available at minimal cost.

Track/Hold Switching Control

The switch in the CLC940 is controlled by a pair of differential inputs. The device will be in track mode when the voltage on "track," pin 2, is greater than the voltage on "hold," pin 1. Similarly, it will be in hold mode when the voltage on "hold" is greater than that on "track." The best switching action is realized when the slew rate of the digital input is at least 20V/μs and when the differential signal excursion is no less than 300mV. In addition, it is recommended that the differential voltage on these pins not exceed ±2.5V while the absolute voltage on either pin should not exceed ($|V_{cc1}|-11V$). This voltage range accommodates most logic families.

Differential ECL signals may be fed directly to the digital control inputs, each of which represents less than one ECL 10k load. In Figure 2 below, the CLC940 is in track mode when the non-inverting ECL output is high.

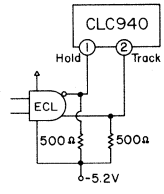


Figure 2: differential ECL control

A single-ended ECL signal can be fed directly into one of the digital inputs while the other pin is biased at −1.4V to accommodate ECL voltage levels. In Figure 3 below, the CLC940 is in track mode when the ECL output is high.

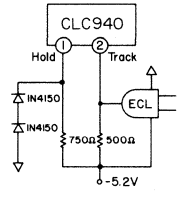


Figure 3: single-ended ECL control

For totem-pole-output TTL, a similar connection scheme is used but with a bias voltage of +1.4V. The digital input represents about 5 LSTTL loads at a high level. In Figure 4 below, the CLC940 is in track mode when the TTL output is high.

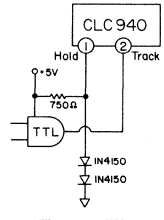


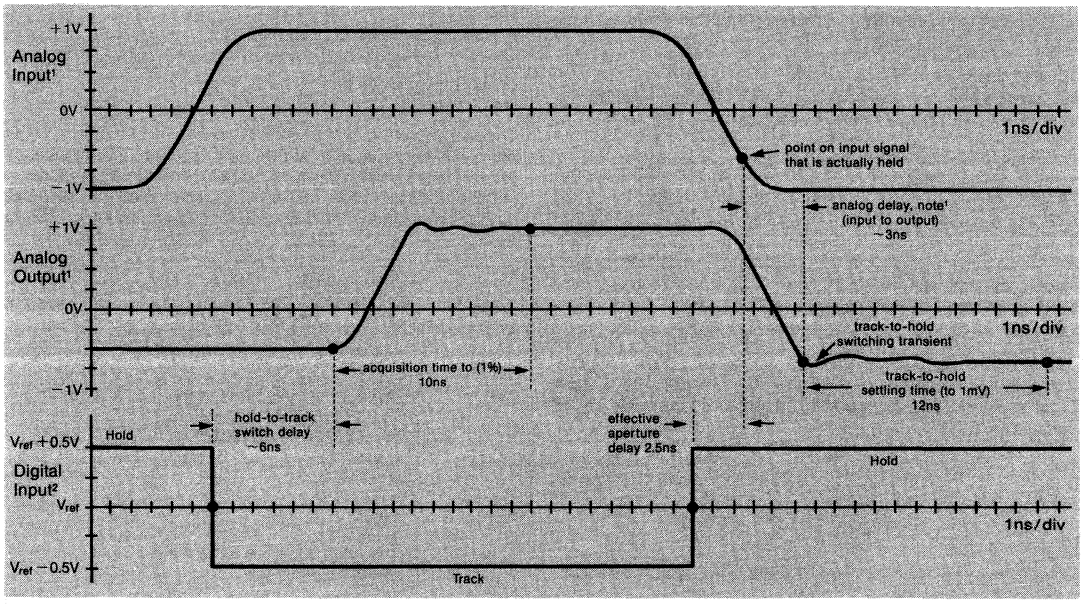
Figure 4: TTL control

Driving Capacitive Loads

In order to maintain performance while driving capacitive loads, a small-value resistor should be placed between the CLC940 output and the load. The optimum value of resistance should be selected from the plot of R_{out} versus Load Capacitance. (See the plot page) For this combination, acquisition time is shown on the Acquisition Time versus Load Capacitance plot. (If the load capacitance is variable, as in some flash A/Ds, the average typical capacitance should be used.)

Track and Hold Terminology

Typical Track and Hold Waveforms



note 1: There is an analog delay of about 3ns from the analog input to the analog output. (The input amplifier contributes 1ns and the output amplifier contributes 2ns.)
note 2: The digital input voltage shown is the voltage applied to "hold," pin 1. "Track," pin 2, is at V_{ref}.

Acquisition Time (hold to track) is the time required for the track and hold to *acquire* the input signal to a specific settling precision when it switches from hold mode to track mode. It is the time from the point when the *output* starts changing to the point when the *output* has settled.

Analog Delay (input to output) is the time required for a signal to travel from the analog input to the analog output. Typically, it is 3ns for the CLC940.

Aperture Jitter or aperture uncertainty is the sample-to-sample variability in Effective Aperture Delay which is caused by a small amount of noise in the switch control circuitry. Aperture Jitter changes the time at which the device goes into hold mode. Coupled with the rate of change (slew rate) of the signal at the storage capacitor, Aperture Jitter causes an error in the held output voltage. (Output voltage error = $\Delta V/\Delta t * \Delta t$, where $\Delta V/\Delta t$ is the slew rate and Δt is the Aperture Jitter.)

Droop Rate is a drift in the held output voltage. It is caused by leakage currents flowing into (or out of) the storage capacitor from the switching circuit and the input stage of the output amplifier.

Effective Aperture Delay tells when the input signal is actually being sampled. It takes into account two delays: 1) the input signal transit time through the input amplifier and 2) the time needed for the switch to open after the part is given the hold command. Typically, the Effective Aperture Delay is 2.5ns which means the held voltage is that which was at the *input* 2.5ns *after* the hold command was given. (Conceivably, Effective Aperture Delay could be negative if the transit time through the input amplifier were longer than the delay in the switch, though this is not the case with the CLC940.)

Feedthrough Rejection or analog input isolation describes how well the switch keeps the input signals from "feeding through" to the output when the device is in hold mode. It is the ratio of the signal that passes through the open switch to the signal at the analog input. Since signal feedthrough is, in part, caused by the capacitance of the switch, Feedthrough Rejection is better for low-frequency input signals (see the plot page for the Feedthrough Rejection vs. Frequency plot). There are, of course, switching transients which feed through from the digital inputs; however, these settle out quickly and are accounted for in the Acquisition Time and Track-to-Hold Settling Time specifications.

Hold-to-Track Switch Delay is the time delay from the track command to the point when the output voltage begins to change as it starts to acquire the new signal. Typically, it is 6ns for the CLC940.

Pedestal Offset or track-to-hold offset is an output offset voltage found in hold mode. (See the Switching Transients and Pedestal plot on the plot page.) It is caused by a small amount of charge injected into (or out of) the storage capacitor when the (diode bridge) switch opens. In practice, this offset is treated just as an output offset voltage. Unlike the Pedestal Offsets of many other high-speed track and holds, the CLC940's Pedestal Offset is virtually unaffected by changes in the analog input voltage.

Track-to-Hold Switching Transient is the switch-induced transient voltage which appears at the output immediately after the device switches from track to hold. (See Track-to-Hold Settling Time and the Switching Transients and Pedestal plot on the plot page.)

Track-to-Hold Settling Time is the time required for the Track-to-Hold Switching Transient to settle out to the point where the output is within 1mV of its final value. (See Track-to-Hold Switching Transient and the Switching Transients and Pedestal plot on the plot page.)

Lower Power Operation

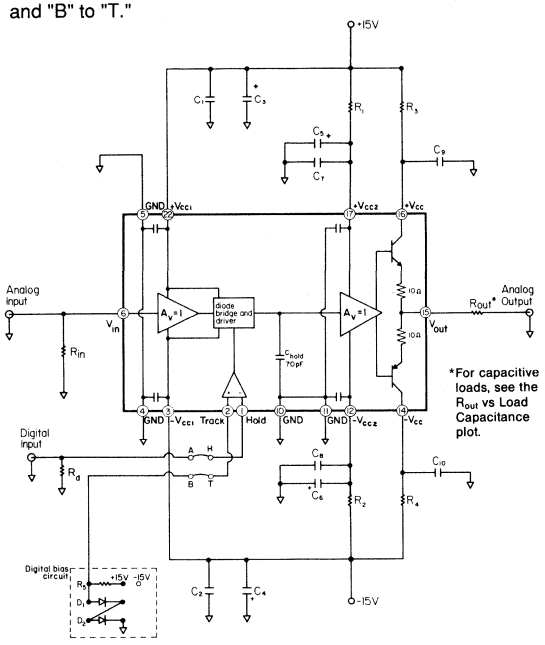
The power dissipation in the output stage transistors may be decreased by reducing the *output-stage* supply voltages, $\pm V_{cc}$, to as low as $\pm 5V$. This only minimally affects performance, yet can substantially reduce output transistor junction temperatures (see the thermal model).

CLC940 Evaluation Board

An evaluation board (part number 730011) is available for the CLC940. The board is user-configurable for either TTL or ECL operation. (See Figure 5)

On the board near pin 1 of the CLC940 are four points labeled "A", "H", "B", and "T." (See Figure 5 and Figure 6.) Jumpers are connected between these points to provide the CLC940 with the bias voltages needed for single-ended ECL and TTL. Points "H" and "T" go to the "hold" and "track" inputs, respectively. Point "A" goes to the "digital input," and "B" goes to the TTL/ECL bias network.

The connection scheme for TTL requires that the bias network provide +1.4V at point "B." The +15V supply is used and the diodes are inserted so as to be forward biased. (See Figures 4 and 5.) Jumpers are used to connect "A" to "H" and "B" to "T."



For TTL, use the bias circuit shown. Omit R_d.

For single-ended ECL, reverse the direction of the diodes and connect R_5 to $-15V$ instead of $+15V$. Omit R_d.

For differential ECL, **omit** the jumper connections "A" to "H" and "B" to "T." Omit bias circuit. Make connections directly to "H"and "T."

Figure 5: evaluation board schematic (configured for TTL operation) and parts list

Parts List

Resistors:

R_1	200Ω	R_3	33Ω	R_5	2.6kΩ	R_{out}	*	*selected for desired input/ output impedance
R_2	200Ω	R_4	33Ω	R_{in}	*	R_d	*	

Capacitors: (35V, +80%|−20%)

C_1	0.01μF ceramic radial lead	C_6	2.2μF (Sprague 150D series)
C_2	0.01μF ceramic radial lead	C_7	0.01μF ceramic radial lead
C_3	6.8μF (Sprague 150D series)	C_8	0.01μF ceramic radial lead
C_4	6.8μF (Sprague 150D series)	C_9	0.01μF ceramic radial lead
C_5	2.2μF (Sprague 150D series)	C_{10}	0.01μF ceramic radial lead

Diodes:

D_1	1N4150
D_2	1N4150

Hardware: (optional)

SMA connectors Amphenol 901-144 (straight) or Amphenol 901-143 (angled)

"Socket" Cambion flush mount connector jacks 450-2598-01-06-00

Single-ended ECL is connected similarly, however the bias network should be configured to provide −1.4V at point "B." The −15V supply is used and the diodes are inserted so as to be forward biased. (See Figures 3 and 5.) Jumpers are used to connect "A" to "H" and "B" to "T."

For differential ECL, signals can be sent directly to points "H" and "T," the "hold" and "track" inputs respectively. The bias circuit and jumper connections should be omitted. (See Figures 2 and 5.)

The resistor at the digital input, R_D, is omitted for TTL and ECL, but is otherwise used to set the (digital) input impedance. The resistor at the analog input, R_{in}, is selected for the desired input impedance. The output resistor, R_{out}, is selected for the desired output impedance and for optimum capacitive-load performance. (See the R_{out} vs Load Capacitance plot on the plot page.)

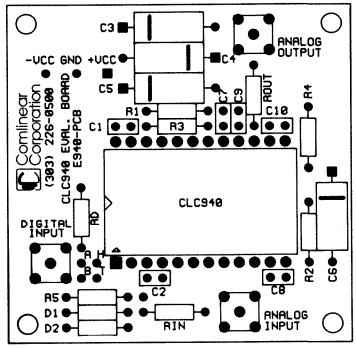


Figure 6: component placement guide

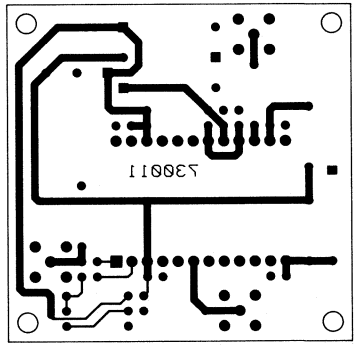


Figure 7: solder side (bottom) as viewed from component side (top)

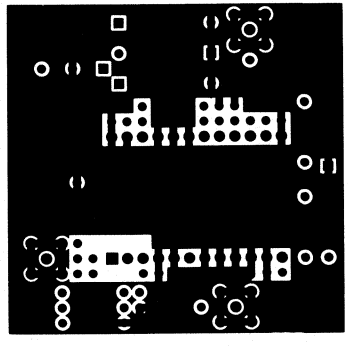


Figure 8: component side (top) showing extensive ground plane

Comlinear Corporation

12-Bit, Fast Sampling Wideband Track-and-Hold

CLC942

APPLICATIONS:

- flash A/D driver
- high-resolution, subranging A/D driver
- signal deglitching (as in CCD or D/A systems)
- communication systems
- radar and IF processors

FEATURES (typical):

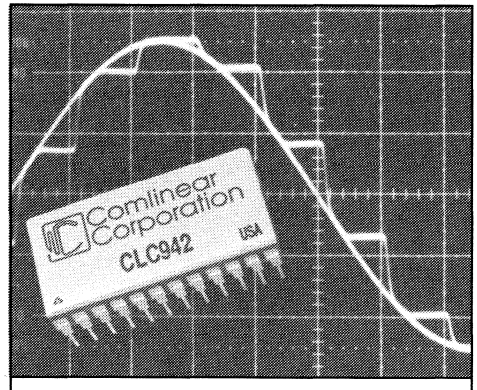
- 25ns hold-to-track acquisition time (0.01%)
- 5ns track-to-hold settling time
- 1.4ps aperture jitter
- 70MHz small-signal bandwidth
- 78dB feedthrough rejection
- ECL control signal

DESCRIPTION:

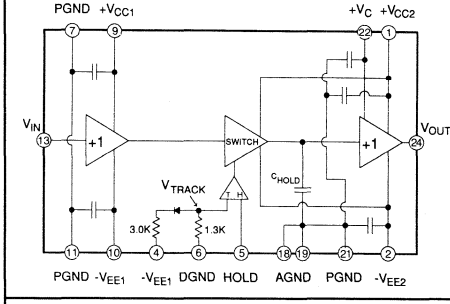
The CLC942 is a 12-Bit accurate, fast sampling, wideband track-and-hold amplifier which offers 5ns switching performance. Closed-loop monolithic buffers ensure that switching accuracy is fully realized. The CLC942 is an improved alternate source for the HTS-0010 and the SHC600.

The CLC942 is an ideal device for driving flash A/D's, especially those configured in high resolution, subranging architectures. The 25ns hold-to-track acquistion time (0.01%) and very fast 5ns track-to-hold settling time permit the high sampling rates needed in applications such as radar and communications. Other specifications, such as the 1.4ps aperture jitter, 15mV pedestal offset, and -74dBc harmonic distortion are similarly supportive of A/D system performance goals. The CLC942 is fully compatible with demanding flash A/D input requirements as demonstrated by its ±2.2V output range and its ability to drive up to 90pF loads.

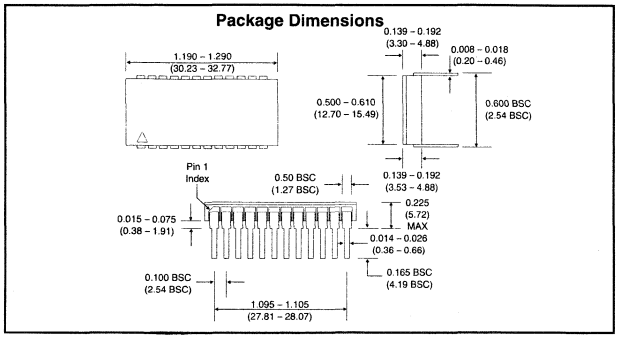
The CLC942 is constructed using thin film resistor/bipolar transistor technology as well as custom integrated circuits. The CLC942AI is specified over a temperature range of -25°C to +85°C, while the CLC942AM is specified over a range of -55°C to +125°C. Both devices are packaged in a 24-pin, 600 mil wide, ceramic DIP.



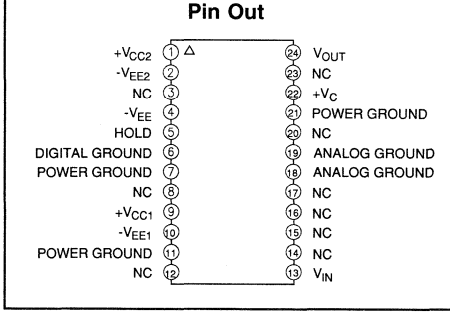
Equivalent Circuit



Package Dimensions



Pin Out



Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

Electrical Characteristics ($+V_{CC1,2}$=+5.0V; $-V_{EE1,2}$=-5.0V; $+V_C$=+15V; R_L=100Ω; unless otherwise specified)

PARAMETER[1]	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC942A8	+25°C	-55°C	+25°C	+125°C		
Ambient Temperature	CLC942AI	+25°C	-25°C	+25°C	+85°C		
TRACK-MODE DYNAMICS							
*-3dB bandwidth		70	40	50	50	MHz	SSBW
slew rate		300	220	250	220	V/μs	SR
2nd harmonic distortion	$2V_{pp}$; 4MHz; R_L=1kΩ	-74	-62	-65	-65	dBc	HD2A
	$2V_{pp}$; 20MHz; R_L=1kΩ	-50	-38	-44	-43	dBc	HD2
3rd harmonic distortion	$2V_{pp}$; 4MHz; R_L=1kΩ	-75	-70	-72	-70	dBc	HD3A
	$2V_{pp}$; 20MHz; R_L=1kΩ	-64	-54	-55	-43	dBc	HD3
HOLD-MODE DYNAMICS							
*droop rate		20	450	230	3000	μV/μs	DR
*feedthrough rejection	20MHz, $V_{IN}=2V_{pp}$	78	70	72	70	dB	FTR
TRACK-TO-HOLD SWITCHING							
*effective aperture delay		-1.5	-3	-4	-6	ns	TA
*aperture jitter		1.4	2.0	2.0	2.0	ps_{rms}	UHD
*pedestal offset		8	12	12	15	mV	PO
temperature coefficient	endpoint average	10	40	40	40	μV/°C	DPO
sensitivity to supply	(-5.0V)	3	6	6	6	mV/V	PORR
switching transient peak-to-peak amplitude	f_S=2MHz	8	13	13	16	mV_{pp}	HTA
track-to-hold settling time	to 1mV	5	13	7	8	ns	HTS
HOLD-TO-TRACK SWITCHING							
acquisition time to 0.1%	$V_{IN}=2V_{pp}$, R_L=100Ω	20	31	24	32	ns	ATS
to 0.01%		25	36	31	36	ns	ATSP
DC ACCURACY							
*gain	1kHz, $4V_{pp}$, no load	0.997	0.993	0.995	0.995	V/V	G
temperature coefficient		15	40	40	40	ppm/°C	DG
non-linearity		0.005	0.025	0.020	0.020	%	GNL
*offset voltage		15	55	40	50	mV	VIO
temperature coefficient	endpoint average	50	150	150	150	μV/°C	DVIO
*power supply rejection ratio		52	40	45	45	dB	PSRR
DIGITAL INPUT							
differential input threshold	$\|V_{TRACK}-V_{HOLD}\|$ (min.)		250	250	250	mV	VDIF
input bias current	logic HIGH	15	60	30	35	μA	IIH
	logic LOW	35	125	65	65	μA	IIL
ANALOG INPUT							
input voltage range[2]			±2.2	±2.2	±2.2	V	VI
input resistance		150	50	85	85	kΩ	RIN
input capacitance		3.5	5.5	5.5	5.5	pF	CIN
*input bias current		10	34	34	34	μA	IB
ANALOG OUTPUT							
*output resistance	at 1kHz	0.2	0.5	0.5	0.5	Ω	RO
POWER REQUIREMENTS							
*supply current ($+V_{CC1}$ and $+V_{CC2}$)	V_{IN}=0V, track mode, no load	50	64	64	64	mA	ICC
*supply current ($-V_{EE1}$ and $-V_{EE2}$)	V_{IN}=0V, track mode, no load	65	81	81	81	mA	IEE
*supply current ($+V_C$)	V_{IN}=0V, track mode, no load	15	17	17	18	mA	I15
power dissipation	V_{IN}=0V, track mode, no load	0.80	0.98	0.98	0.995	W	PD

NOTES:
1. Parameters preceded by an * are the final electrical test parameters and are 100% tested. A8C units are tested at – 55°C, + 25°C, and + 125°C. AI units are tested only at + 25°C, although their performance is guaranteed at – 25°C and + 85°C as indicated above.
2. For optimum performance, differential voltage between the input and the output should not exceed 3V in HOLD mode.
3. Absolute Maximum Ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
4. Junction-to-Case temperature rise is approximately 16°C; θ_{CA} = 35°C/W.

Recommended Operating Conditions

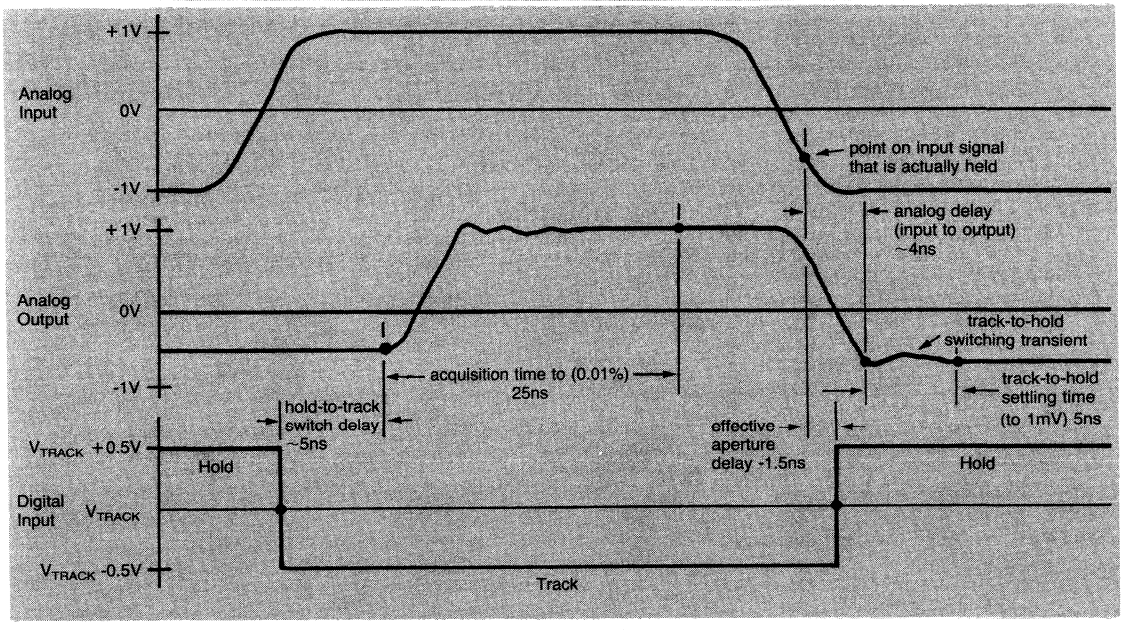
supply voltage:	
$+V_{CC1}$ and $+V_{CC2}$	+5.0V(+4.5V min)
$-V_{EE1}$ and $-V_{EE2}$	-5.0V(-4.5 min)
$+V_C$	+11.0V to +15.75V
$-V_{EE}$	-5.0V±5%
analog to digital ground differential	10mV
analog input voltage range[2]	±2.2V
input to output differential voltage	3V
HOLD input voltage range	-0.75 to -1.9V
HOLD to V_{TRACK} differential voltage	0.6V
HOLD signal rise/fall time	<16ns

Absolute Maximum Ratings[3]

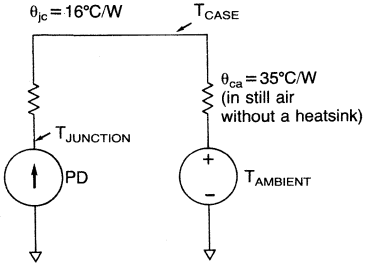
supply voltage:	
$+V_{CC1}$ and $+V_{CC2}$	0V to 7.0V
$-V_{EE1}$ and $-V_{EE2}$	-7.0V to 0V
$+V_C$	+20V
$-V_{EE}$	-7.0V to +3.0V
analog to power ground differential	200mV
analog input voltage range	$-V_{EE1}$ to + V_{CC1}
V_{TRACK} and HOLD voltage range	(V_{EE1} +2V) to (V_{CC1}-2V)
output current	±50mA continuous
power dissipation[4]	see thermal model
junction temperature	+175°C
operating temperature range	AI: -25°C to +85°C
	AM: -55°C to +125° C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec.

Comlinear reserves the right to change specifications without notice.

Typical TRACK-and-HOLD Waveforms



Thermal Model



$PD = |(I_{CC})\ (V_{CC})| + |(I_{EE})\ (V_{EE})|$

$\theta_{ca} = \theta_{cs} + \theta_{sa}$ (with heatsink)

Where θ_{sa} = Heatsink-to-Ambient (°C/W);
θ_{cs} = Case-to-Heatsink (°C/W)

and usually $\theta_{sa} >> \theta_{cs}$,

therefore θ_{ca} (with heatsink) $\approx \theta_{sa}$

$T_{junction} = T_{ambient} + (\theta_{jc} + \theta_{ca})\ PD = T_{ambient} + (\theta_{ja})\ PD$

where $\theta_{ja} = \theta_{jc} + \theta_{ca}$

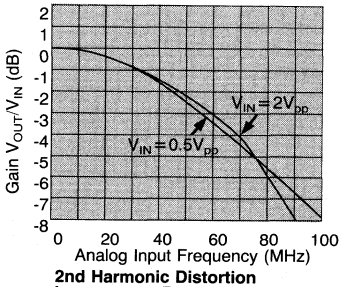
or

$T_{junction} = T_{case} + (\theta_{jc})\ PD$,

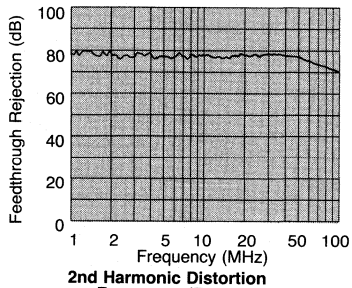
where in either case $T_{junction} < T_{junction}$ (max)

Typical Performance Characteristics (T_A =+25 C; R_L=100Ω; $+V_{CC1,2}$=+5.0V; $-V_{EE1,2}$=-5.0V; $+V_C$=+15V)

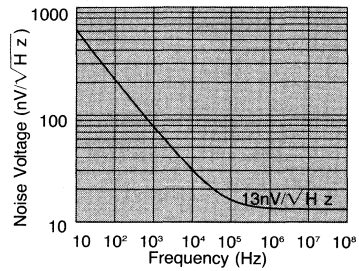
Voltage Gain vs. Frequency



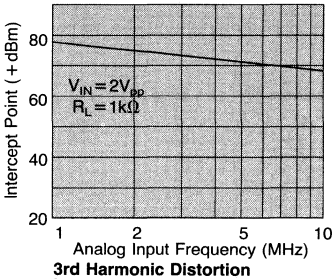
Feedthrough Rejection vs. Frequency



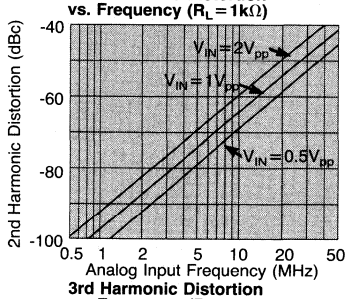
Equivalent Input Noise Voltage



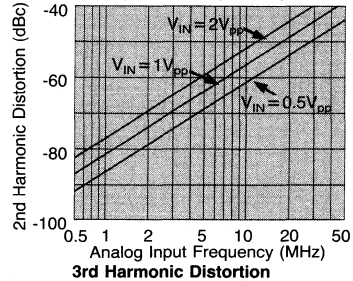
2nd Harmonic Distortion Intercept vs. Frequency



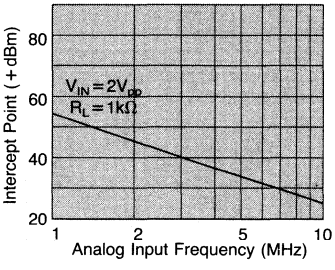
2nd Harmonic Distortion vs. Frequency (R_L=1kΩ)



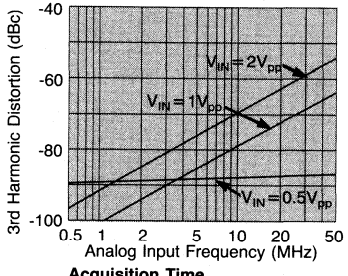
2nd Harmonic Distortion vs. Frequency (R_L=100Ω)



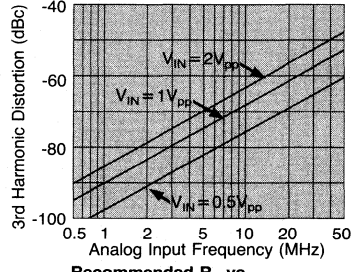
3rd Harmonic Distortion Intercept vs. Frequency



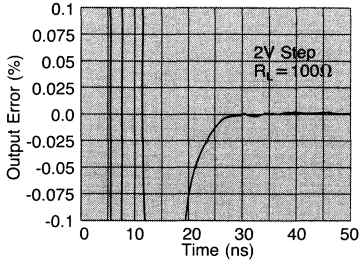
3rd Harmonic Distortion vs. Frequency (R_L=1kΩ)



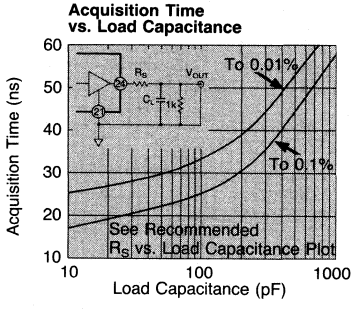
3rd Harmonic Distortion vs. Frequency (R_L=100Ω)



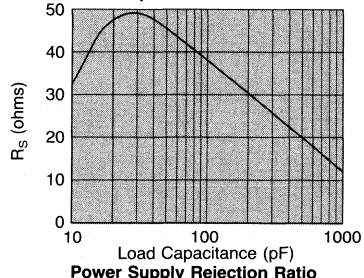
Acquisition Time



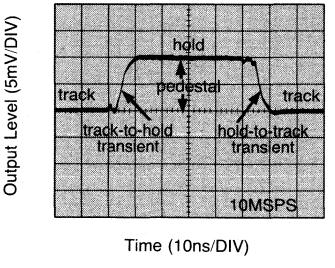
Acquisition Time vs. Load Capacitance



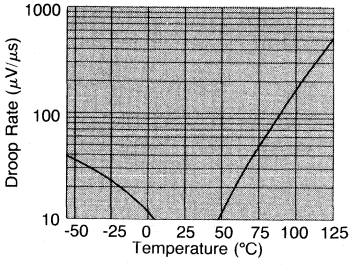
Recommended R_S vs. Load Capacitance



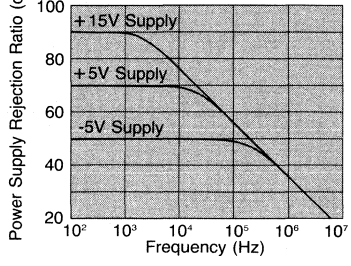
Switching Transients and Pedestal



Droop Rate vs. Temperature



Power Supply Rejection Ratio vs. Frequency



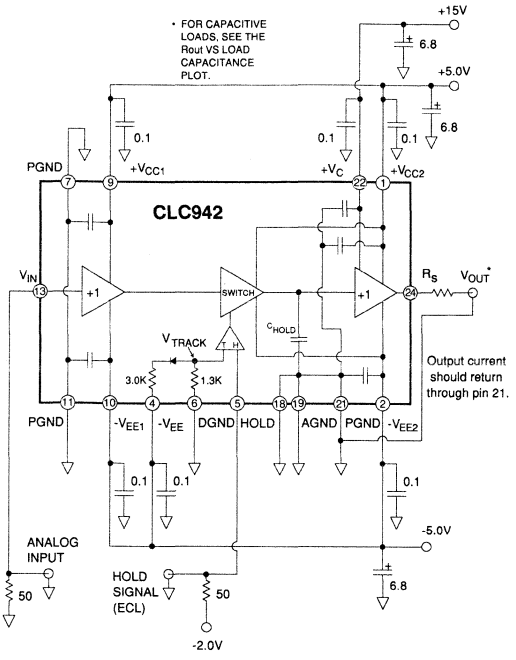


Figure 1: recommended CLC942 application circuit

Layout Considerations

For optimum performance from any precision, high-speed, track-and-hold, such as the CLC942, a high-quality printed circuit board layout is required. The main facet of the printed circuit board is a substantial ground plane around and under the CLC942. The ground plane will serve two main purposes, that of partially shielding the CLC942 from other system signals, as well as providing both power supply and signal return paths.

The input and output signals of the CLC942 should be controlled impedance transmission line such as stripline or micro-stripline for optimum performance (including the use of surface-mount termination components). In any case, as much attention must be paid to the ground return path as to the signal path itself. In general, a ground path at least 250 mils wide should provide an adequate ground return, but the stripline techniques are strongly recommended for high-frequency applications.

All supply lines to the CLC942 should be individually decoupled with 0.1μF capacitors. These decoupling capacitors should be located as close to the supply pins as possible. In addition, the decoupling capacitor lead lengths must also be kept to a minimum to avoid any effects from lead inductance. A better solution is the use of chip capacitors located right at the supply pins.

The use of sockets is not recommended with the CLC942, in that they tend to increase lead-to-lead capacitance as well as lead inductance, both degrading performance. If sockets must be used, low-profile Teflon types or individual "pin" sockets are preferred.

Track/Hold Switching Control

At the heart of the CLC942 is an active bipolar transistor bridge circuit. This bridge circuit allows the input signal to pass through to the HOLD capacitor during the signal acquisition mode, and isolates the HOLD capacitor during the HOLD mode. A differential driver circuit determines the state of the bridge circuit, either "open" or "closed."

In normal mode, only the HOLD side of the bridge driver circuit is used. With the resistor diode network between pins 4 and 6 of the CLC942 bias as in figure 1, the HOLD input (pin 5) responds to standard 10K and 10KH ECL signals. At room temperature, 100K ECL logic family devices may also work with the CLC942, but their use is not guaranteed nor recommended.

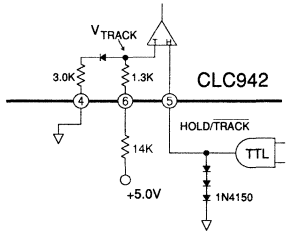


Figure 2: TTL compatible driver circuit

By re-biasing the resistor/diode network between pins 4 and 6, the CLC942 will respond to standard TTL level logic families (Figure 2). The resistors tied to pin 6 and +5.0V, effectively raises the internal threshold level to +1.4V for use with TTL compatible devices. The three series diodes on pin 5 provide over-voltage protection for the inputs of the bridge driver circuit. For optimum dynamic performance from the CLC942, use of the more modern TTL families is recommended, such as the "AS" or "F" series.

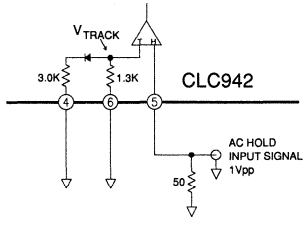
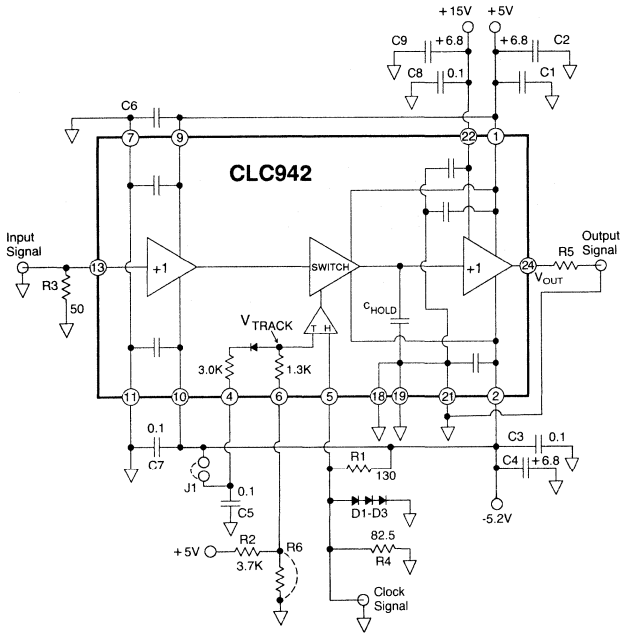


Figure 3: "ground" referenced driver circuit

The resistor/diode network can be further modified for operation with "ground" referenced ac signals. Figure 3 illustrates the required connections, which amount to connecting both pins 4 and 6 to ground. The CLC942 will then operate from a 1.0V_{pp} HOLD input signal. With the 50Ω input termination resistor, the HOLD control signal can be either dc or ac coupled.

CLC942 Evaluation Board

An evaluation board (part number 730017) is available for the CLC942. The board is user-configurable for either TTL, ECL, or "ac-signal" control. Operational details are available below.



CLC942 Evaluation Board Schematic

Configuration Table

Mode	D1-D3	J1	R1	R2	R4	R6
ECL	none	short	130	NC	82.5	short
TTL	used	open	open	3.9k	open	1.5k
GND Ref.	none	open	open	NC	50	short

NC – Not Critical

Parts List

Resistors:

R1	130Ω
R2	3.9kΩ
R3	50Ω (suggested)
R4	82.5Ω/50Ω
R5	see "Recomm. R_S" plot
R6	1.5kΩ

Diodes:

D1-D3 1N4150

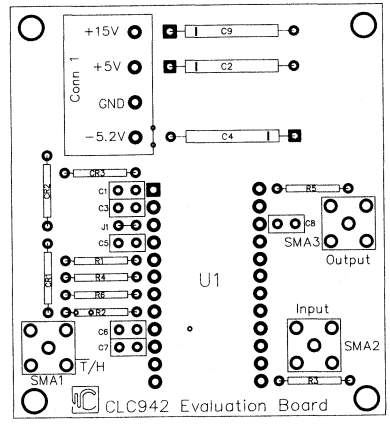
Capacitors: (35V, +80%|-20%)

C1	0.1μF ceramic radial lead
C2	6.8μF(Sprague 150D Series)
C3	0.1μF ceramic radial lead
C4	6.8μF(Sprague 150D Series)
C5	0.1μF ceramic radial lead
C6	0.1μF ceramic radial lead
C7	0.1μF ceramic radial lead
C8	0.1μF ceramic radial lead
C9	6.8μF(Sprague 150D Series)

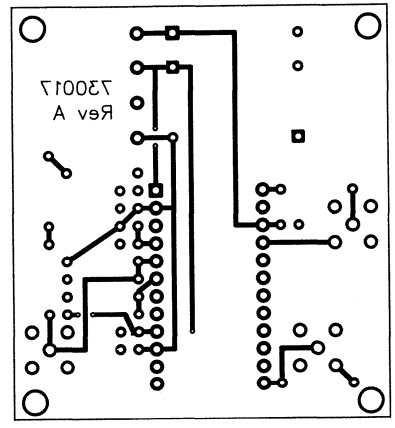
Hardware: (Optional)

SMA Connectors
Amphenol 901-144 (straight)
Amphenol 901-143 (angled)

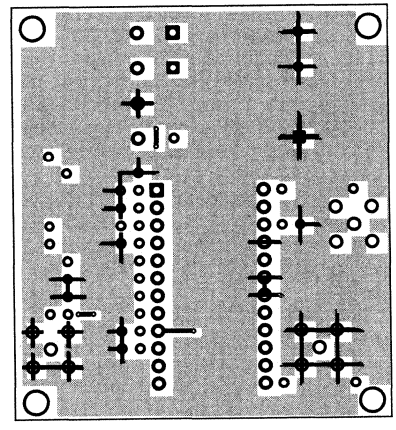
"Sockets"
Cambion flush mount connector jacks
450-2598-01-06-00



Component Placement Guide



Solder Side (viewed from top)



Component Side (viewed from top)

Analog-to-Digital Converters

Contents

Comlinear Corporation

Dual Supply, 12-Bit, 10MSPS A/D Converter

CLC922

APPLICATIONS:

- radar processing
- FLIR processing/electronic imaging
- instrumentation
- medical imaging
- transient signal recorders

FEATURES (typical):

- 66.6dB spurious free signal range; $f_{IN} = 5MHz$
- no missing codes guaranteed
- 0.35LSB differential linearity
- small package ($2.28in^2$)
- low power dissipation 4W

DESCRIPTION:

The CLC922 is a 12-bit analog-to-digital converter subsystem, including 12-bit quantizer, internal track-and-hold, reference circuitry and error correction circuits. The CLC922 has been specifically designed to operate from dual supplies, +5V and −5.2V. Constructed using advanced thin-film technology, the CLC922 is built in a fully certified MIL-STD-1772 facility.

The CLC922 incorporates a complete two-pass subranging architecture, constructed from several high-speed building blocks. A broadband (70MHz) input amplifier buffers input signals and provides an accurate drive signal to the on-board track-and-hold. Laser trimmed gain and offset circuits assure accurate matching unit to unit, while also offering broad flexibility in both gain and offset adjustment. Gain adjustment range is ±10%, with the $2V_{PP}$ input range adjustable over a +1V to −2V range. The latched outputs of the CLC922 mean that only a convert clock, analog input and power supplies are required for operation; internal logic generates all required timing signals.

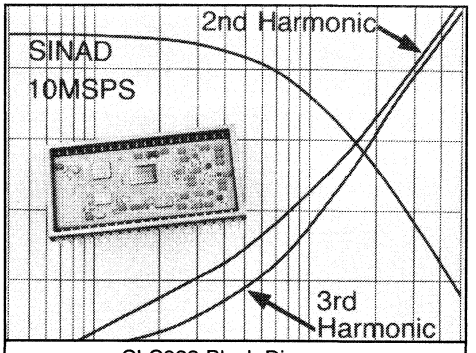
Comprehensive dynamic testing on every part ensures that system performance goals will be met. The spurious-free-signal-range of 73.5dB@404kHz and 66.6dB@4.99MHz give an effective dynamic range of 12.0 bits and 10.8 bits respectively. This, coupled with an SNR specification of 66.6dB@4.99MHz, means that the CLC922 is ideally suited for use in areas like radar, instrumentation, and medical signal processing.

The CLC922BI is specified over a temperature range of −25°C to +85°C, while the CLC922B8C is specified over a range of −55°C to +125°C. Both devices are packaged in 40-pin, 1.1 inch wide, ceramic DIP's (note: leads are side brazed for easy access and inspection).

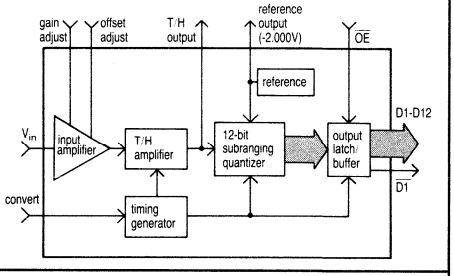
Contact factory for DESC SMD number.

Ordering Information		
CLC922BI	−25°C to +85°C	industrial version
CLC922B8C	−55°C to +125°C	HIREL version MIL-STD-883, Class B

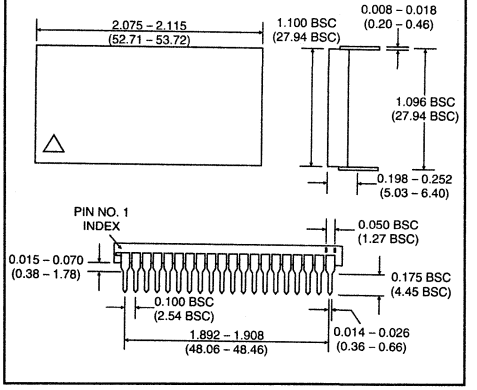
All versions of the CLC922 are manufactured in Comlinear's MIL-STD-1772 certified factory in Fort Collins, Colorado, U.S.A.



CLC922 Block Diagram



Package Dimensions



Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

DS922.01

January 1993

Electrical Characteristics ($+V_{CC} = +5.0V$; $-V_{EE} = -5.2V$; unless specified)

PARAMETER[1]	CONDITIONS		TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Case Temperature	CLC922B8C		+25°C	-55°C	+25°C	+125°C		
Case Temperature	CLC922BI		+25°C	-25°C	+25°C	+85°C		
DYNAMIC CHARACTERISTICS								
small signal bandwidth	$V_{IN} = 1/4$ FS		70	50	50	50	MHz	SSBW
large signal bandwidth	$V_{IN} =$ FS		65	45	45	45	MHz	LSBW
slew rate			300	250	250	230	V/μs	SR
overvoltage recovery time	$V_{IN} = 2$FS		26	38	38	38	ns	OR
effective aperture delay			1.2	3.0	2.5	3.0	ns	TA
aperture jitter			4.5	7.0	6.0	6.0	ps(RMS)	AJ
NOISE AND DISTORTION (10MSPS)								
* signal-to-noise ratio								
(not including harmonics)	404kHz;	FS	67.5	64.5	65	65	dB	SNR1
	4.996MHz;	FS	66.6	63.5	65	65	dB	SNR2
*in-band harmonics	404kHz;	FS-1dB	−73.5	−60	−63.5	−64	dBc	IBH1
	4.996MHz;	FS-1dB	−66.6	−58	−61.5	−60	dBc	IBH2
*total harmonic distortion	404kHz;	FS-1dB	−70.2	−59	−63	−63	dBc	THD1
	4.996MHz;	FS-1dB	−62.8	−57	−60	−57	dBc	THD2
*signal-to-noise-and distortion								
(including harmonics)	404kHz;	FS-1dB	65	58.5	61	61	dB	SND1
	4.996MHz;	FS-1dB	62	57	59	56.5	dB	SND2
*spurious-free-signal-range								
(SFSR)	404kHz;	FS-1dB	73.5	60	63.5	64	dB	SFSR1
	4.996MHz;	FS-1dB	66.6	58	61.5	60	dB	SFSR2
*effective bits								
(based on SFSR)	404kHz;	FS-1dB	11.9	9.67	10.25	10.33	bits	SFEB1
	4.996MHz;	FS-1dB	10.7	9.34	9.92	9.67	bits	SFEB2
*effective bits								
(based on SINAD)	404kHz;	FS-1dB	10.50	9.42	9.84	9.84	bits	EB1
	4.996MHz;	FS-1dB	10.00	9.17	9.50	9.09	bits	EB2
DC ACCURACY and PERFORMANCE								
* differential non-linearity	dc; FS		0.35	1.0	1.0	1.0	LSB	DNL
*integral non-linearity	ds; FS		1.2	4.0	4.0	4.0	LSB	INL
*missing codes			0	0	0	0	codes	MC
*bipolar offset error			3.4	30	10	12	mV	VIO
temperature coefficient				300		150	μV /°C	DVIO
*bipolar gain error			0.3	2.7	1.0	1.5	%FS	GE
temperature coefficient				0.035		0.010	%FS /°C	DGE
reference voltage output			−2.000				V	VREF
ANALOG INPUT PERFORMANCE								
+ analog input bias current			10	45	25	35	μA	IBN
+ temperature coefficient			100	250	—	100	nA /°C	DIBN
analog input resistance			80	>25	>50		kΩ	RIN
analog input capacitance			3.5	5.5	5.5	5.5	pF	CIN
POWER REQUIREMENTS								
*supply current ($+V_{CC} = +5.0V$)	10MSPS; no load		343	440	415	390	mA	ICC
*supply current ($-V_{EE} = -5.2V$)	10MSPS; no load		454	700	630	550	mA	IEE
nominal power dissipation	10MSPS; no load		4.08				W	PD

Note 1: Parameters preceded by an * are the final electrical test parameters and are 100% tested. B8C units are tested at – 55°C, + 25°C, and + 125°C. Parameters preceded by a + are 100% tested on B8C units only. BI units are tested only at + 25°C although their performance is guaranteed at – 25°C and + 85°C as indicated above.

Note 2: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3: Junction temperature rise above case ≈ 16°C; θ_{ca} = 16°C/W; θ_{ca} = 7°C/W @ 500LFPM, (Use of a SIL-PAD® #550007, from Berquist (800-347-4572), can lower case-to-ambient rise; θ_{ca} = 12°C/W @ still air – 12in² ground-plane; θ_{ca} = 3.4°C/W @ 100LFPM – 12in² ground plane.)

Electrical Characteristics ($+V_{CC}$ = +5.0V; $-V_{EE}$ = -5.2V; unless specified)

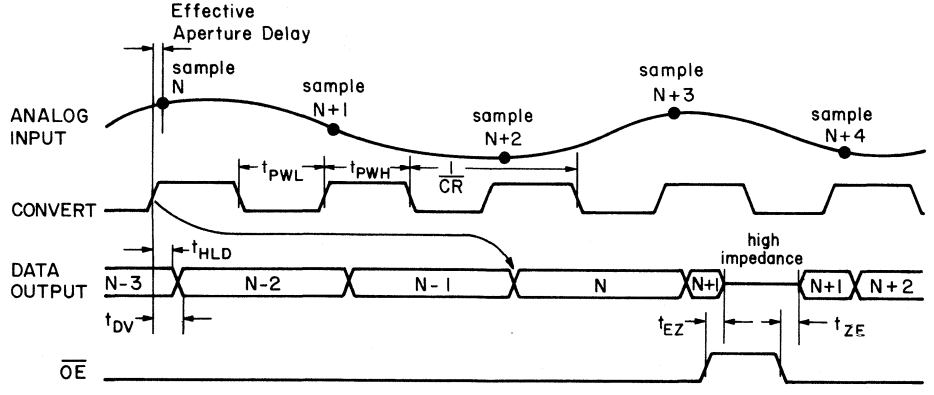
PARAMETER[1]	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Case Temperature	CLC922B8C	+25°C	-55°C	+25°C	+125°C		
Case Temperature	CLC922BI	+25°C	-25°C	+25°C	+85°C		
DIGITAL INPUTS							
+ input voltage	logic low		0.8	0.8	0.8	V	VIL
	logic high		2.0	2.0	2.0	V	VIH
+ input current	logic low	−0.5	−2.8	−2.8	−2.8	mA	IIL
	logic high	40	350	350	350	μA	IIH
DIGITAL OUTPUTS							
+ output voltage	logic low, IOL = 4mA	0.2	0.5	0.5	0.5	V	VOL
	logic high, IOH = 400μA	3.2	2.4	2.4	2.4	V	VOH
+ output leakage current, high impedance	logic low	5	150	150	150	μA	IOZL
	logic high	5	150	150	150	μA	IOZH
TIMING							
maximum conversion rate			10	10	10	MSPS	CR
minimum conversion rate		0				MSPS	CRM
data hold time		13	9	10	10	ns	THLD
output propagation delay		24	35	35	40	ns	TDV
OE LOW to enabled output		19	30	30	30	ns	TZE
OE HIGH to high impedance		12	30	30	30	ns	TEZ

Recommended Operating Conditions

positive supply voltage ($+V_{CC}$) +5V±5%
negative supply voltage ($-V_{EE}$) −5.2V±5%
differential voltage between any two GNDs 10mV
analog input voltage range $2V_{pp}$ (within +1V to −2V)
maximum V_{REF} output current 2mA
minimum CONVERT pulse width HIGH (t_{PWH}) 30ns
minimum CONVERT pulse width LOW (t_{PWL}) 40ns
digital input voltage range 0V to $+V_{CC}$

Absolute Maximum Ratings[2]

positive supply voltage ($+V_{CC}$) +7.0V
negative supply voltage ($-V_{EE}$) −7.0V
differential voltage between any two GNDs 200mV
analog input voltage range $-V_{EE}$ to $+V_{CC}$
V_{REF} output current 20mA
CONVERT and OE input voltage range 0V to $+V_{CC}$
gain and offset adjust voltage range $-V_{EE}$ to $+V_{CC}$
output short circuit duration (one pin to ground) Infinite
Junction Temperature[3] +175°C
Operating Temperature Range (Case)
BI −25°C to +85°C
B8C −55°C to +125°C
Storage Temperature Range −65°C to +150°C
Lead Solder Duration (+300°C) 10 sec



Understanding A/D Dynamic Specifications

Analog-to-Digital converters are specified in many ways. As a component achieves higher performance, its specifications and their definitions can become more critical. Fortunately, the vast number of converter applications can generally be placed into one of two classes. These are processed data and non-processed data applications. The distinction seems quite simple but the split implies a completely different approach in specifying A/D converters for a given application.

The processed data area includes the frequency domain applications which employ Fourier processing (FFT). Also in this category are the highly averaged applications, usually concerned with low noise. In each case, the converter's data is averaged or convolved mathematically. This processing reduces the apparent noise level in the output data. For FFTs, the noise is simply spread over a large number of frequency bins. For simple averaging approaches, the gaussian distribution of noise is greatly reduced, appearing to increase the converter's resolution. Processed applications include radar, network and spectrum analyzers, communications receivers, etc.

The non-processed applications tend to take the converter's data in its original form with very little processing. This means that the noise reduction benefits of the processed applications are not seen. The non-processed area is composed primarily of time domain applications like imaging, DSO's, ultrasound, etc.

The processed vs. non-processed issue has several implications in terms of converter specifications. For the non-processed (time domain) systems the dominant converter specifications deal with noise (SNR) and converter accuracy (DNL). The converter's quantization noise and input stage noise dominate converter accuracy . The harmonic distortion (primarily INL) of the converter is generally of little interest given that most time domain applications present data for visual analysis and tend to focus on "local" accuracy rather than over the full input range. "Local" accuracy is best described through the standard noise measurements, such as SNR and DNL.

In the frequency domain application areas, the noise of the converter is processed to the point where, for almost all systems, it is no longer of issue. This is manifested as a reduction in the apparent noise floor. The actual RMS noise is not reduced, but is spread over more and more frequency bins as processing levels are increased. Unfortunately, the harmonic distortion performance of the converter is not affected by increased processing. This makes the harmonic performance, or more specifically the spurious performance, the dominant error source for frequency domain applications. SFSR becomes the dominant specification for determining converter performance in the frequency domain.

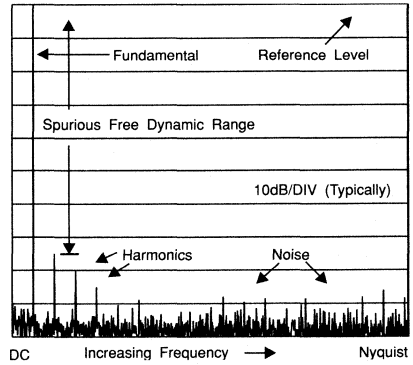
Signal-to-Noise Ratio (SNR) is the ratio of the power contained in the fundamental signal compared to the power contained in the entire noise floor. That is to say all individual noise components are added together to arrive at an integrated noise power. For SNR, harmonic power is excluded from the noise measurement. SNR is particularly important in time domain applications like digital image processing and infrared imaging, where conversion accuracy can be heavily degraded by integrated noise.

Signal-to-Noise-and-Distortion (SINAD) is the ratio of the fundamental signal power to the power at all other frequencies. This includes all noise as well as all harmonics. SINAD is a worst case specification for A/D converters, combining variables from both frequency and time domains. The value of SINAD in high-performance converter applications is not clear since it does not accurately predict the best converter for a given application. Because applications tend to fall into time domain/non-processed or frequency domain/processed applications, those specifications more directly related to the application should be the primary focus in selecting the converter.

Total Harmonic Distortion (THD) is the combined power of a specified number of harmonics, compared to the power of the fundamental signal. Harmonics are located at predictable frequencies, spaced at integer multiples of the fundamental signal. For example, a 1MHz fundamental would generate harmonics at 2MHz, 3MHz, 4MHz, ... and so on. In practice, only the first five harmonics contribute significantly to THD, although more may be included in the measurement. THD does not tend to apply well in frequency domain applications which are by their nature very SFSR oriented. In time domain applications, THD is indicative of full-scale input range distortion, however the high-performance time domain applications are generally most interested in local distortion performance. Local distortion and accuracy is dominated by DNL. The use of THD for applications requiring local performance is not likely to yield accurate or repeatable results in selecting the correct converter.

Spurious-Free-Signal-Range (SFSR) is the "clean" dynamic range of the converter, free from harmonic and spurious signals. SFSR is ratio of the power of the fundamental compared to the power of the next largest component in the frequency spectrum. The SFSR specification is especially important to frequency domain applications which perform Fourier transforms to analyze the converter's output data. Processed applications like radar and network analyzers are typical areas where SFSR offers a direct prediction of converter's performance at both the system and component levels. SFSR is the single best specification for selecting a converter to be used in a frequency domain application.

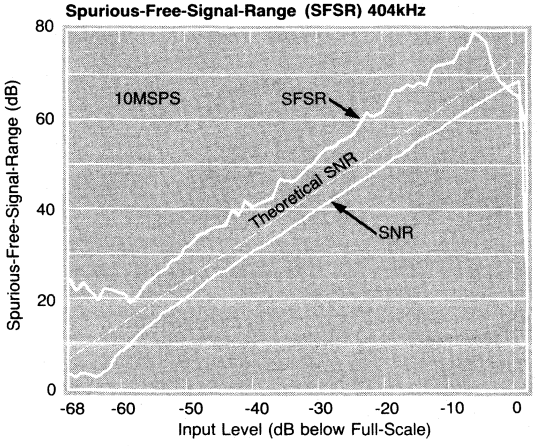
In-Band Harmonics (IBH) is the ratio of the power of the fundamental compared to the power of the single largest harmonic. This specification is very similar to SFSR, but since it only considers a fairly limited number of harmonics, it is potentially an incomplete gauge of converter performance. SFSR is more stringent and should be used whenever possible in lieu of IBH.



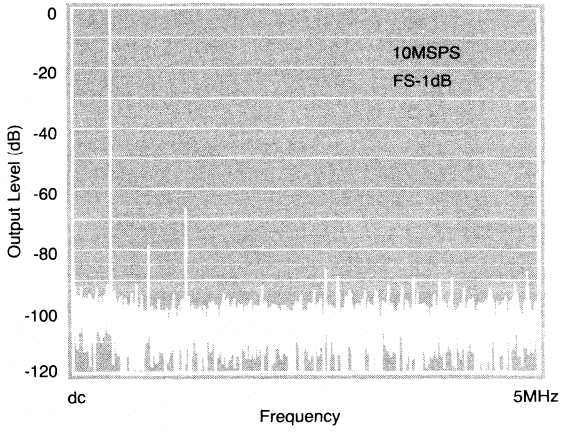
Typical Frequency Spectrum and its Components

Typical Performance Characteristics (10MSPS unless specified)

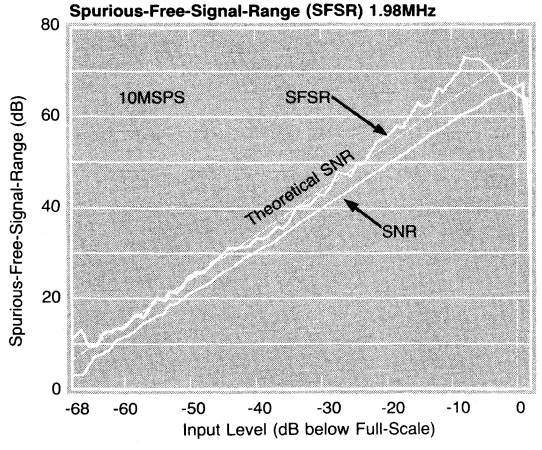
Spurious-Free-Signal-Range (SFSR) 404kHz



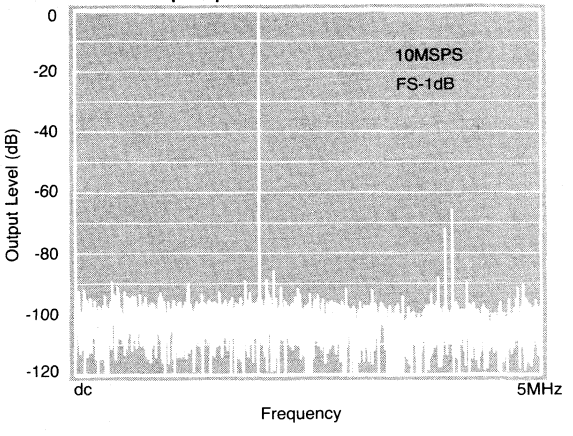
404kHz Output Spectrum



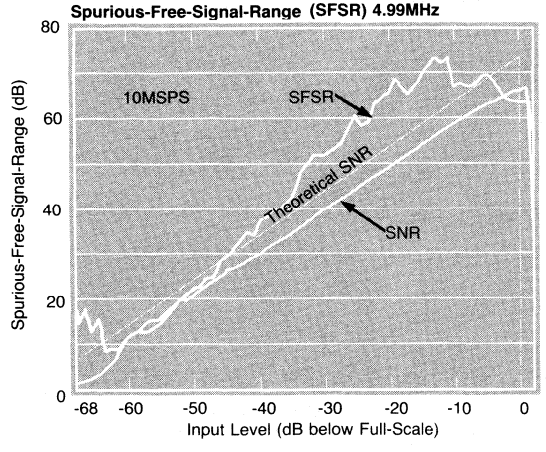
Spurious-Free-Signal-Range (SFSR) 1.98MHz



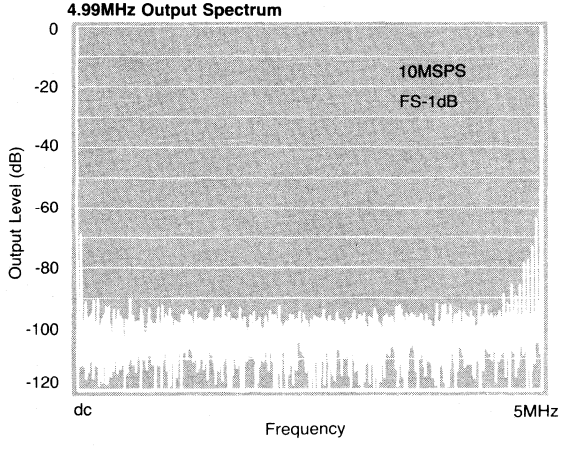
1.98MHz Output Spectrum



Spurious-Free-Signal-Range (SFSR) 4.99MHz



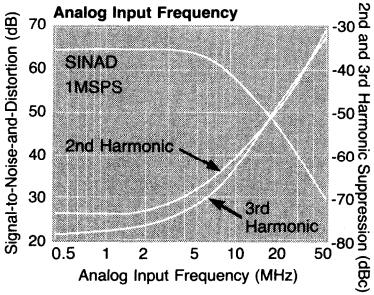
4.99MHz Output Spectrum



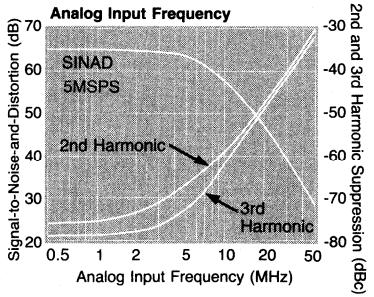
10

Typical Performance Characteristics (10MSPS unless specified)

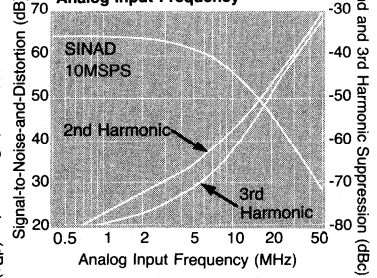
SINAD and Harmonics vs Analog Input Frequency



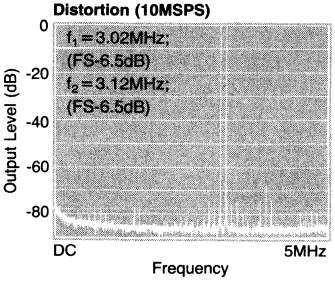
SINAD and Harmonics vs Analog Input Frequency



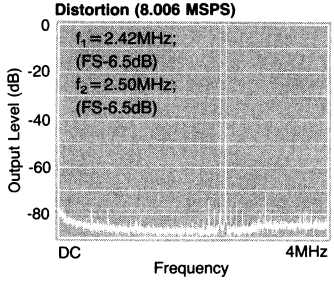
SINAD and Harmonics vs Analog Input Frequency



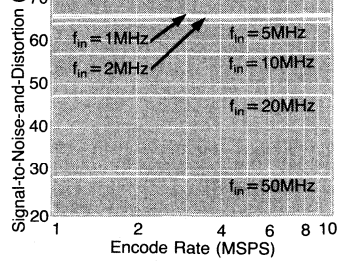
Two-Tone Intermodulation Distortion (10MSPS)



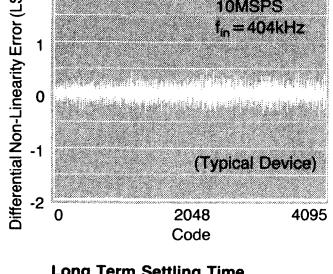
Two-Tone Intermodulation Distortion (8.006 MSPS)



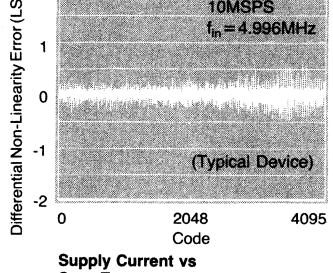
SINAD vs Encode Rate



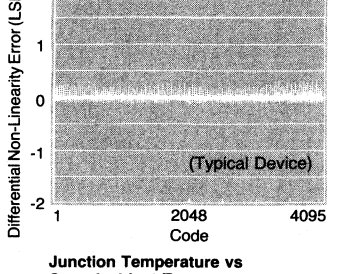
Differential Non-Linearity Error (Derived from Histogram)



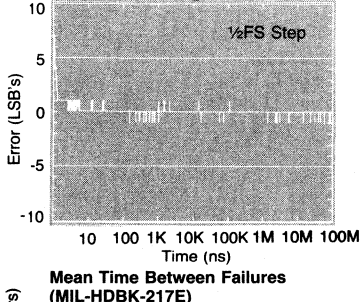
Differential Non-Linearity Error (Dynamic)



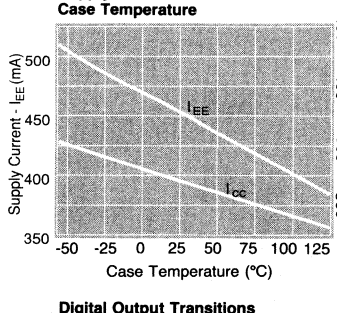
Differential Non-Linearity Error (Static)



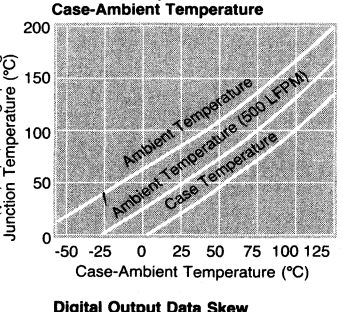
Long Term Settling Time



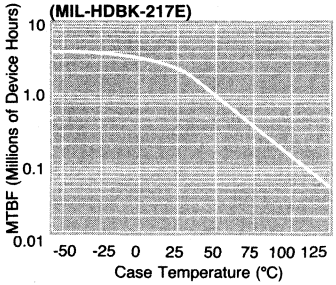
Supply Current vs Case Temperature



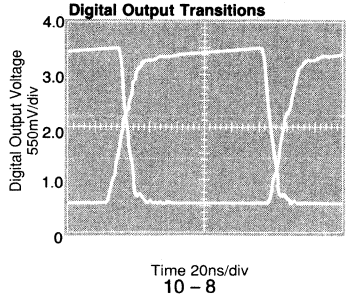
Junction Temperature vs Case-Ambient Temperature



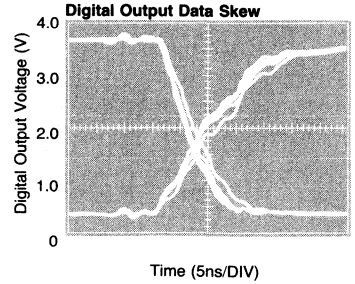
Mean Time Between Failures (MIL-HDBK-217E)



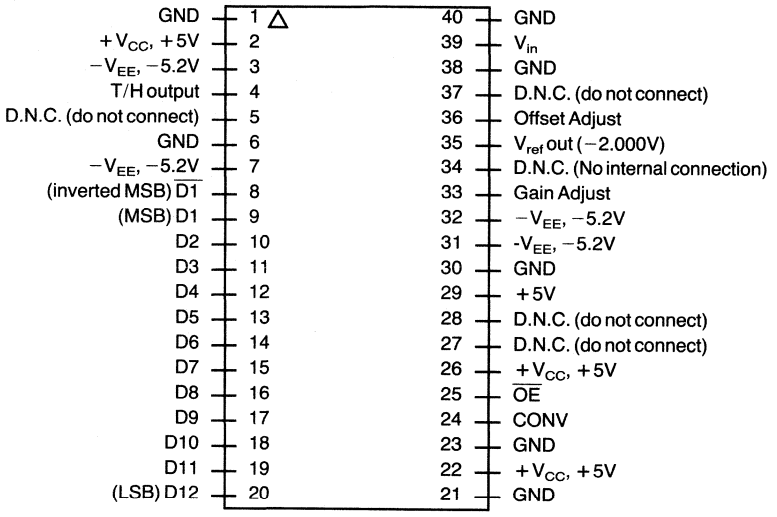
Digital Output Transitions



Digital Output Data Skew



CLC922 Pinout



Pin Description and Usage

TTL-level Digital Inputs

CONV — "Convert Command" begins a new conversion with a rising edge.

$\overline{OE}$ — "Output Enable" is an active low input which causes the digital outputs to leave their high-impedance state.

TTL-level Digital Outputs

D1-D12 — Digital data output. D1 is the MSB and D12 is the LSB.

$\overline{D1}$ — Inverted version of the MSB, which is used for twos complement coding.

Analog Input

V_{in} — Analog input with $2V_{pp}$ input range which can be placed anywhere in a −2V to +1V range. See offset adjust pin.

Gain Adjust — This input has a +2V to −2V input range and scales the $2V_{pp}$ analog input range by +10% or −10% respectively. Gain adjustments should be made prior to offset adjustments, or an iterative technique will be required. If this feature is not used, this pin should be grounded.

Offset Adjust — This pin has a ±2V input range and is used to translate the $2V_{pp}$ analog input anywhere in the −2V to +1V range, as well as to provide a facility for adjusting the DC offset of the part. Offset adjust is slightly dependent on the gain adjustment setting; offset adjustments should be made after any gain adjustments have been completed. This pin should be grounded if it is not used.

Miscellaneous

V_{ref} — V_{ref} is a high stability −2.000V voltage reference, although its precise value varies with specific gain adjust settings (see text).

D.N.C. — Do not connect!

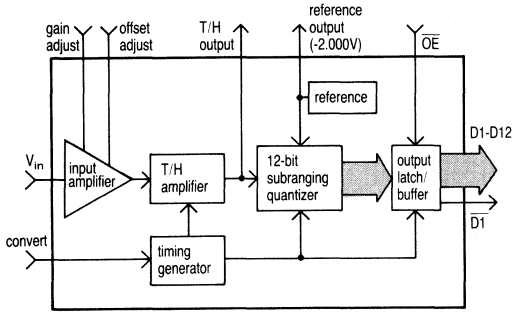
T/H output — This pin brings the internal T/H voltage out of the package through a 950Ω source impedance. The T/H output voltage is an inverted representation of the input signal, ranging from 0V to −2.0V. Normally this pin should be left unconnected.

Power and Ground

+5V, −5.2V & GND

CLC922 Operation

The CLC922 is a complete 12-bit 10MSPS A/D converter system. It includes input buffering, an internal track and hold amplifier, and references needed in a high-accuracy A/D system. The user need only apply power, ground, an input signal, and a convert signal to obtain 12-bit data every 100ns. Below is a block diagram of the converter:



CLC922 Block Diagram

The CLC922 uses the subranging A/D architecture, providing both high speed and high accuracy. This is the architecture of choice for A/D converters requiring high-speed and high resolution.

A conversion is initiated on the rising edge of the CONVERT signal, causing the internal T/H amplifier to switch from TRACK mode to HOLD mode. The internal two-pass quantizer will then convert the on-board track-and-hold signal into its digital equivalent. Approximately 25ns after the rising edge of CONVERT, new data will be latched into the output buffers. Since the CLC922 is a "pipelined" design, this data will be from the conversion two cycles before. Data from the present conversion will appear two cycles later (see timing diagram). The CLC922 incorporates several useful features including tri-statable outputs, offset adjust, gain adjust, and output data formatting. These features are detailed in the subsequent text.

T/H Output, V_{ref}, and Test Points (D.N.C.)

Several internal nodes are brought out of the package. Most of these are test points and should not be connected. Doing so may severely degrade performance or cause internal damage. The exceptions to this are the T/H output and the A/D reference voltage output, both of which are available to the user. Obviously, these nodes are critical to A/D performance and must be used with care – this is particularly true of the inverted T/H output (0V to −2.0V), which should normally be left unconnected.

The use of the −2.000V reference voltage output, on the other hand, is strongly encouraged. The reference output is a highly-stable voltage source, which can drive as little as 1kΩ at full accuracy. (Note: V_{REF} voltage output has been designed for tracking stability. Some variation in the precise output level is possible with various gain adjustment settings.)

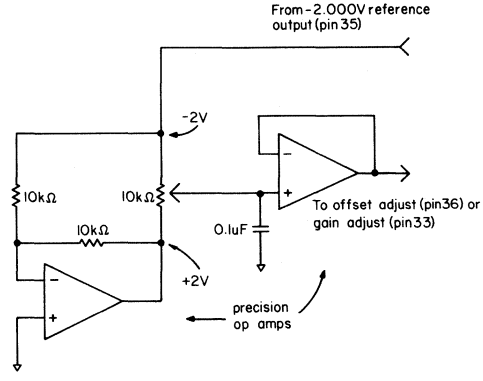
Input Range and Offset Adjustment

The input range of the CLC922 is laser trimmed to $2V_{pp}$ centered around ground (±1V). Additional flexibility has been built into the CLC922 by allowing negative unipolar operation (negative unipolar . . . −2V to 0V). The input offset is determined by the voltage at pin 36.

offset adjust voltage (pin 36)	analog input range
GND	−1V to +1V
−2V	−2V to GND

The $2V_{pp}$ input range of the CLC922 may be placed anywhere within the 1V to −2V window.

The offset adjustment pin should be driven from a voltage source that both exhibits a low impedance and is free of excessive noise. A voltage divider between power supplies fails both of these requirements. An elegant approach for this design is to use the CLC922's built-in 2V reference (pin 35). It may be connected directly to the offset adjust pin for a −2V to GND range or it may be used as shown below. The circuit below generates +2V by inverting the −2V reference voltage output. This +2V output may be used directly to provide an input signal range of GND to +2V. The +2V may also be used in conjunction with the −2V output and a potentiometer to provide maximum flexibility in setting the input range and adjusting the offset (as it is below). The unity-gain buffering op amp is needed to drive the adjustment pin with a low impedance.



Input Range and Offset Adjustment Circuit

Adjusting the Full-Scale Range

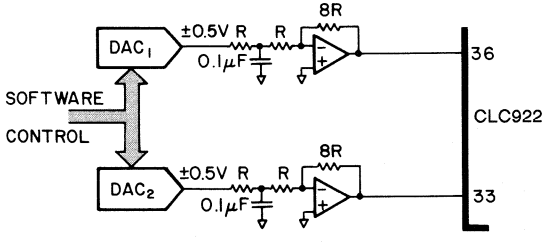
The 2V full-scale analog input range may be adjusted by up to ±10%. As with the offset adjust pin, the gain adjust pin has a ±2V input range. A voltage of −2V compresses the full scale range by 10%. In other words, with −2V applied to the gain adjust pin, the full scale range is 1.8V. (This effectively increases the gain of the converter by 10%.)

Conversely, applying +2V to the gain adjust pin expands the full scale range to 2.2V. (This effectively decreases the gain of the converter by 10%.) In each case, the expansion or compression is symmetric about "0" – both FS and –FS change. In practice, this means the gain adjustments should be made before the offset is adjusted.

gain adjust voltage (pin 33)	analog input range
GND	$2V_{pp}$
–2V	$1.8V_{pp}$
+2V	$2.2V_{pp}$

The circuit considerations which apply to the offset adjust pin also apply to the gain adjust pin (i.e., low source impedance and low noise); the offset adjust circuit may also be used for gain adjustments as indicated on the schematic. If flexibility is desired for both offset and gain adjust, an additional 10kΩ potentiometer and unity gain buffering op amp may be added.

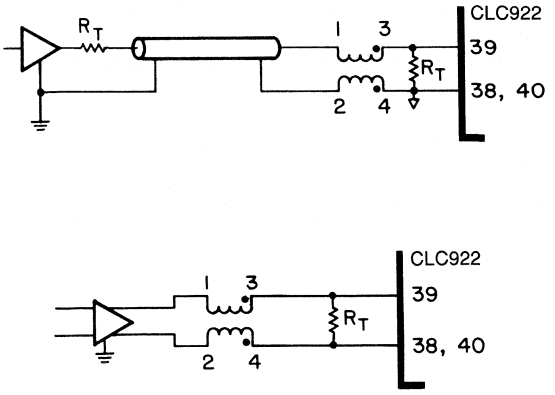
Auto-Calibration
Many systems benefit from the ability to dynamically adjust offset and/or the gain. This is easily accomplished by incorporating a D/A converter into the adjustment circuit above. The computer system drives the D/A and thereby adjusts the voltage applied to the offset and/or the gain adjust pins. Gain adjustments should be made before any offset adjustments.



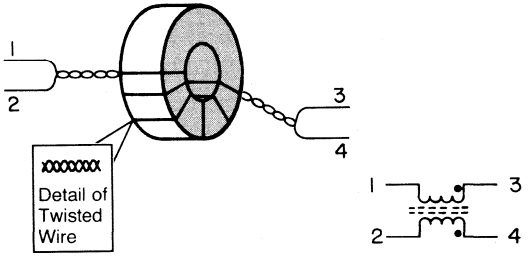
Simple DAC's provide Auto-cal Capability

Using a Balun for Impedance Control
Harsh environments may have an excessive amount of noise on signal and ground lines. Much of this type of "common mode" noise can be eliminated from the analog signal path through the use of a balun. A balun is a 1:1 impedance matching transformer which forces equal currents in both the signal and ground paths, forming a common mode choke. The inputs of the balun may be driven from either an isolated signal and ground, or a differential driver; either is acceptable.

A balun is constructed from approximately ten turns of twisted wire (#26 or #28 AWG) wound around a powdered iron toroid. This 1:1 impedance matching circuit should also minimize ground-loop effects.



Typical Balun Circuits



Balun Construction and Use

Timing Considerations
The CLC922 is designed to provide up to 10MSPS (10 million samples per second). This is equivalent to 100ns per conversion cycle. After the rising edge of the CONVERT signal (which initiates the actual conversion cycle), the on-board track-and-hold will move from TRACK mode to HOLD mode, followed by a two-step conversion process. Data is "pipelined" within the CLC922, meaning that data from a specific conversion will take two more conversion cycles to make its way to the CLC922 outputs (see timing diagram page 5).

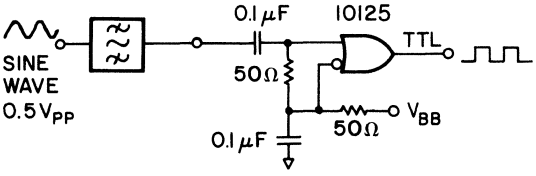
The conversion cycle ends approximately 30ns after rising edge of CONVERT. The CONVERT pulse should remain HIGH during this 30ns interval to prevent the clock transition from corrupting the conversion cycle accuracy. On the other end of the CONVERT cycle (prior to the rising edge which initiates the next conversion cycle), the LOW period should also be at least 40ns long. The on-board track-and-hold will move from HOLD mode to TRACK mode soon after the falling edge of CONVERT. The CLC922 requires just less than 40ns of track time for rated performance, hence the 40ns CONVERT pulse width LOW requirement. Both t_{PWH} and t_{PWL} for CONVERT may be extended much longer in time, although no increase in conversion accuracy should be expected.

There is no lower bound for the CLC922 conversion rate. In other words "dc" clocks are acceptable, but the edge transition times should be less than 20ns for proper operation.

Convert Clock Considerations

The CLC922 requires a TTL level clock signal to control the conversion timing. On each rising edge of the CONVERT signal, the CLC922 will initiate a conversion sequence. The quality and purity of the clock signal has a major impact on the quality and accuracy of the conversion process. Essentially what the CLC922 requires is an extremely low jitter clock source, at least as good as the CLC922 aperature jitter specification at 4.5ps(rms). Excessive jitter will manifest itself as broad-band noise, severely degrading the converter's accuracy.

The low clock jitter requirements eliminate nearly all commercial pulse generators, and most signal sources, at least in terms of their direct output. A simple method of "squaring up" low-jitter clock signals, is to use a narrow-band pass filter to generate a pure sine wave at the conversion frequency. This signal is then "squared up" using a modified ECL-to-TTL translator. This technique should allow most low-jitter signal sources to be used without loss of conversion accuracy. A detailed circuit is illustrated below.



SINE to TTL Conversion Circuit

If the signal-to-noise ratio is below expectations and the input signal is not noisy, clock jitter should be investigated.

$$SNR_{MAX} = 20LOG \left| \frac{1}{2\pi f_{in}\ Jitter_{RMS}} \right|$$

where . . .

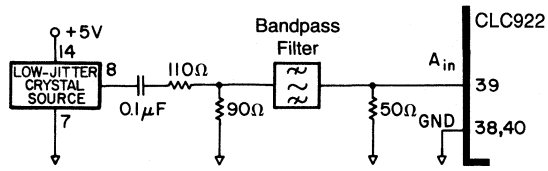
$$Jitter_{RMS} = \sqrt{(Clock\ Jitter_{RMS})^2 + (Analog\ Jitter_{RMS})^2}$$

Crystal Sources

Standard crystal controlled TTL oscillators are a very cost-effective and a convenient source of high purity clock signals. The inherently low jitter present in such sources is ideal for ADC testing and evaluation. Additionally, crystal sources are an excellent source, once filtered, for use as an analog input signal, particularly in test and evaluation applications.

Output Latching

The CLC922 ouput data will, in most cases, be placed in a buffer memory prior to further processing. This may require higher digital drive capability than the CLC922 can provide. To overcome this, output latches should be placed just after the CLC922.



Low Jitter Crystal Source with Bandpass Filtering

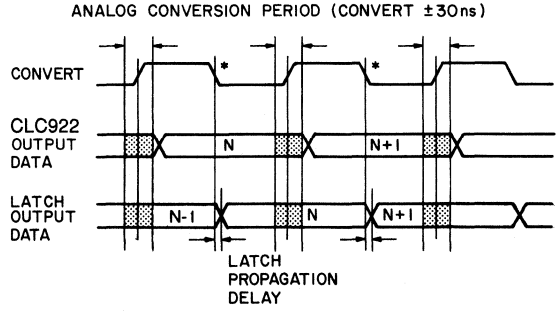
The timing of these latches can play a major role in the conversion accuracy. Some of the issues involved here are minimizing digital feedthrough to the analog signal, digital corruption of the conversion process, digital corruption of the output data, and proper setup and hold time condition.

Data Ready

The most critical portion of the conversion cycle is the 30ns after the rising edge of CONVERT (the actual conversion period) and the 15ns window just before the rising edge of CONVERT (the final track-and-hold setting period just prior to the conversion). Any digital switching, latches or otherwise, may seriously undermine the CLC922 conversion accuracy. In other words . . . the use of the CONVERT Clock (rising edge) as a DATA READY signal, may inject digital switching noise back onto the analog input signal.

Using the rising edge of CONVERT for a DATA READY signal means that no more than 10ns of hold time is available to external logic. On the other hand, assuming 10MSPS and a 50% duty cycle CONVERT clock, better than 40ns of setup time is available with 60ns hold time, provided the falling edge of CONVERT is used as a DATA READY.

The falling edge DATA READY will place latch and bus transitions after the internal conversion cycle, but also well before the critical final setting interval for the on-board track-and-hold. This technique is particularly effective when used with a 50% duty cycle CONVERT clock. Assuming the worst-case timing at 10MSPS operation, the falling edge of CONVERT used as a DATA READY will be approximately 20ns after the internal conversion is complete, and a full 20ns before the on-board track-and-hold enters track mode for the next cycle. This should allow switching transients to die down, even in a very noisy digital system, before the next analog digitization takes place.



***Note that when the falling edge of convert is used to clock subsequent logic, that no digital transitions occur during the analog conversion period (shaded region ±30ns around the rising edge of convert)**

Recommended Latch/DATA READY Timing

Output Coding

The CLC922 offers two output coding formats, Offset Binary and Two's Complement. "Offset Binary" assumes a bipolar input range for convenience, but essentially it denotes all zeroes for the most negative input representation, and all ones for the most positive input representation. The Two's Complement format also assumes a bipolar input, but inverts D1(MSB) to provide the proper coding.

Both output formats function normally if offset input ranges are employed (i.e., unipolar or negative). The selection of output formats is made by choosing whether D1(MSB) or D1(MSB) is used as a data output.

Analog Input	Offset Binary	Two's Complement
FS-1LSB	111111111111	011111111111
FS-2LSB's	111111111110	011111111110
FS-3LSB's	111111111101	011111111101
–	–	–
–	–	–
mid-scale + 1/2LSB	100000000000	000000000000
mid-scale – 1/2LSB	011111111111	111111111111
–	–	–
–	–	–
-FS + 2LSB's	000000000010	100000000010
-FS + 1LSB	000000000001	100000000001
-FS	000000000000	100000000000

Grounding

All of the CLC922 grounds are internally connected. Pins 1, 6, 21, and 40 are connected through the package itself; these are further connected to all other ground pins by way of the substrate and bond wires.

The CLC922 has been designed to incorporate a single ground plane for both digital and analog return currents. A "split" ground plane (one for digital components and another for analog components) is not recommended. Although a split ground approach is not recommended, certain types of systems preclude the use of a single ground plane. For these systems, the following chart matches signals and return currents so that the most appropriate grounding choices can be made.

Signal/ Power	Ground Return	Primary Activity
2, 3	1	T/H Power Supply Pins
7, 26, 32	6	Quantizer Power
8-20, 22	21, 23	Digital Output Stage Power
29, 31	30	Digital Processing Power
39	38, 40	Analog Input Signal

NOTE: Pins 1, 6, 21, and 40 are connected through the package metalization itself.

Power Supplies and Decoupling

The CLC922 does not require separate analog and digital power supplies as is often recommended for high-performance data converters. The design is well-balanced internally and includes on-board decoupling capacitors. As with any high-performance circuit, supply variations can degrade performance. DC variation of supplies, within the rated ±5% range, should have only a minimal effect on performance. AC supply variation can be more troublesome. The CLC922 operates with a power supply rejection ratio (PSRR) of better than −50dB. Even so, adequate supply decoupling will help to ensure rated performance.

The recommended supply decoupling scheme is as follows:

Option #1: One 0.1μF ceramic capacitor at each supply pin, with a 5-10μF electrolytic or tantalum for each of the three main supply feeds (proximity not critical).

Option #2: One 0.1 to 0.033 chip capacitor at each supply pin, with a 5-10μF electrolytic or tantalum for each of the three main supply feeds (proximity not critical).

Please note that supply feeds, with excessive digital switching noise from other sources, may require additional filtering.

Layout Considerations

The CLC922 has been designed to be easily accommodated on a printed circuit board; for example, the inputs enter one side of the package and the ouputs leave on the opposite side, with the analog and digital connections widely separated from one another. The PC board should exhibit similar layout guidelines. If the analog input signal has had to travel more than a few inches to reach the analog input pin (V_{IN}), proper termination techniques should be followed to avoid reflections caused by improper impedance matching. Special care should also be exercised to place external output latches close to the CLC922 digital outputs.

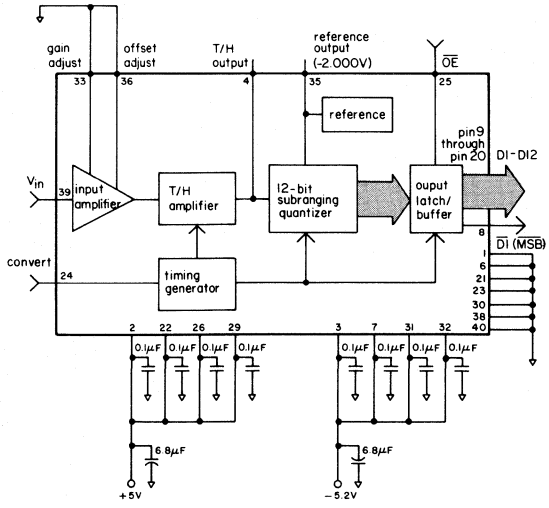
Sockets are not recommended, in that they increase both lead inductance and inter-lead capacitance. If sockets must be used, Teflon or "pin" type sockets should minimize this effect. Additionally, the "Recommended Power Supply Decoupling Scheme" illustrates an effective bypass arrangement. Chip capacitors are preferred and should be located as close as practical to the individual supply pins.

CLC922 Evaluation Board Support

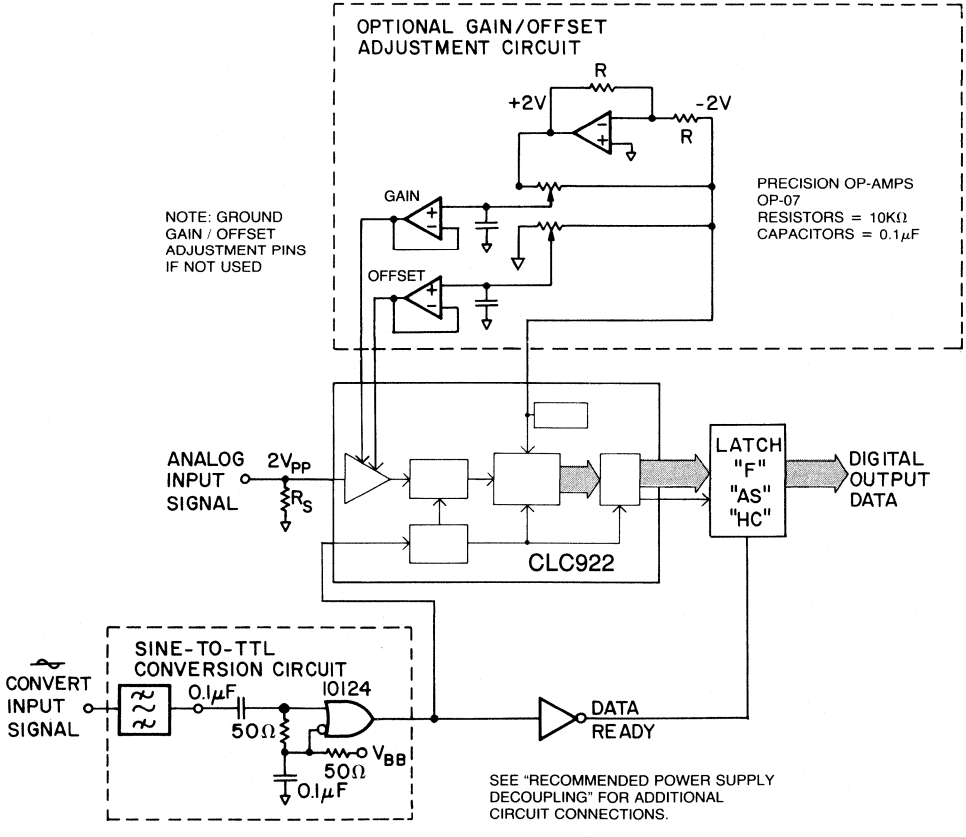
An evaluation board (Comlinear part number 730015) is available for the CLC922 at minimal cost. It is designed to provide a simple platform for evaluating the CLC922.

Applications Assistance

Comlinear maintains a staff of R&D-level applications engineers, who are available for design and applications assistance at (303) 226-0500.



Recommended Power Supply Decoupling Scheme



Complete System Architecture with Offset and Gain Adjustment

Comlinear Corporation

12-Bit, 10MSPS A/D Converter

CLC925

APPLICATIONS:

- radar processing
- FLIR processing/electronic imaging
- instrumentation
- medical imaging
- transient-signal recorders

FEATURES (typical):

- 66.8dB spurious free signal range; $f_{IN} = 5MHz$
- no missing codes guaranteed
- 0.35LSB differential linearity
- small package (2.28in²)
- low power dissipation 4.2W

DESCRIPTION

The CLC925 is a 12-bit analog-to-digital converter subsystem, including 12-bit quantizer, internal track-and-hold, reference circuitry and error correction circuits. The CLC925 is constructed using advanced thin-film technology, and is built in a fully certified MIL-STD-1772 facility.

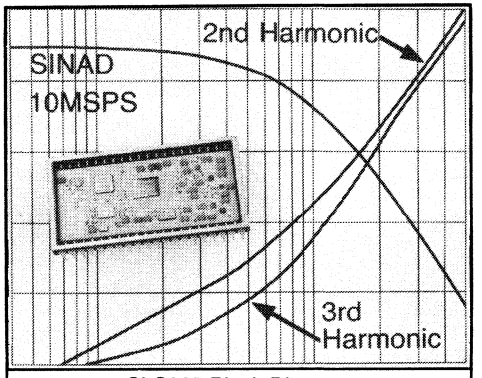
The CLC925 incorporates a complete two-pass subranging architecture, constructed from several high-speed building blocks. A broadband (70MHz) input amplifier buffers input signals and provides an accurate drive signal to the on-board track-and-hold. Laser trimmed gain and offset circuits assure accurate matching unit to unit, while also offering broad flexibility in both gain and offset adjustment. Gain adjustment range is ±10%, with the $2V_{PP}$ input range adjustable over a ±2V range. The latched outputs of the CLC925 mean that only a convert clock, analog input and power supplies are required for operation; internal logic generates all required timing signals.

Comprehensive dynamic testing on every part ensures that system performance goals will be met. The spurious-free-signal-range of 74.2dB@404kHz and 66.8dB@4.99MHz give an effective dynamic range of 12.0 bits and 10.8 bits respectively. This, coupled with an SNR specification of 66.6dB@4.99MHz, means that the CLC925 is ideally suited for use in areas like radar, instrumentation, and medical signal processing.

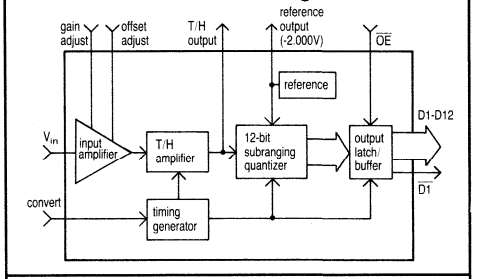
The CLC925BI is specified over a temperature range of -25°C to +85°C, while the CLC925B8C is specified over a range of -55°C to +125°C. Both devices are packaged in 40-pin, 1.1 inch wide, ceramic DIP's (note: leads are side brazed for easy access and inspection).

Ordering Information		
CLC925BI	– 25°C to + 85°C	industrial version
CLC925B8C	– 55°C to + 125°C	MIL-STD-883, Level B

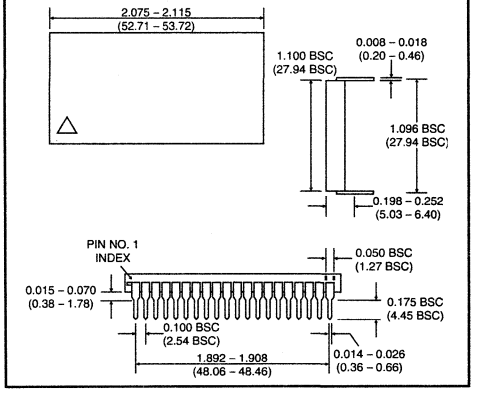
All versions of the CLC925 are manufactured in Comlinear's MIL-STD-1772 certified facility in Fort Collins, Colorado, U.S.A. The DESC SMD number is 5962-90995.



CLC925 Block Diagram



Package Dimensions



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DS925.07

January 1993

Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_{EE}$ = -5.2V; unless specified)

PARAMETER[1]	CONDITIONS		TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Case Temperature	CLC925B8C		+25°C	-55°C	+25°C	+125°C		
Case Temperature	CLC925BI		+25°C	-25°C	+25°C	+85°C		
DYNAMIC CHARACTERISTICS								
small signal bandwidth	V_{IN} = 1/4 FS		70	50	50	50	MHz	SSBW
large signal bandwidth	V_{IN} = FS		65	45	45	45	MHz	LSBW
slew rate			300	250	250	230	V/μs	SR
overvoltage recovery time	V_{IN} = 2FS		26	38	38	38	ns	OR
effective aperture delay			1.2	3.0	2.5	3.0	ns	TA
aperture jitter			4.5	7.0	6.0	6.0	ps(RMS)	AJ
NOISE AND DISTORTION (10MSPS)								
* signal-to-noise ratio								
(not including harmonics)	404kHz;	FS	67.5	64.5	65	65	dB	SNR1
	4.996MHz;	FS	66.6	63.5	65	65	dB	SNR2
*in-band harmonics	404kHz;	FS-1dB	-74.2	-60.5	-64	-64	dBc	IBH1
	4.996MHz;	FS-1dB	-66.8	-59	-61.5	-60	dBc	IBH2
*total harmonic distortion	404kHz;	FS-1dB	-71.2	-60	-63	-63	dBc	THD1
	4.996MHz;	FS-1dB	-64.6	-58	-60	-57	dBc	THD2
*signal-to-noise-and distortion								
(including harmonics)	404kHz;	FS-1dB	65	59	61	61	dB	SND1
	4.996MHz;	FS-1dB	62	57	59	56.5	dB	SND2
*spurious-free-signal-range								
(SFSR)	404kHz;	FS-1dB	74.2	60.5	64	64	dB	SFSR1
	4.996MHz;	FS-1dB	66.8	59	61.5	60	dB	SFSR2
*effective bits								
(based on SFSR)	404kHz;	FS-1dB	12.0	9.75	10.33	10.33	bits	SFEB1
	4.996MHz;	FS-1dB	10.8	9.50	9.92	9.67	bits	SFEB2
*effective bits								
(based on SINAD)	404kHz;	FS-1dB	10.50	9.50	9.84	9.84	bits	EB1
	4.996MHz;	FS-1dB	10.00	9.17	9.50	9.09	bits	EB2
DC ACCURACY and PERFORMANCE								
* differential non-linearity	dc; FS		0.35	1.0	1.0	1.0	LSB	DNL
*integral non-linearity	dc; FS		1.2	4.0	4.0	4.0	LSB	INL
*missing codes			0	0	0	0	codes	MC
*bipolar offset error			3.4	30	10	12	mV	VIO
temperature coefficient				300		150	μV /°C	DVIO
*bipolar gain error			0.3	2.7	1.0	1.5	%FS	GE
temperature coefficient				0.035		0.010	%FS /°C	DGE
reference voltage output			-2.000				V	VREF
ANALOG INPUT PERFORMANCE								
+ analog input bias current			10	45	25	35	μA	IBN
+ temperature coefficient			100	250	-	100	nA /°C	DIBN
analog input resistance			80	> 25	> 50		kΩ	RIN
analog input capacitance			3.5	5.5	5.5	5.5	pF	CIN
POWER REQUIREMENTS								
*supply current ($+V_{CC}$ = +5.0V)	10MSPS; no load		318	410	385	360	mA	ICC
*supply current ($-V_{EE}$ = -5.2V)	10MSPS; no load		454	700	630	550	mA	IEE
*supply current ($+V_1$ = +15.0V)	10MSPS; no load		24	30	30	30	mA	I1
nominal power dissipation	10MSPS; no load		4.2				W	PD

Note 1: Parameters preceded by an * are the final electrical test parameters and are 100% tested. B8C units are tested at – 55°C, + 25°C, and + 125°C. Parameters preceded by a + are 100% tested on B8C units only. BI units are tested only at + 25°C although their performance is guaranteed at – 25°C and + 85°C as indicated above.

Note 2: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3: Operation down to 11V is possible with negligible degradation in performance.

Note 4: Junction temperature rise above case ≈ 16°C; θ_{ca} = 16°C/W; θ_{ca} = 7°C/W @ 500LFPM. (Use of a SIL-PAD* #550007, from Berquist (800-347-4572), can lower case-to-ambient rise; θ_{CA} = 12°C/W @ still air – 12in² ground-plane; θ_{CA} = 3.4°C/W @ 100LFPM – 12in² ground plane.)

Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_{EE}$ = -5.2V; unless specified)

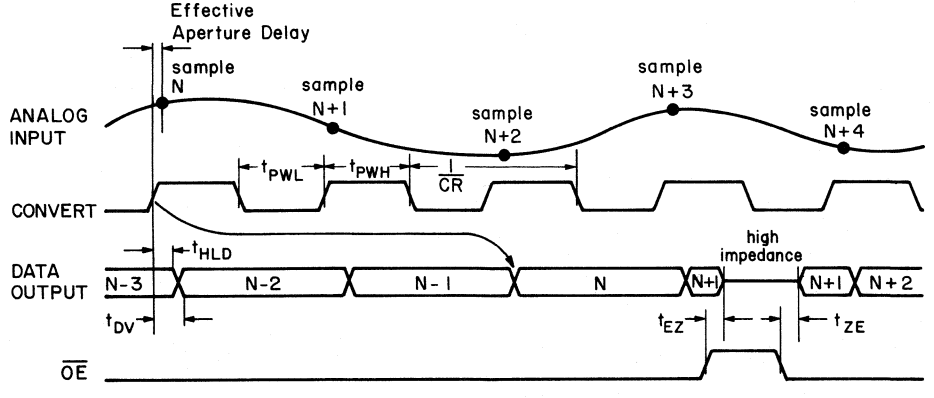
PARAMETER[1]	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Case Temperature	CLC925B8C	+25°C	-55°C	+25°C	+125°C		
Case Temperature	CLC925BI	+25°C	-25°C	+25°C	+85°C		
DIGITAL INPUTS							
+ input voltage	logic low		0.8	0.8	0.8	V	VIL
	logic high		2.0	2.0	2.0	V	VIH
+ input current	logic low	-1.9	-2.8	-2.8	-2.8	mA	IIL
	logic high	80	350	350	350	μA	IIH
DIGITAL OUTPUTS							
+ output voltage	logic low, IOL = 4mA	0.2	0.5	0.5	0.5	V	VOL
	logic high, IOH = -1mA	3.2	2.4	2.4	2.4	V	VOH
+ output leakage current, high impedance	logic low	5	150	150	150	μA	IOZL
	logic high	5	150	150	150	μA	IOZH
TIMING							
maximum conversion rate			10	10	10	MSPS	CR
minimum conversion rate		0				MSPS	CRM
data hold time		13	9	10	10	ns	THLD
output propagation delay		24	35	35	40	ns	TDV
OE LOW to enabled output		19	30	30	30	ns	TZE
OE HIGH to high impedance		12	30	30	30	ns	TEZ

Recommended Operating Conditions

positive supply voltage ($+V_{CC}$)	+5V±5%
positive supply voltage ($+V_1$)[3]	+15V±5%
negative supply voltage ($-V_{EE}$)	-5.2V±5%
differential voltage between any two GNDs	10mV
analog input voltage range	$2V_{pp}$ (within ±2V)
maximum V_{REF} output current	2mA
minimum CONVERT pulse width HIGH (t_{PWH})	30ns
minimum CONVERT pulse width LOW (t_{PWL})	40ns
digital input voltage range	0V to $+V_{CC}$

Absolute Maximum Ratings[2]

positive supply voltage ($+V_{CC}$)	+7.0V
positive supply voltage ($+V_1$)	+18V
negative supply voltage ($-V_{EE}$)	-7.0V
differential voltage between any two GNDs	200mV
analog input voltage range	$-V_{EE}$ to $+V_{CC}$
V_{REF} output current	20mA
CONVERT and OE input voltage range	0V to $+V_{CC}$
gain and offset adjust voltage range	$-V_{EE}$ to $+V_{CC}$
output short circuit duration (one pin to ground)	Infinite
Junction Temperature[4]	+175°C
Operating Temperature Range (Case)	
BI	-25°C to +85°C
B8C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Solder Duration (+300°C)	10 sec



Timing Diagram

Understanding A/D Dynamic Specifications

Analog-to-Digital converters are specified in many ways. As a component achieves higher performance, its specifications and their definitions can become more critical. Fortunately, the vast number of converter applications can generally be placed into one of two classes. These are processed data and non-processed data applications. The distinction seems quite simple but the split implies a completely different approach in specifying A/D converters for a given application.

The processed data area includes the frequency domain applications which employ Fourier processing (FFT). Also in this category are the highly averaged applications, usually concerned with low noise. In each case, the converter's data is averaged or convolved mathematically. This processing reduces the apparent noise level in the output data. For FFTs, the noise is simply spread over a large number of frequency bins. For simple averaging approaches, the gaussian distribution of noise is greatly reduced, appearing to increase the converter's resolution. Processed applications include radar, network and spectrum analyzers, communications receivers, etc.

The non-processed applications tend to take the converter's data in its original form with very little processing. This means that the noise reduction benefits of the processed applications are not seen. The non-processed area is composed primarily of time domain applications like imaging, DSO's, ultrasound, etc.

The processed vs. non-processed issue has several implications in terms of converter specifications. For the non-processed (time domain) systems the dominant converter specifications deal with noise (SNR) and converter accuracy (DNL). The converter's quantization noise and input stage noise dominate converter accuracy . The harmonic distortion (primarily INL) of the converter is generally of little interest given that most time domain applications present data for visual analysis and tend to focus on "local" accuracy rather than over the full input range. "Local" accuracy is best described through the standard noise measurements, such as SNR and DNL.

In the frequency domain application areas, the noise of the converter is processed to the point where, for almost all systems, it is no longer of issue. This is manifested as a reduction in the apparent noise floor. The actual RMS noise is not reduced, but is spread over more and more frequency bins as processing levels are increased. Unfortunately, the harmonic distortion performance of the converter is not affected by increased processing. This makes the harmonic performance, or more specifically the spurious performance, the dominant error source for frequency domain applications. SFSR becomes the dominant specification for determining converter performance in the frequency domain.

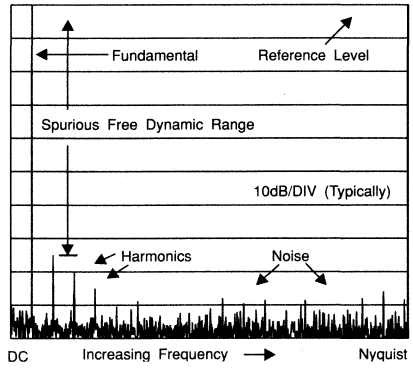
Signal-to-Noise Ratio (SNR) is the ratio of the power contained in the fundamental signal compared to the power contained in the entire noise floor. That is to say all individual noise components are added together to arrive at an integrated noise power. For SNR, harmonic power is excluded from the noise measurement. SNR is particularly important in time domain applications like digital image processing and infrared imaging, where conversion accuracy can be heavily degraded by integrated noise.

Signal-to-Noise-and-Distortion (SINAD) is the ratio of the fundamental signal power to the power at all other frequencies. This includes all noise as well as all harmonics. SINAD is a worst case specification for A/D converters, combining variables from both frequency and time domains. The value of SINAD in high-performance converter applications is not clear since it does not accurately predict the best converter for a given application. Because applications tend to fall into time domain/non-processed or frequency domain/processed applications, those specifications more directly related to the application should be the primary focus in selecting the converter.

Total Harmonic Distortion (THD) is the combined power of a specified number of harmonics, compared to the power of the fundamental signal. Harmonics are located at predictable frequencies, spaced at integer multiples of the fundamental signal. For example, a 1MHz fundamental would generate harmonics at 2MHz, 3MHz, 4MHz, ... and so on. In practice, only the first five harmonics contribute significantly to THD, although more may be included in the measurement. THD does not tend to apply well in frequency domain applications which are by their nature very SFSR oriented. In time domain applications, THD is indicative of full-scale input range distortion, however the high-performance time domain applications are generally most interested in local distortion performance. Local distortion and accuracy is dominated by DNL. The use of THD for applications requiring local performance is not likely to yield accurate or repeatable results in selecting the correct converter.

Spurious-Free-Signal-Range (SFSR) is the "clean" dynamic range of the converter, free from harmonic and spurious signals. SFSR is ratio of the power of the fundamental compared to the power of the next largest component in the frequency spectrum. The SFSR specification is especially important to frequency domain applications which perform Fourier transforms to analyze the converter's output data. Processed applications like radar and network analyzers are typical areas where SFSR offers a direct prediction of converter's performance at both the system and component levels. SFSR is the single best specification for selecting a converter to be used in a frequency domain application.

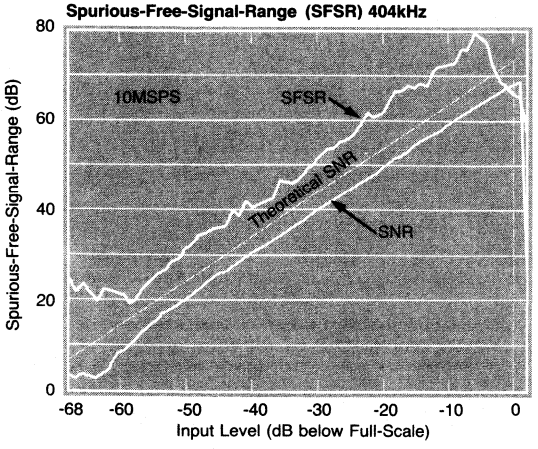
In-Band Harmonics (IBH) is the ratio of the power of the fundamental compared to the power of the single largest harmonic. This specification is very similar to SFSR, but since it only considers a fairly limited number of harmonics, it is potentially an incomplete gauge of converter performance. SFSR is more stringent and should be used whenever possible in lieu of IBH.



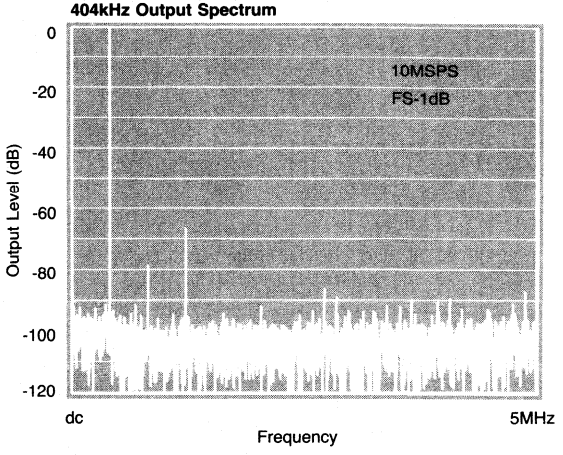
Typical Frequency Spectrum and its Components

Typical Performance Characteristics (10MSPS unless specified)

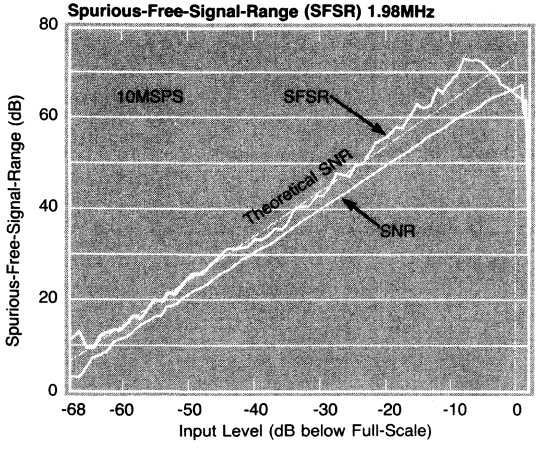
Spurious-Free-Signal-Range (SFSR) 404kHz



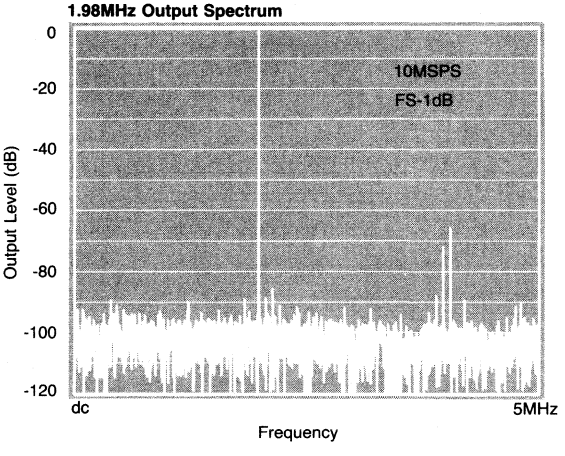
404kHz Output Spectrum



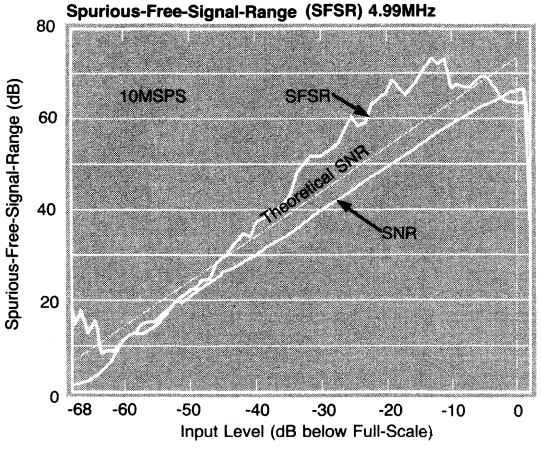
Spurious-Free-Signal-Range (SFSR) 1.98MHz



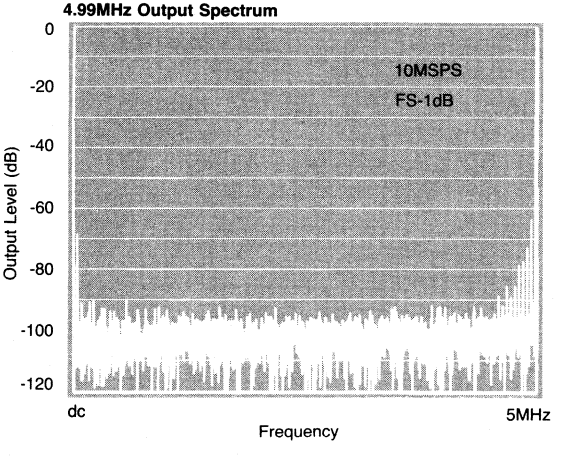
1.98MHz Output Spectrum



Spurious-Free-Signal-Range (SFSR) 4.99MHz



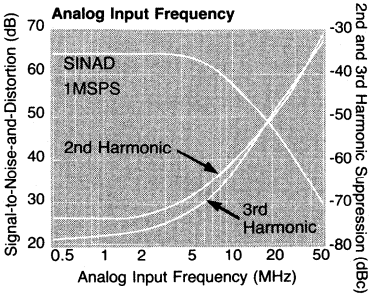
4.99MHz Output Spectrum



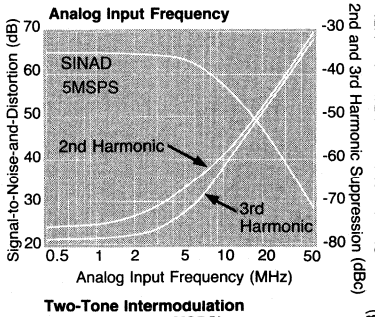
10

Typical Performance Characteristics (10MSPS unless specified)

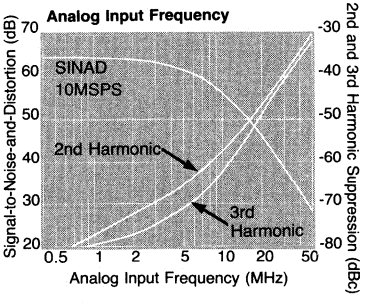
SINAD and Harmonics vs Analog Input Frequency



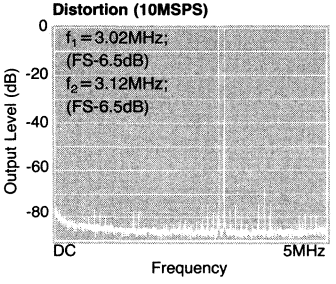
SINAD and Harmonics vs Analog Input Frequency



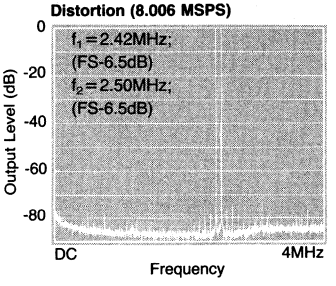
SINAD and Harmonics vs Analog Input Frequency



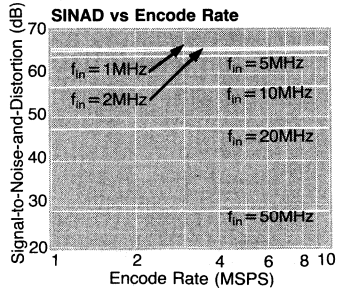
Two-Tone Intermodulation Distortion (10MSPS)



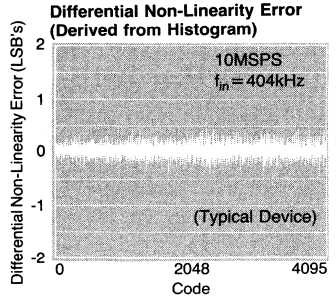
Two-Tone Intermodulation Distortion (8.006 MSPS)



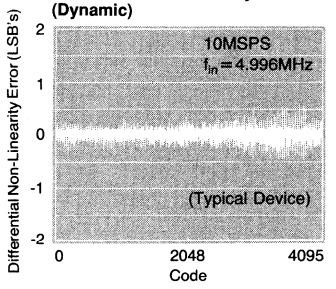
SINAD vs Encode Rate



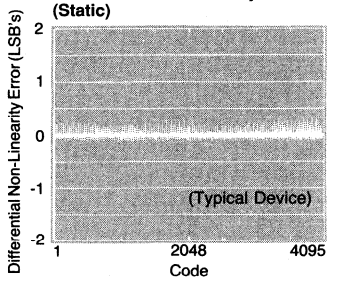
Differential Non-Linearity Error (Derived from Histogram)



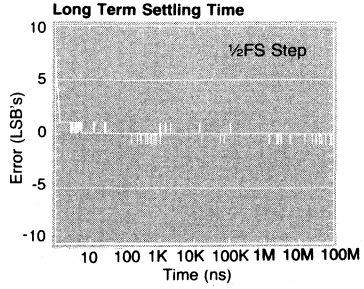
Differential Non-Linearity Error (Dynamic)



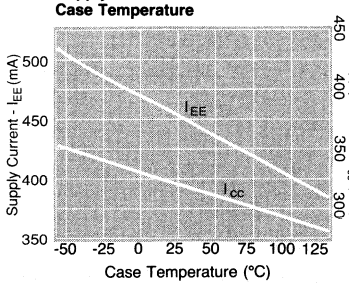
Differential Non-Linearity Error (Static)



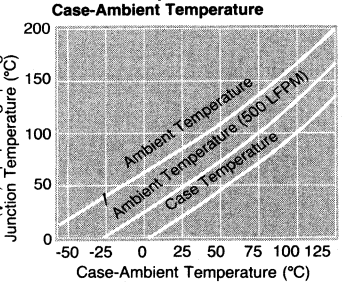
Long Term Settling Time



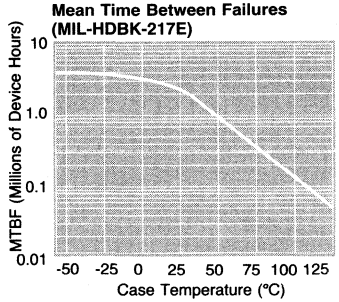
Supply Current vs Case Temperature



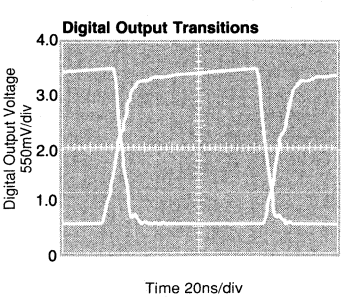
Junction Temperature vs Case-Ambient Temperature



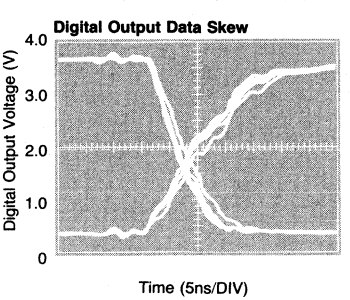
Mean Time Between Failures (MIL-HDBK-217E)



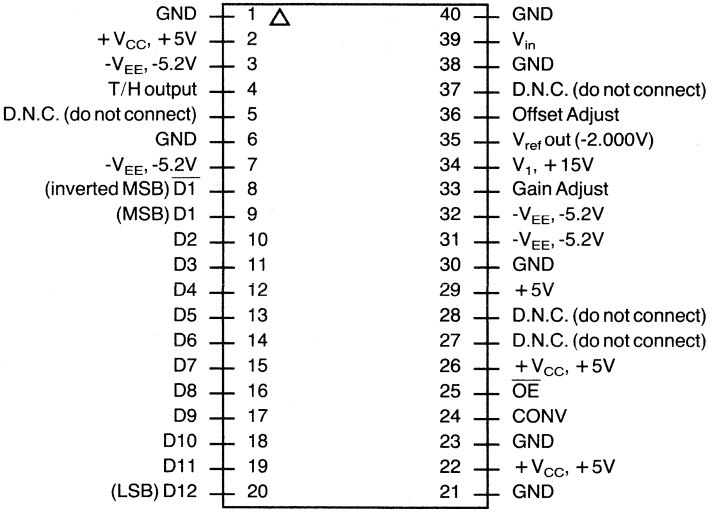
Digital Output Transitions



Digital Output Data Skew



CLC925 Pinout



Pin Description and Usage

TTL-level Digital Inputs

CONV — "Convert Command" begins a new conversion with a rising edge.

$\overline{OE}$ — "Output Enable" is an active low input which causes the digital outputs to leave their high-impedance state.

TTL-level Digital Outputs

D1-D12 — Digital data output. D1 is the MSB and D12 is the LSB.

$\overline{D1}$ — Inverted version of the MSB, which is used for twos complement coding.

Analog Input

V_{in} — Analog input with $2V_{pp}$ input range which can be placed anywhere in a -2V to +2V range. See offset adjust pin.

Gain Adjust — This input has a +2V to -2V input range and scales the $2V_{pp}$ analog input range by +10% or -10% respectively. Gain adjustments should be made prior to offset adjustments, or an iterative technique will be required. If this feature is not used, this pin should be grounded.

Offset Adjust — This pin has a ±2V input range and is used to translate the $2V_{pp}$ analog input anywhere in the -2V to +2V range, as well as to provide a facility for adjusting the DC offset of the part. Offset adjust is slightly dependent on the gain adjustment setting; offset adjustments should be made after any gain adjustments have been completed. This pin should be grounded if it is not used.

Miscellaneous

V_{ref} — V_{ref} is a high stability -2.000V voltage reference, although its precise value varies with specific gain adjust settings (see text).

D.N.C. — Do not connect!

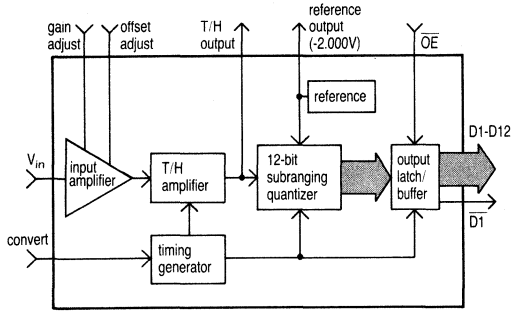
T/H output — This pin brings the internal T/H voltage out of the package through a 950Ω source impedance. The T/H output voltage is an inverted representation of the input signal, ranging from 0V to -2.0V. Normally this pin should be left unconnected.

Power and Ground

+5V, +15V, -5.2V & GND

CLC925 Operation

The CLC925 is a complete 12-bit 10MSPS A/D converter system. It includes input buffering, an internal track and hold amplifier, and references needed in a high-accuracy A/D system. The user need only apply power, ground, an input signal, and a convert signal to obtain 12-bit data every 100ns. Below is a block diagram of the converter:



CLC925 Block Diagram

The CLC925 uses the subranging A/D architecture, providing both high speed and high accuracy. This is the architecture of choice for A/D converters requiring high-speed and high resolution.

A conversion is initiated on the rising edge of the CONVERT signal, causing the internal T/H amplifier to switch from TRACK mode to HOLD mode. The internal two-pass quantizer will then convert the on-board track-and-hold signal into its digital equivalent. Approximately 25ns after the rising edge of CONVERT, new data will be latched into the output buffers. Since the CLC925 is a "pipelined" design, this data will be from the conversion two cycles before. Data from the present conversion will appear two cycles later (see timing diagram). The CLC925 incorporates several useful features including tri-statable outputs, offset adjust, gain adjust, and output data formatting. These features are detailed in the subsequent text.

T/H Output, V_{ref}, and Test Points (D.N.C.)

Several internal nodes are brought out of the package. Most of these are test points and should not be connected. Doing so may severely degrade performance or cause internal damage. The exceptions to this are the T/H output and the A/D reference voltage output, both of which are available to the user. Obviously, these nodes are critical to A/D performance and must be used with care – this is particularly true of the inverted T/H output (0V to -2.0V), which should normally be left unconnected.

The use of the -2.000V reference voltage output, on the other hand, is strongly encouraged. The reference output is a highly-stable voltage source, which can drive as little as 1kΩ at full accuracy. (Note: V_{REF} voltage output has been designed for tracking stability. Some variation in the precise output level is possible with various gain adjustment settings.)

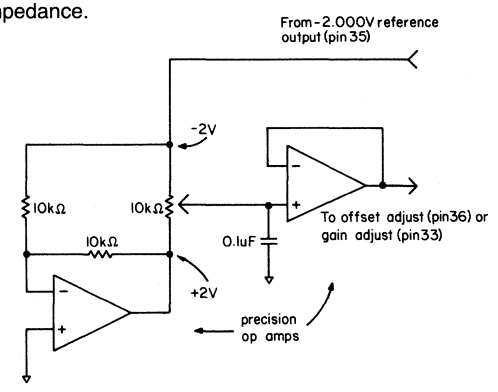
Input Range and Offset Adjustment

The input range of the CLC925 is laser trimmed to $2V_{pp}$ centered around ground (±1V). Additional flexibility has been built into the CLC925 by allowing both positive and negative unipolar operation (positive unipolar . . . 0V to +2V; negative unipolar . . . -2V to 0V). The input offset is determined by the voltage at pin 36.

offset adjust voltage (pin 36)	analog input range
GND	-1V to +1V
-2V	-2V to GND
+2V	GND to +2V

The $2V_{pp}$ input range of the CLC925 may be placed anywhere within the ±2V window.

The offset adjustment pin should be driven from a voltage source that both exhibits a low impedance and is free of excessive noise. A voltage divider between power supplies fails both of these requirements. An elegant approach for this design is to use the CLC925's built-in 2V reference (pin 35). It may be connected directly to the offset adjust pin for a -2V to GND range or it may be used as shown below. The circuit below generates +2V by inverting the -2V reference voltage output. This +2V output may be used directly to provide an input signal range of GND to +2V. The +2V may also be used in conjunction with the -2V output and a potentiometer to provide maximum flexibility in setting the input range and adjusting the offset (as it is below). The unity-gain buffering op amp is needed to drive the adjustment pin with a low impedance.



Input Range and Offset Adjustment Circuit

Adjusting the Full-Scale Range

The 2V full-scale analog input range may be adjusted by up to ±10%. As with the offset adjust pin, the gain adjust pin has a ±2V input range. A voltage of -2V compresses the full scale range by 10%. In other words, with -2V applied to the gain adjust pin, the full scale range is 1.8V. (This effectively increases the gain of the converter by 10%.)

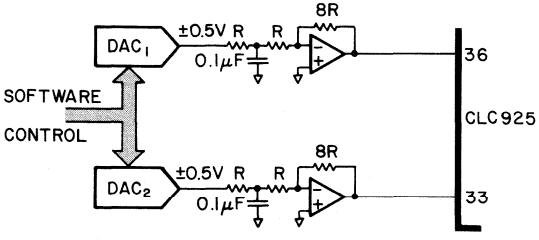
Conversely, applying +2V to the gain adjust pin expands the full scale range to 2.2V. (This effectively decreases the gain of the converter by 10%.) In each case, the expansion or compression is symmetric about "0" . . . both FS and -FS change. In practice, this means the gain adjustments should be made before the offset is adjusted.

gain adjust voltage (pin 33)	analog input range
GND	$2V_{pp}$
-2V	$1.8V_{pp}$
+2V	$2.2V_{pp}$

The circuit considerations which apply to the offset adjust pin also apply to the gain adjust pin (i.e., low source impedance and low noise); the offset adjust circuit may also be used for gain adjustments as indicated on the schematic. If flexibility is desired for both offset and gain adjust, an additional 10kΩ potentiometer and unity gain buffering op amp may be added.

Auto-Calibration

Many systems benefit from the ability to dynamically adjust offset and/or the gain. This is easily accomplished by incorporating a D/A converter into the adjustment circuit above. The computer system drives the D/A and thereby adjusts the voltage applied to the offset and/or the gain adjust pins. Gain adjustments should be made before any offset adjustments.

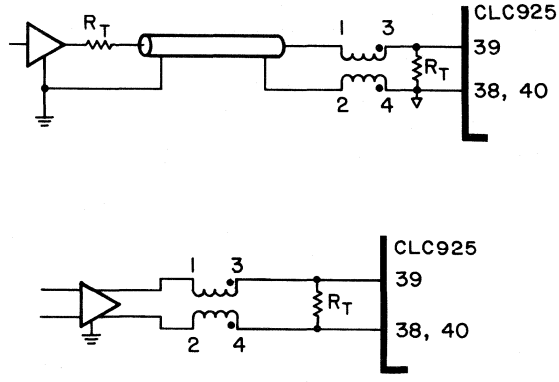


Simple DAC's provide Auto-cal Capability

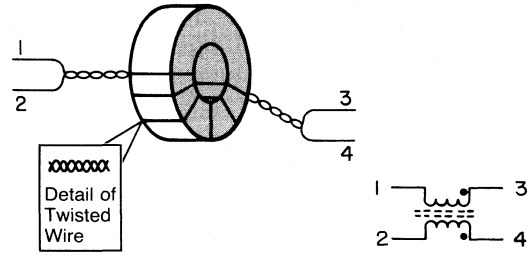
Using a Balun for Impedance Control

Harsh environments may have an excessive amount of noise on signal and ground lines. Much of this type of "common mode" noise can be eliminated from the analog signal path through the use of a balun. A balun is a 1:1 impedance matching transformer which forces equal currents in both the signal and ground paths, forming a common mode choke. The inputs of the balun may be driven from either an isolated signal and ground, or a differential driver; either is acceptable.

A balun is constructed from approximately ten turns of twisted wire (#26 or #28 AWG) wound around a powdered iron toroid. This 1:1 impedance matching circuit should also minimize ground-loop effects.



Typical Balun Circuits



Balun Construction and Use

Timing Considerations

The CLC925 is designed to provide up to 10MSPS (10 million samples per second). This is equivalent to 100ns per conversion cycle. After the rising edge of the CONVERT signal (which initiates the actual conversion cycle), the on-board track-and-hold will move from TRACK mode to HOLD mode, followed by a two-step conversion process. Data is "pipelined" within the CLC925, meaning that data from a specific conversion will take two more conversion cycles to make its way to the CLC925 outputs (see timing diagram page 5).

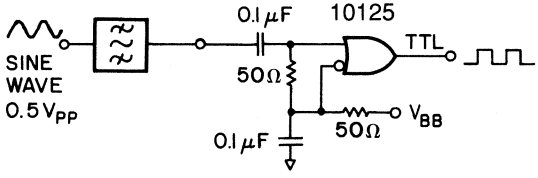
The conversion cycle ends approximately 30ns after rising edge of CONVERT. The CONVERT pulse should remain HIGH during this 30ns interval to prevent the clock transition from corrupting the conversion cycle accuracy. On the other end of the CONVERT cycle (prior to the rising edge which initiates the next conversion cycle), the LOW period should also be at least 40ns long. The on-board track-and-hold will move from HOLD mode to TRACK mode soon after the falling edge of CONVERT. The CLC925 requires just less than 30ns of track time for rated performance, hence the 30ns CONVERT pulse width LOW requirement. Both t_{PWH} and t_{PWL} for CONVERT may be extended much longer in time, although no increase in conversion accuracy should be expected.

There is no lower bound for the CLC925 conversion rate. In other words "dc" clocks are acceptable, but the edge transition times should be less than 20ns for proper operation.

Convert Clock Considerations

The CLC925 requires a TTL level clock signal to control the conversion timing. On each rising edge of the CONVERT signal, the CLC925 will initiate a conversion sequence. The quality and purity of the clock signal has a major impact on the quality and accuracy of the conversion process. Essentially what the CLC925 requires is an extremely low jitter clock source, at least as good as the CLC925 aperture jitter specification at 4.5ps(rms). Excessive jitter will manifest itself as broad-band noise, severely degrading the converter's accuracy.

The low clock jitter requirements eliminate nearly all commercial pulse generators, and most signal sources, at least in terms of their direct output. A simple method of "squaring up" low-jitter clock signals, is to use a narrow-band pass filter to generate a pure sine wave at the conversion frequency. This signal is then "squared up" using a modified ECL-to-TTL translator. This technique should allow most low-jitter signal sources to be used without loss of conversion accuracy. A detailed circuit is illustrated below.



SINE to TTL Conversion Circuit

If the signal-to-noise ratio is below expectations and the input signal is not noisy, clock jitter should be investigated.

$$SNR_{MAX} = 20LOG\left[\frac{1}{2\pi f_{in}\ Jitter_{RMS}}\right]$$

where . . .

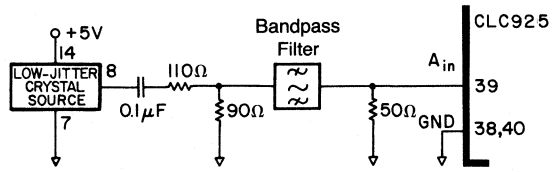
$$Jitter_{RMS} = \sqrt{(Clock\ Jitter_{RMS})^2 + (Analog\ Jitter_{RMS})^2}$$

Crystal Sources

Standard crystal controlled TTL oscillators are a very cost-effective and a convenient source of high purity clock signals. The inherently low jitter present in such sources is ideal for ADC testing and evaluation. Additionally, crystal sources are an excellent source, once filtered, for use as an analog input signal, particularly in test and evaluation applications.

Output Latching

The CLC925 ouput data will, in most cases, be placed in a buffer memory prior to further processing. This may require higher digital drive capability than the CLC925 can provide. To overcome this, output latches should be placed just after the CLC925.



Low Jitter Crystal Source with Bandpass Filtering

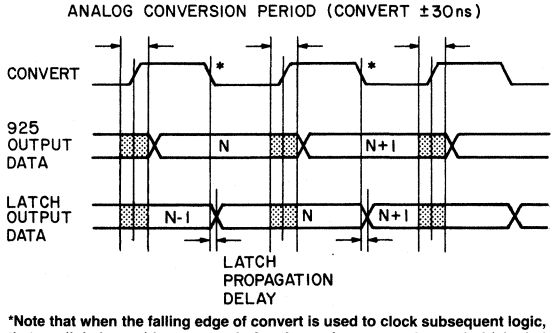
The timing of these latches can play a major role in the conversion accuracy. Some of the issues involved here are minimizing digital feedthrough to the analog signal, digital corruption of the conversion process, digital corruption of the output data, and proper setup and hold time condition.

Data Ready

The most critical portion of the conversion cycle is the 30ns after the rising edge of CONVERT (the actual conversion period) and the 15ns window just before the rising edge of CONVERT (the final track-and-hold setting period just prior to the conversion). Any digital switching, latches or otherwise, may seriously undermine the CLC925 conversion accuracy. In other words . . . the use of the CONVERT Clock (rising edge) as a DATA READY signal, may inject digital switching noise back onto the analog input signal.

Using the rising edge of CONVERT for a DATA READY signal means that no more than 10ns of hold time is available to external logic. On the other hand, assuming 10MSPS and a 50% duty cycle CONVERT clock, better than 40ns of setup time is available with 60ns hold time, provided the falling edge of CONVERT is used as a DATA READY.

The falling edge DATA READY will place latch and bus transitions after the internal conversion cycle, but also well before the critical final setting interval for the on-board track-and-hold. This technique is particularly effective when used with a 50% duty cycle CONVERT clock. Assuming the worst-case timing at 10MSPS operation, the falling edge of CONVERT used as a DATA READY will be approximately 20ns after the internal conversion is complete, and a full 20ns before the on-board track-and-hold enters track mode for the next cycle. This should allow switching transients to die down, even in a very noisy digital system, before the next analog digitization takes place.



***Note that when the falling edge of convert is used to clock subsequent logic, that no digital transitions occur during the analog conversion period (shaded region ±30ns around the rising edge of convert)**

Recommended Latch/DATA READY Timing

Output Coding

The CLC925 offers two output coding formats, Offset Binary and Two's Complement. "Offset Binary" assumes a bipolar input range for convenience, but essentially it denotes all zeroes for the most negative input representation, and all ones for the most positive input representation. The Two's Complement format also assumes a bipolar input, but inverts D1(MSB) to provide the proper coding.

Both output formats function normally if offset input ranges are employed (i.e., unipolar, positive, or negative). The selection of output formats is made by choosing whether D1(MSB) or $\overline{D1(MSB)}$ is used as a data output.

Analog Input	Offset Binary	Two's Complement
FS-1LSB	111111111111	011111111111
FS-2LSB's	111111111110	011111111110
FS-3LSB's	111111111101	011111111101
–	–	–
–	–	–
mid-scale + 1/2LSB	100000000000	000000000000
mid-scale – 1/2LSB	011111111111	111111111111
–	–	–
–	–	–
-FS + 2LSB's	000000000010	100000000010
-FS + 1LSB	000000000001	100000000001
-FS	000000000000	100000000000

Grounding

All of the CLC925 grounds are internally connected. Pins 1, 6, 21, and 40 are connected through the package itself; these are further connected to all other ground pins by way of the substrate and bond wires.

The CLC925 has been designed to incorporate a single ground plane for both digital and analog return currents. A "split" ground plane (one for digital components and another for analog components) is not recommended. Although a split ground approach is not recommended, certain types of systems preclude the use of a single ground plane. For these systems, the following chart matches signals and return currents so that the most appropriate grounding choices can be made.

Signal/ Power	Ground Return	Primary Activity
2, 3, 34	1	T/H Power Supply Pins
7, 26, 32	6	Quantizer Power
8-20, 22	21, 23	Digital Output Stage Power
29, 31	30	Digital Processing Power
39	38, 40	Analog Input Signal

NOTE: Pins 1, 6, 21, and 40 are connected through the package metalization itself.

Power Supplies and Decoupling

The CLC925 does not require separate analog and digital power supplies as is often recommended for high-performance data converters. The design is well-balanced internally and includes on-board decoupling capacitors. As with any high-performance circuit, supply variations can degrade performance. DC variation of supplies, within the rated ±5% range, should have only a minimal effect on performance. AC supply variation can be more troublesome. The CLC925 operates with a power supply rejection ratio (PSRR) of better than -50dB. Even so, adequate supply decoupling will help to ensure rated performance.

The recommended supply decoupling scheme is as follows:

Option #1: One 0.1μF ceramic capacitor at each supply pin, with a 5-10μF electrolytic or tantalum for each of the three main supply feeds (proximity not critical).

Option #2: One 0.1 to 0.033 chip capacitor at each supply pin, with a 5-10μF electrolytic or tantalum for each of the three main supply feeds (proximity not critical).

Please note that supply feeds, with excessive digital switching noise from other sources, may require additional filtering.

Layout Considerations

The CLC925 has been designed to be easily accommodated on a printed circuit board; for example, the inputs enter one side of the package and the ouputs leave on the opposite side, with the analog and digital connections widely separated from one another. The PC board should exhibit similar layout guidelines. If the analog input signal has had to travel more than a few inches to reach the analog input pin (V_{IN}), proper termination techniques should be followed to avoid reflections caused by improper impedance matching. Special care should also be exercised to place external output latches close to the CLC925 digital outputs.

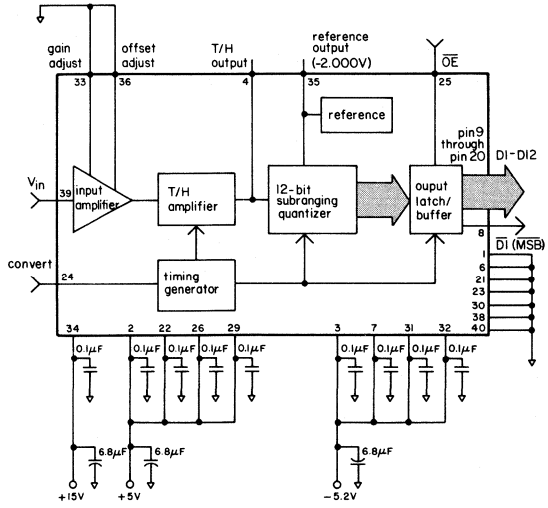
Sockets are not recommended, in that they increase both lead inductance and inter-lead capacitance. If sockets must be used, Teflon or "pin" type sockets should minimize this effect. Additionally, the "Recommended Power Supply Decoupling Scheme" illustrates an effective bypass arrangement. Chip capacitors are preferred and should be located as close as practical to the individual supply pins.

CLC925 Evaluation Board Support

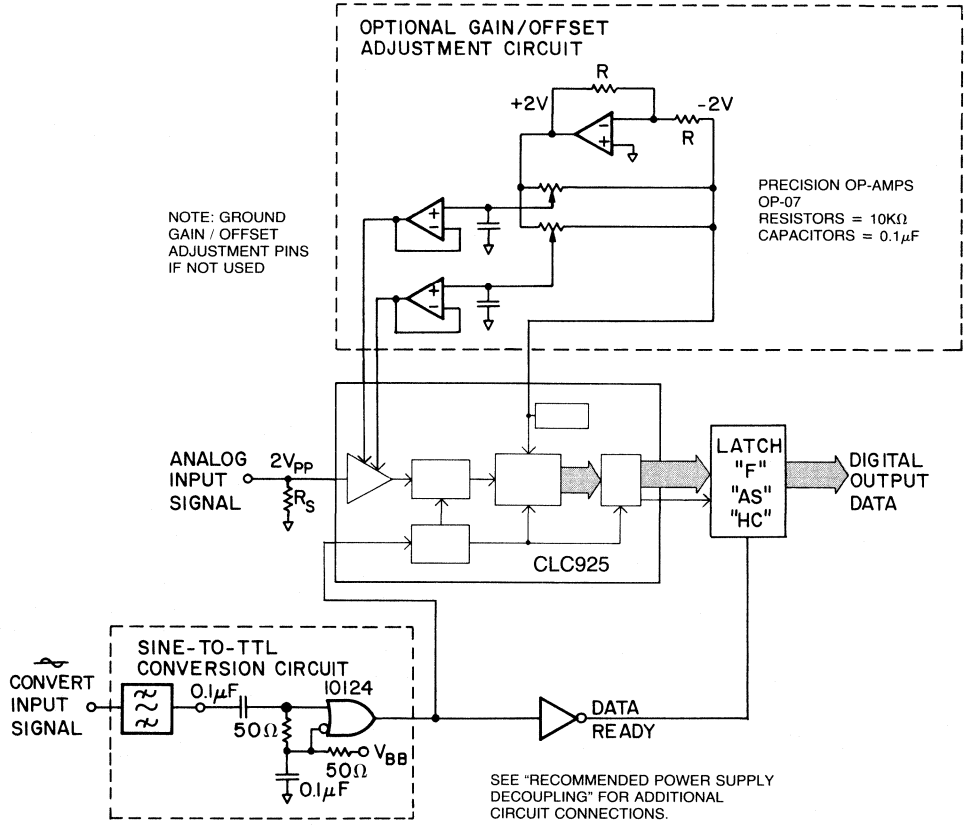
An evaluation board (Comlinear part number 730015) is available for the CLC925 at minimal cost. It is designed to provide a simple platform for evaluating the CLC925.

Applications Assistance

Comlinear maintains a staff of R&D-level applications engineers, who are available for design and applications assistance at (303) 226-0500.



Recommended Power Supply Decoupling Scheme



Complete System Architecture with Offset and Gain Adjustment

Comlinear Corporation

12-Bit, 15MSPS A/D Converter

CLC935

APPLICATIONS:

- radar processing
- infrared processing/ electronic imaging
- instrumentation
- medical imaging
- transient-signal recorders

FEATURES (typical):

- 77dB spurious free signal range; f_{IN}=7.22MHz
- no missing codes guaranteed
- 0.7LSB differential linearity
- small package (2.28in²)

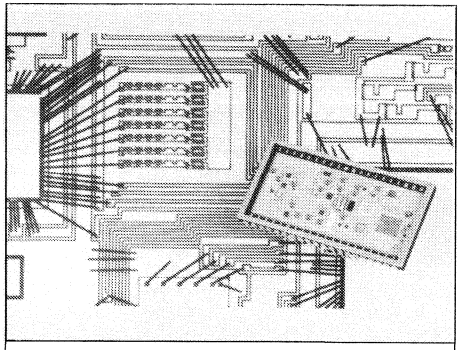
DESCRIPTION:

The CLC935 is a 12-bit analog-to-digital converter hybrid, including voltage references, track-and-hold, and 12-bit quantizer with ECL compatible outputs. The CLC935 has been especially optimized for a Spurious-Free-Signal-Range of better than 70dB. The CLC935 is constructed using advanced thin-film hybrid technology in a fully certified MIL-STD-1772 facility.

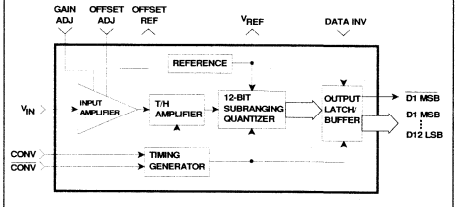
Comprehensive dynamic testing on every part ensures that system performance goals will be met, including spurious-free-signal-range (SFSR) of 77dB from 408kHz to 7.22MHz. This, coupled with an SNR specification of 66.5dB@7.22MHz, means that the CLC935 is ideally suited for use in areas such as radar and instrumentation signal processing.

The CLC935 incorporates a complete two-pass subranging architecture, constructed from several high-speed building blocks. A broadband (135MHz) input amplifier buffers input signals and provides an accurate drive signal to the on-board track-and-hold. Laser trimmed gain and offset circuits assure accurate matching unit to unit. The latched outputs of the CLC935 mean that only a convert clock, analog input, and power supplies are required for operation; internal logic generates all required timing signals.

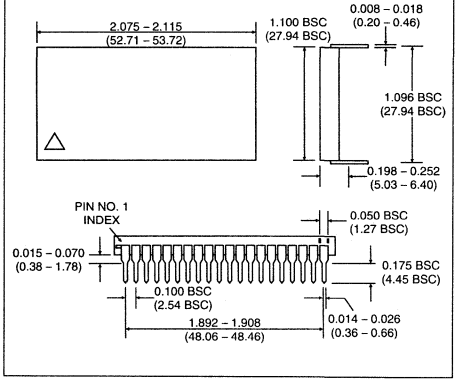
The CLC935AC is specified over a temperature range of 0°C to +70°C, while the CLC935A8C is specified over a range of -55°C to +125°C. Both devices are packaged in 40-pin, 1.1in wide, ceramic DIPs (note: leads are side brazed for easy access and inspection). Contact factory for availability of "gull-wing" surface-mount versions.



Block Diagram



Package Dimensions



Ordering Information		
CLC935AC	0°C to +70°C	industrial version
CLC935A8C	-55°C to +125°C	MIL-STD-883, class B
DESC SMD 5960-92039		

Both versions of the CLC935 are manufactured in Comlinear's MIL-STD-1772 certified facility in Fort Collins, Colorado, U.S.A.

Comlinear Corporation * **4800 Wheaton Drive, Fort Collins, CO 80525** * **(303) 226-0500** * **FAX (303) 226-0564**

DS935.00

January 1993

Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_2$ = -15.0V; $-V_{EE}$ = -5.2V; unless specified)

PARAMETER[1]	CONDITIONS	TYP	MAX & MIN RATINGS						UNITS	SYMBOL
			CLC935AC			CLC935A8C				
Case Temperature		+25°C	0°C	+25°C	+70°C	-55°C	+25°C	+125°C		
DYNAMIC CHARACTERISTICS										
small signal bandwidth	V_{IN} = 1/4 FS	135	95	100	100	90	100	105	MHz	SSBW
large signal bandwidth	V_{IN} = FS	125	75	75	75	75	75	75	MHz	LSBW
slew rate		450	300	300	300	300	300	300	V/µs	SR
overvoltage recovery time	V_{IN} = 2FS	14	25	25	25	25	25	25	ns	OR
effective aperture delay		-0.4	-1.5	-2.0	-2.0	-1.5	-2.0	-2.0	ns	TA
aperture jitter		1.25	2.5	2.0	2.0	2.5	2.0	2.0	ps(RMS)	AJ
NOISE and DISTORTION (15MSPS)										
* signal-to-noise ratio										
(not including harmonics)	408kHz; FS	67.4	65.0	66.0	66.0	62.0	66.0	65.0	dB	SNR1
	4.996MHz; FS	67.0	65.0	65.0	65.5	62.0	65.5	65.0	dB	SNR2
	7.220MHz; FS	66.5	64.0	66.0	65.0	62.0	65.0	65.0	dB	SNR3
* in-band harmonics										
	408kHz; FS-1dB	-77.2	-74.0	-74.0	-70.0	-69.0	-74.0	-67.0	dBc	IBH1
	4.996MHz; FS-1dB	-77.0	-69.5	-72.0	-70.0	-67.0	-72.0	-65.0	dBc	IBH2
	7.220MHz; FS-1dB	-77.0	-69.5	-72.0	-68.0	-65.0	-72.0	-64.0	dBc	IBH3
* spurious-free-signal-range										
	408kHz; FS-1dB	77.2	74.0	74.0	70.0	69.0	74.0	67.0	dB	SFSR1
	1.98MHz; FS-1dB	77.0	69.5	72.0	70.0	67.0	72.0	65.0	dB	SFSR2
	4.99MHz; FS-1dB	77.0	69.5	72.0	68.0	65.0	72.0	64.0	dB	SFSR3
intermodulation distortion (f_1=4.95MHz@FS-6.5dB; f_2=5.05MHz@FS-6.5dB)		75							dBc	IMD
noise-power-ratio (dc to xxMHz white noise; xxMHz slot)	FS-12dB								dB	NPR
DC ACCURACY and PERFORMANCE										
differential non-linearity	dc; FS	0.7	1.0	1.0	1.0	1.0	1.0	1.0	LSB	DNL
integral non-linearity	dc; FS	1.3	2.0	2.0	2.0	3.0	2.0	3.0	LSB	INL
missing codes		0	0	0	0	0	0	0	codes	MC
bipolar offset error		3.0	12	10	15	30	10	20	mV	VIO
temperature coefficient			300		250	300		250	µV/°C	DVIO
bipolar gain error		1.2	2.2	2.0	2.2	3.0	2.0	3.0	%FS	GE
temperature coefficient			0.07		0.05	0.07		0.05	%FS/°C	DVIO
ANALOG INPUT PERFORMANCE										
analog input bias current		10	45	25	35	45	25	35	µA	IBN
temperature coefficient		100	250		100	250		100	nA/°C	DIBN
analog input resistance		80	50	50		25	50		kΩ	RIN
analog input capacitance		3.5	5.5	5.5	5.5	5.5	5.5	5.5	pF	CIN
POWER REQUIREMENTS										
* supply current ($+V_{CC}$ = +5.0V)	15MSPS; no load	119	150	150	150	150	150	150	mA	ICC
* supply current ($-V_{EE}$ = -5.2V)[4]	15MSPS; no load	769	960	960	960	960	960	960	mA	IEE
* supply current ($+V_1$ = +15.0V)	15MSPS; no load	16.3	20	20	20	20	20	20	mA	I1
* supply current ($-V_2$ = -15.0V)	15MSPS; no load	28.2	35	35	35	35	35	35	mA	I2
nominal power dissipation[4]	15MSPS; no load	5.26							W	PD

Note 1: Parameters preceded by an * are 100% tested. AC units are tested at 25°C and guaranteed at 0°C and 70°C.

Note 2: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Note 3: Junction temperature rise above case = 16°C; θ_{CA}=16°C/W; θ_{CA}=7°C/W@500LFPM. Use of a SIL-PAD® #550007, from Berquist (1-800-347-4572), can lower case-to-ambient rise; θ_{CA} = 12°C/W@still air, 12in² ground-plane; θ_{CA}=3.4°C/W@100LFPM, 12in² ground-plane.

Note 4: Planned product improvements are expected to lower -5.2V supply current, as well as nominal power dissipation.

Electrical Characteristics ($+V_{CC}$ = +5.0V, $+V_1$ = +15.0V, $-V_1$ = -15.0V, $-V_{EE}$ = -5.2V unless specified)

PARAMETER[1]	CONDITIONS	TYP	MAX & MIN RATINGS						UNITS	SYMBOL
			CLC935AC			CLC935A8C				
Case Temperature		+25°C	0°C	+25°C	+70°C	-55°C	+25°C	+125°C		
DIGITAL INPUTS										
input voltage	logic LOW		-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	V	VIL
	logic HIGH		-1.1	-1.1	-1.1	-1.1	-1.1	-1.1	V	VIH
input current	logic LOW		1.0	1.0	1.0	1.0	1.0	1.0	mA	IIL
	logic HIGH		1.0	1.0	1.0	1.0	1.0	1.0	mA	IIH
DIGITAL OUTPUTS										
output voltage	logic LOW		-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	V	VOL
	logic HIGH		-1.1	-1.1	-1.1	-1.1	-1.1	-1.1	V	VOH
TIMING										
maximum conversion rate			15	15	15	15	15	15	MSPS	CR
minimum conversion rate		0	0	0	0	0	0	0	MSPS	CRM
data hold time		6	3	4	3	3	4	3	ns	THLD
output propagation delay		10	15	15	15	15	15	15	ns	TDV

Recommended Operating Conditions

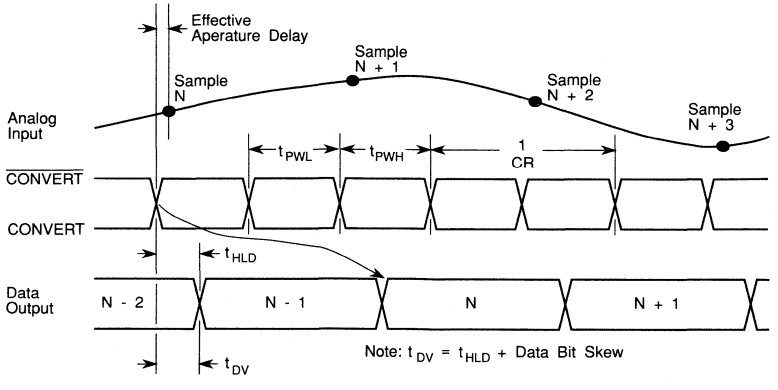
positive supply voltage ($+V_{CC}$)	+5V
positive supply voltage ($+V_1$)	+15V
negative supply voltage ($-V_{EE}$)	-5.2V
negative supply voltage ($-V_1$)	-15V
differential voltage between any two GND's	<10mV
analog input voltage range (Full Scale)	±1V
digital output current sinking	6mA(max)
sourcing	6mA(max)
digital input voltage range	-2.0V to 0.0V

Absolute Maximum Ratings[2]

positive supply voltage ($+V_{CC}$)	-0.5 to +7.0V
positive supply voltage ($+V_1$)	-0.5 to +18V
negative supply voltage ($-V_{EE}$)	+0.5 to -7.0V
negative supply voltage ($-V_1$)	+0.5 to -18.0V
differential voltage between any two GND's	200mV
analog input voltage range	$-V_{EE}$ to $+V_{CC}$
DIGITAL input voltage range	+0.5V to $-V_{EE}$
gain and offset adjust voltage range	$-V_{EE}$ to $+V_{CC}$
output short circuit duration (one pin to ground)	Infinite
Junction Temperature	+175°C
Operating Temperature Range[3]	
CLC935AC	0°C to +70°C
CLC935A8C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Solder Duration (+300°C)	10 sec

10

Timing Diagram



Understanding A/D Dynamic Specifications

Analog-to-Digital converters are specified in many ways. As a component achieves higher performance, its specifications and their definitions can become more critical. Fortunately, the vast number of converter applications can generally be placed into one of two classes. These are processed data and non-processed data applications. The distinction seems quite simple but the split implies a completely different approach in specifying A/D converters for a given application.

The processed data area includes the frequency domain applications which employ Fourier processing (FFT). Also in this category are the highly averaged applications, usually concerned with low noise. In each case, the converter's data is averaged or convolved mathematically. This processing reduces the apparent noise level in the output data. For FFTs, the noise is simply spread over a large number of frequency bins. For simple averaging approaches, the gaussian distribution of noise is greatly reduced, appearing to increase the converter's resolution. Processed applications include radar, network and spectrum analyzers, communications receivers, etc.

The non-processed applications tend to take the converter's data in its original form with very little processing. This means that the noise reduction benefits of the processed applications are not seen. The non-processed area is composed primarily of time domain applications like imaging, DSO's, ultrasound, etc.

The processed vs. non-processed issue has several implications in terms of converter specifications. For the non-processed (time domain) systems the dominant converter specifications deal with noise (SNR) and converter accuracy (DNL). The converter's quantization noise and input stage noise dominate converter accuracy . The harmonic distortion (primarily INL) of the converter is generally of little interest given that most time domain applications present data for visual analysis and tend to focus on "local" accuracy rather than over the full input range. "Local" accuracy is best described through the standard noise measurements, such as SNR and DNL.

In the frequency domain application areas, the noise of the converter is processed to the point where, for almost all systems, it is no longer of issue. This is manifested as a reduction in the apparent noise floor. The actual RMS noise is not reduced, but is spread over more and more frequency bins as processing levels are increased. Unfortunately, the harmonic distortion performance of the converter is not affected by increased processing. This makes the harmonic performance, or more specifically the spurious performance, the dominant error source for frequency domain applications. SFSR becomes the dominant specification for determining converter performance in the frequency domain.

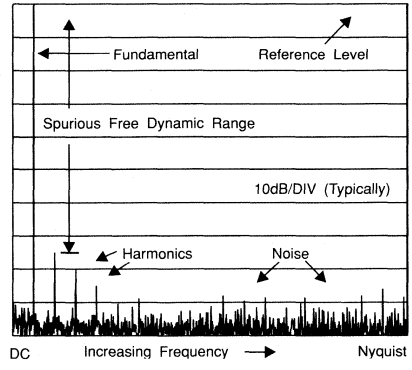
Signal-to-Noise Ratio (SNR) is the ratio of the power contained in the fundamental signal compared to the power contained in the entire noise floor. That is to say all individual noise components are added together to arrive at an integrated noise power. For SNR, harmonic power is excluded from the noise measurement. SNR is particularly important in time domain applications like digital image processing and infrared imaging, where conversion accuracy can be heavily degraded by integrated noise.

Signal-to-Noise-and-Distortion (SINAD) is the ratio of the fundamental signal power to the power at all other frequencies. This includes all noise as well as all harmonics. SINAD is a worst case specification for A/D converters, combining variables from both frequency and time domains. The value of SINAD in high-performance converter applications is not clear since it does not accurately predict the best converter for a given application. Because applications tend to fall into time domain/non-processed or frequency domain/processed applications, those specifications more directly related to the application should be the primary focus in selecting the converter.

Total Harmonic Distortion (THD) is the combined power of a specified number of harmonics, compared to the power of the fundamental signal. Harmonics are located at predictable frequencies, spaced at integer multiples of the fundamental signal. For example, a 1MHz fundamental would generate harmonics at 2MHz, 3MHz, 4MHz, ... and so on. In practice, only the first five harmonics contribute significantly to THD, although more may be included in the measurement. THD does not tend to apply well in frequency domain applications which are by their nature very SFSR oriented. In time domain applications, THD is indicative of full-scale input range distortion, however the high-performance time domain applications are generally most interested in local distortion performance. Local distortion and accuracy is dominated by DNL. The use of THD for applications requiring local performance is not likely to yield accurate or repeatable results in selecting the correct converter.

Spurious-Free-Signal-Range (SFSR) is the "clean" dynamic range of the converter, free from harmonic and spurious signals. SFSR is ratio of the power of the fundamental compared to the power of the next largest component in the frequency spectrum. The SFSR specification is especially important to frequency domain applications which perform Fourier transforms to analyze the converter's output data. Processed applications like radar and network analyzers are typical areas where SFSR offers a direct prediction of converter's performance at both the system and component levels. SFSR is the single best specification for selecting a converter to be used in a frequency domain application.

In-Band Harmonics (IBH) is the ratio of the power of the fundamental compared to the power of the single largest harmonic. This specification is very similar to SFSR, but since it only considers a fairly limited number of harmonics, it is potentially an incomplete gauge of converter performance. SFSR is more stringent and should be used whenever possible in lieu of IBH.



Typical Frequency Spectrum and its Components

Some of the performance plots that follow require more explanation than is feasible in the caption. This section goes into more detail as to how these plots were generated, and how they might be interpreted. Additional information can be found in the application note AD-01 ... Designing with High-Performance A/D converters"

Spectral Plots
The output frequency spectrum is shown for input frequencies of 406KHz, 4.9MHz and 7.2MHz. All of these plots were generated with a 15MSPS Clock. Four thousand point (4K) FFT's were taken, using a Blackmann-Harris window and the power spectra were averaged over 10 cycles to accentuate the harmonics and reduce variance in the noise level. The plots show the frequency spectrum from dc to the 7.5MHz Nyquist frequency for 15MSPS.

SFSR and SNR vs Input level Plots
As the signal level is reduced from full scale, the noise level remains relatively constant. This results in a backward declining straight line shown as SNR vs Input Amplitude. In some converters the 'noise' is not independent of the input signal level and hence the line may not be straight. The 74dB theoretical limit on SNR is shown with the -1dB/dB backward declining slope for reference. The CLC935 noise performance parallels this reference, and indicates that noise performance is relatively uniform for all analog input levels.

The SFSR performance is somewhat less uniform. As the ratio of the largest non-fundamental frequency component relative to the fundamental, it is more susceptible to random variations in the spectrum. The input power was measured at the A/D converter. For each amplitude a 4K point FFT was taken and analyzed to determine the SNR and SFSR. The vertical scale is measured in dBc, this is dB relative to the test signal, and the horizontal scale is dB-FS which is dB relative to the converter's full-scale analog input range.

Two Tone Linearity Spectrum
In a linear system, the input signal can be viewed mathematically as a superposition of sinusoids (Fourier Transform). The system output can be predicted by the superpositioning of the individual effects on each of the sinusoid inputs. For example, if a linear network is presented with a single tone signal F_1 and the result is an attenuation by a factor A_1, and it is then presented with another frequency F_2 attenuated by A_2 through the system, then the expected output for an input of F_1+F_2 would be $A_1F_1 + A_2F_2$.

If the network is not linear, the output will contain frequency components in addition to those present at the input. The most common frequencies likely to be present in the output are at $MF_1 \pm NF_2$, where M and N are integers, and F_1 and F_2 are the two input frequencies. In the *two-tone linearity* plot, the input to the CLC935 consists of 4.95MHz and 5.05MHz superpositioned sinusoids. Intermodulation terms on the order of -80dBc confirm the CLC935's excellent linearity.

SNR, and SFSR vs Input Frequency
These plots shows the variation in converter performance relative to analog input frequency. Input frequencies to about 65MHz (the Full-Power-Bandwidth) are included, and should be useful for over-sampling applications. Beyond the full-power-bandwidth, performance for large signals degrades quickly. The small-signal-bandwidth (measured with analog inputs below $200mV_{PP}$) performance does not degrade until around 135MHz.

SNR vs Conversion Rate
There are several critical timing processes inside the converter, including the track time, the time allowed for settling of internal nodes, and time to perform the coarse and fine quantizations. When a rising edge of CONVERT is detected, a pre-timed sequence of events is set into motion. Accordingly the performance of the CLC935 is very independent of clock rate, up to the specified speed of 15MSPS, after which performance can degrade rapidly. If a higher speed conversion is required, the CLC936, 12-bit 20MSPS A/D converter is recommended. The CLC936 is pin compatible with the CLC935, providing an easy upgrade path.

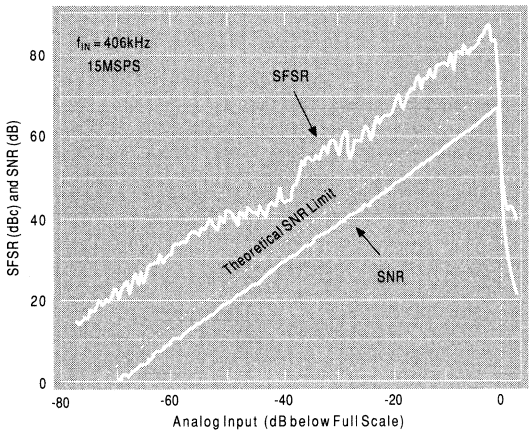
Digital output skew plot
The digital outputs make their transition T_{DV}ns after the rising edge of the CONVERT signal. The actual time to this transition varies slightly from output bit to output bit. The amount of this variation is small , and well within the timing needs for this type of system. In the *Bit Skew* plot, all 12 output bits are shown for various transitions. As can be seen, the total variation, bit-to-bit, is about 2ns.

Pulse response plots
This plot has been generated with a $1V_{PP}$ flat top pulse input signal with a 600ps rise time and a 15.000549MHz repetition rate. The input signal is effectively aliased to 549Hz when sampled at 15MSPS.

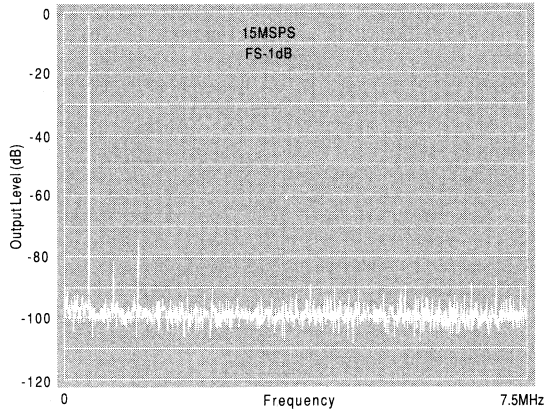
A sequence of 4096 samples will now represent an equivalent time window of 10ns. Any slew rate limitations, ringing or other non-idealities in the A/D analog input stage will now be apparent in the aliased output signal. As can be seen from the plots, the only non-ideality is a bandwidth limitation, which limits the time to an accurate sample to about 7ns. If your input signal is a step function, such as a CCD output or T/H output, this means that the sample should be taken at least 7ns after the start of the transition.

Typical Performance Characteristics (T_A = +35°C, 15MSPS unless specified)

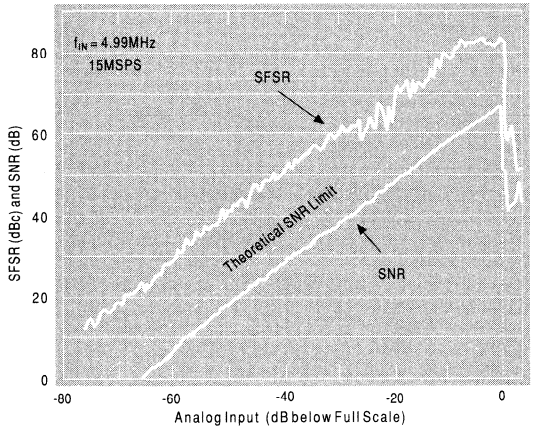
SFSR & SNR vs. Analog Input Amplitude



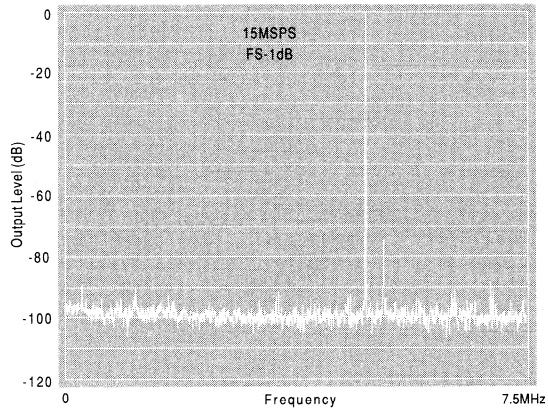
406kHz Output Spectrum



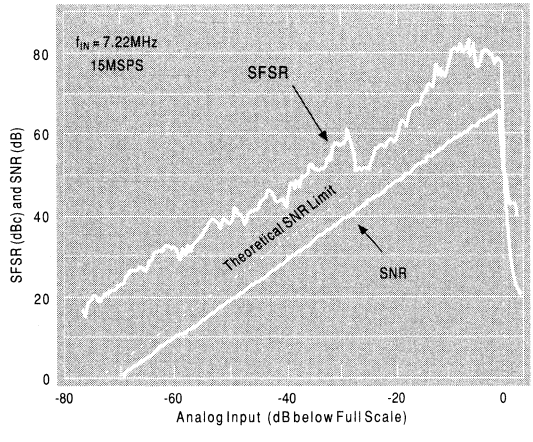
SFSR & SNR vs. Analog Input Amplitude



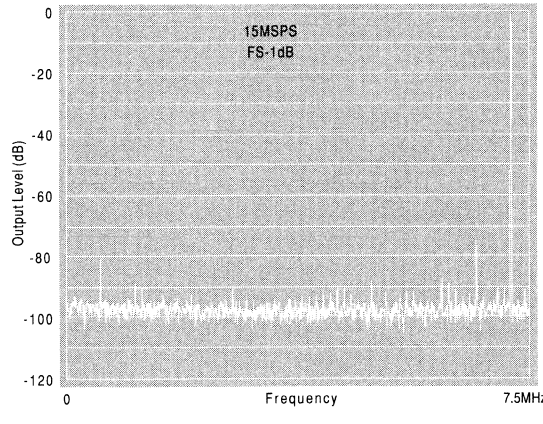
4.99MHz Output Spectrum



SFSR & SNR vs. Analog Input Amplitude

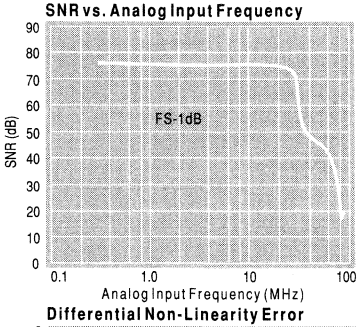


7.220MHz Output Spectrum

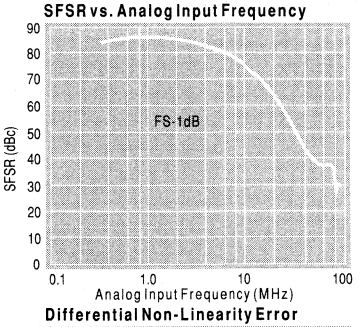


Typical Performance Characteristics (T$_A$ = +35°C, 15MSPS unless specified)

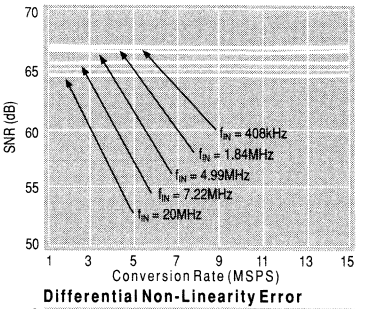
SNR vs. Analog Input Frequency



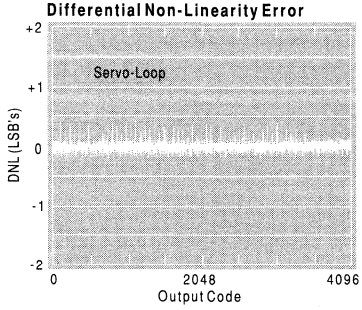
SFSR vs. Analog Input Frequency



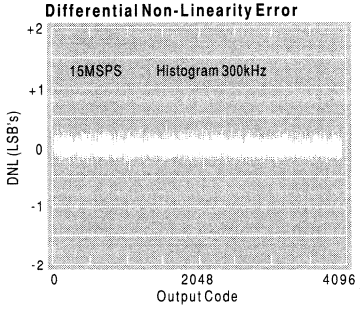
SNR vs. Conversion Rate



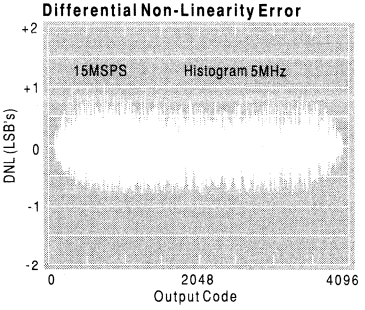
Differential Non-Linearity Error



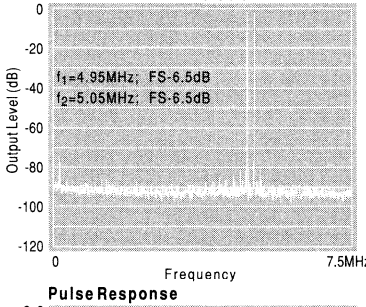
Differential Non-Linearity Error



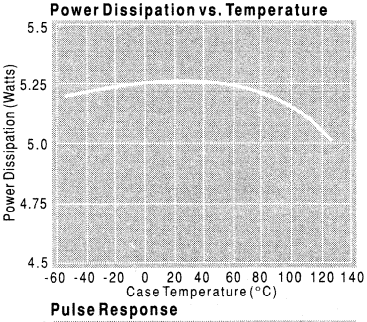
Differential Non-Linearity Error



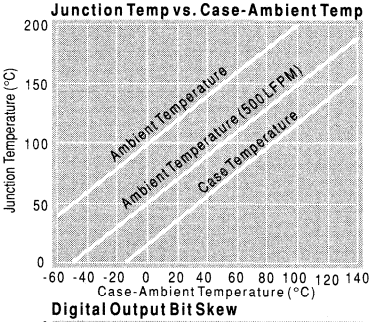
Two-Tone Intermodulation Distortion



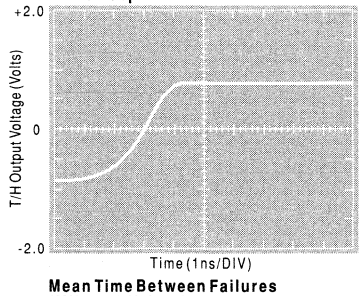
Power Dissipation vs. Temperature



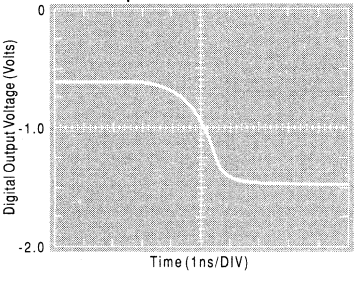
Junction Temp vs. Case-Ambient Temp



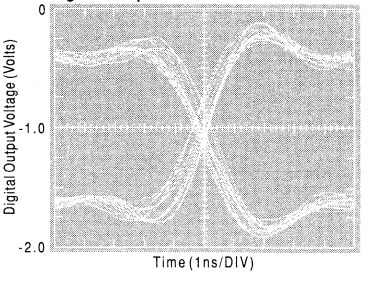
Pulse Response



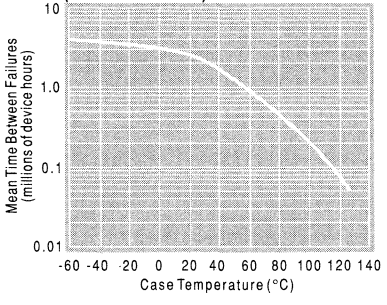
Pulse Response



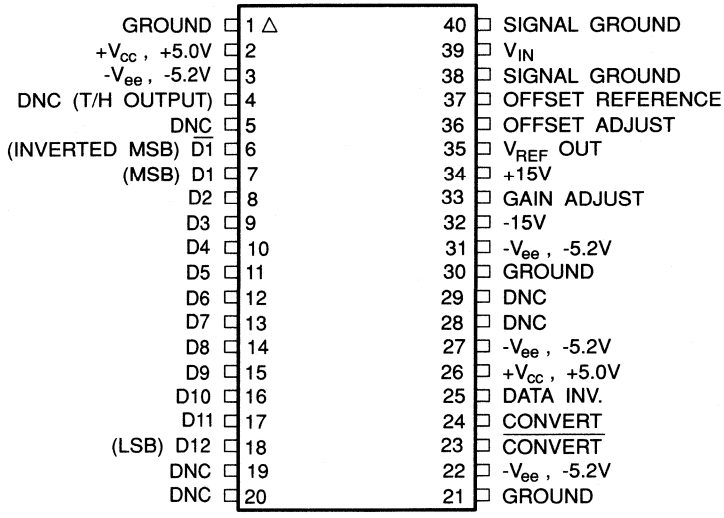
Digital Output Bit Skew



Mean Time Between Failures (MIL-HDBK-217E)



CLC935 Pinout



Pin Description and Usage

ECL-Level Digital Inputs

CONVERT, $\overline{\text{CONVERT}}$ — *Pins 23, 24*
"Differential Convert Command" initiates a new conversion cycle on the rising edge of CONVERT.

DATA INV — *Pin 25*
DATA INVERT is an active HIGH (grounded) ECL input which causes the data outputs [D2 to (LSB) D12] to be inverted. In normal operation, DATA INV is left floating or tied to ECL logic LOW.

ECL-Level Digital Outputs

(MSB) D1-D12 — *Pins 7 to 18*
Digital Data Outputs. D1 is the MSB; D12 is the LSB. In their normal state, the digital outputs offer Offset Binary output coding.

$\overline{\text{(MSB) D1}}$ — *Pin 6*
Inverted version of the MSB, used for 2's Complement coding.

Analog Input

V_{IN} — *Pin 39*
Analog input with a $2V_{PP}$ input range from +1V to -1V.

Gain Adjust — *Pin 33*
The GAIN ADJUST has a +4V to +1V input range and scales the analog input full-scale range by -10% to +10% respectively. If unused, Gain Adjust should be left floating.

Offset Adjust — *Pin 36*
The OFFSET ADJUST has a GROUND to OFFSET REFERENCE input range and scales the analog input offset by ±0.1V. If unused, Offset Adjust should be left floating.

Offset Reference — *Pin 37*
The OFFSET REFERENCE tracks gain adjustments and is used for offset voltage adjust.

Miscellaneous

V_{REF} — *Pin 35*
V_{REF} is a highly stable +2.500V voltage reference. (Recommended current drain ≤2mA.)

D.N.C — *Pins 5, 19, 20, 28, 29*
Do Not Connect.

DNC (T/H Output) — Pin 4
Internal Track-and-Hold output voltage test point. Do not Connect.

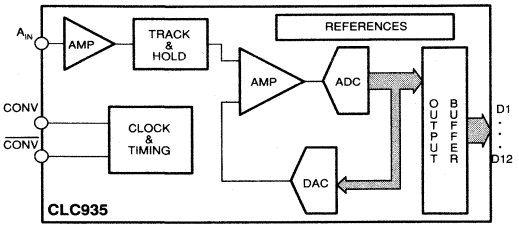
Power and Ground

+5V, Pins 2,26; +15V, Pin 34; -5.2V, Pins 3, 22, 27, 31; -15V, Pin 32; GROUND, Pins 1, 21, 30, 38, 40.

In high-speed data acquisition systems, overall performance is usually determined by the A/D converter. Accordingly, special attention should be given to the converter, its operation, and its environment. To assist in this process, information on these critical items has been included in this data sheet. Additional information on using high-performance A/D converters can also be found in Comlinear Corporation application note AD-01.

Principle of Operation

The CLC935 is a complete two step, subranging A/D converter, with input buffering, internal track-and-hold, quantizer, and all necessary voltage references. The block diagram for the converter is shown below.

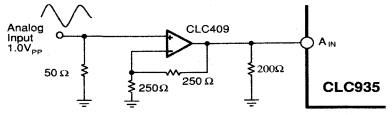


CLC935 Functional Block Diagram

The conversion cycle is initiated on the rising edge of the CONVERT signal. The analog input is sampled by the track-and-hold amplifier and is then digitized with an 8-bit digitizer. The 6 MSBs of this conversion are the "coarse-quantization", which drive a 14-bit accurate DAC to match the input level. The DAC output is then subtracted from the original analog input to generate an error signal, which is then digitized. The two digitized results are combined to form the 12-Bit accurate output. Error correction and output buffering are also provided by the CLC935.

Analog Input Driving Circuits

The high dynamic range of the CLC935 places high demands on any analog processing circuitry that precedes the converter. This is particularly true in the area of harmonic distortion where the CLC935's performance often exceeds -77dBc. Fortunately the CLC935 employs an internal buffer for the analog input, and external buffering circuits are usually not required. Both the CLC207 and the CLC409 amplifiers can be configured for better than -80dBc harmonic distortion (note that the CLC409 does not support 12-bit settling performance necessary for "time domain" applications). This makes them ideal choices for any analog signal conditioning or buffering that may be required.



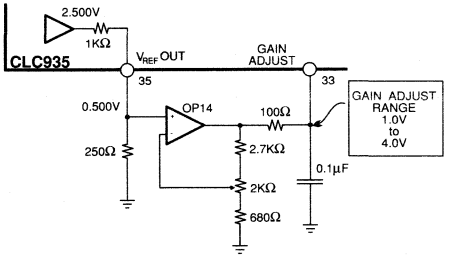
Analog Input Buffering

Gain Adjust

The CLC935 input range can be adjusted ±10% from its nominal ±1V range. The input range is controlled by adjusting the gain of the internal input buffer. This gain is controlled by the applied voltage at the GAIN ADJUST (pin33). The relationship between applied voltage at pin 33 and the analog input range is:

$$\text{analog input range} = \pm [2V + (0.129)(V_{\text{GAIN ADJUST}} - 2.5V)]$$

GAIN ADJUST pin(33) Voltage	Analog Input Range
1.0V	$1.8V_{PP}$
2.5V or open	$2.0V_{PP}$
4.0V	$2.2V_{PP}$

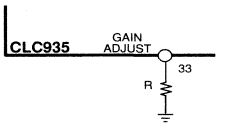


Analog Input Range Adjust Circuit

A resistor from GAIN ADJUST to ground provides a second method of adjusting the analog input range. This technique will decrease the converter's gain and increase the analog input range.

$$R = \frac{774 - 4,800\Delta}{\Delta}$$

Where Δ is the gain change factor,i.e 0.01 equals 1% change.



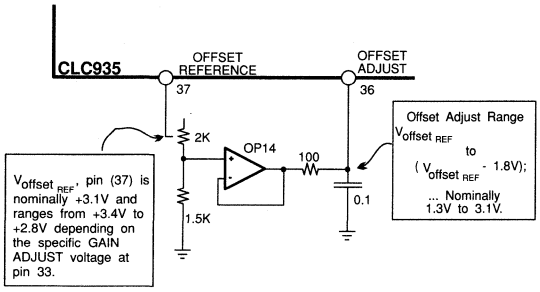
Alternate Input Range Adjust Circuit

Offset Adjust

Typically the center of the ±1V analog input range is laser trimmed to 0V during construction. By applying a voltage at the OFFSET ADJUST (pin 36), the analog input offset can be adjusted approximately ±100mV around ground. The applied voltage at pin 36 can range from GROUND to $V_{\text{OFFSET REFERENCE}}$. If the OFFSET REFERENCE (pin 37) voltage is used to generate the applied OFFSET ADJUST voltage, adjustments in the analog input range *offset* will track any adjustments made to the analog input range *gain*. Analog input range gain and offset adjustments are tightly coupled when the OFFSET REFERENCE is used to generate the OFFSET ADJUST applied voltage. Self-calibration techniques for adjusting offset and gain should use OFFSET REFERENCE in adjusting the offset.

Analog input offset and gain adjustments can be made independent of each other if the V_{REF} OUT (pin 35) is used to generate the applied OFFSET ADJUST voltage instead of the OFFSET REFERENCE voltage. If the V_{REF} OUT approach is adopted, the CLC935 offset and gain will be independent of each other, but will likely need an iterative adjustment approach where both offset and gain are successively adjusted until the desired result is obtained.

Offset Adjust Range pin (36)	Analog Input Offset
$V_{OFFSET\ REFERENCE}$	+100mV
open	0mV
GROUND	-100mV



Offset Adjust Circuit

The OFFSET ADJUST and GAIN ADJUST pins are very sensitive to noise; and should be bypassed to ground with 0.1µF ceramic capacitors. If the OFFSET ADJUST and GAIN ADJUST pins are not used, then they should be left floating.

CONVERT Clock Generation

All high-speed high-resolution A/D converters are sensitive to the CONVERT clock quality. With a full scale 7MHz analog input signal, the slew rate at the 0V crossing is 90LSB/ns. An error (jitter) of as little as 5ps in the clock edge will yield a 0.5LSB error at the A/D output. This is as great or greater than any other error source likely to be present. This type of clock error or clock jitter is most easily seen in the form of poor SNR (signal-to-noise ratio). If the SNR is below expectations, clock jitter should be investigated.

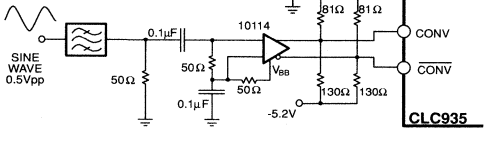
$$SNR_{MAX} = 20Log\left[\frac{1}{2\pi f_{in}\, jitter_{RMS}}\right]$$

where ...

$$jitter_{RMS} = \sqrt{(\text{clock } jitter_{RMS})^2 + (\text{analog } jitter_{RMS})^2}$$

It should also be noted that jitter in the analog input source will have the same detrimental effect on SNR. Analog input signal jitter is usually only a problem in evaluation setups, and does not generally present a problem in full systems.

Low-jitter crystal controlled oscillators make the best CONVERT clock sources. If the CONVERT clock is generated from another type of source, by gating, dividing or other method, it should be registered by the original clock as the last step. This should keep jitter terms from compounding.



Sine to ECL Conversion Circuit

For variable frequency CONVERT clocks, low-phase-noise frequency synthesizers like the Fluke 6080A or the HP8662 are good choices. Sinusoidal sources of this type will require a sine-to-ECL conversion circuit, such as the one above. This circuit operates consistently with low level inputs (0dBm), but is sensitive to noise (jitter) from the synthesizer. By maintaining a larger input level (>+6dBm), the 10114 jitter contribution can be greatly minimized.

Output Coding

The CLC935 is capable of producing four possible digital output formats: offset binary, two's complement, and their inverted versions. In offset binary the outputs count from 000h to FFFh, as the input varies from -FS (full-scale) to +FS. For two's complement output coding, the MSB in the offset binary format is inverted. On the CLC935, this is achieved by using the D1 (MSB) (pin 6) output rather than the D1(MSB) (pin 7). When using inverted coding formats, the data outputs D2 - D12(LSB) are inverted by tying DATA INV (pin 25) to an ECL logic HIGH (or grounding). For non-inverted operation DATA INV should be left floating, or tied to an ECL logic LOW.

Analog Input	Offset Binary	Two's Complement
+FS - 1 LSB	1111 1111 1111	0111 1111 1111
+FS - 2 LSBs	1111 1111 1110	0111 1111 1110
+FS - 3 LSBs	1111 1111 1101	0111 1111 1101
-	-	-
-	-	-
mid-scale + ½ LSB	1000 0000 0000	0000 0000 0000
mid-scale - ½ LSB	0111 1111 1111	1111 1111 1111
-	-	-
-	-	-
-FS + 2 LSBs	0000 0000 0010	1000 0000 0010
-FS + 1 LSB	0000 0000 0001	1000 0000 0001
-FS	0000 0000 0000	1000 0000 0000

Output Data and "Data Ready"

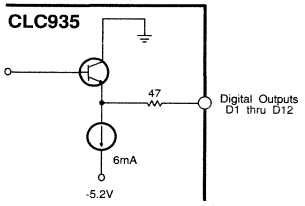
The CLC935 has one internal pipeline delay. This means that a sample taken on the rising edge of CONVERT (t_N) will appear at the output on the t_{N+1} clock cycle. The internally latched data from the previous conversion (t_{N-1}) is latched to the digital outputs on the rising edge of CONVERT. The previous output data is guaranteed to be valid for at least t_{HLD} after the rising edge of CONVERT and the new output data will be stable t_{DV} after the rising edge of CONVERT (see timing diagram).

Since the CLC935 has a synchronous interface, it does not require a separate Data Ready signal. The falling edge of the CONVERT should be used to generate the output latch clock signal, or Data Ready signal, as required by the system. This will limit the bulk of the digital switching noise to a period well away from the sensitive analog processing inside the converter. The use of the rising edge of CONVERT for Data Ready, and buffer clocking signals, is not recommended. Separate drivers for CONVERT and output latch strobing should be used to minimize corruption and jitter in the CONVERT signal.

Digital Interface and Termination Differences

All high-resolution A/D converters are susceptible to performance degradation if interference from the digital outputs is allowed to couple back to the analog input. Capacitive coupling back to the A/D input can result in increased harmonic distortion, or an elevated noise floor. This "noise" tends to be highly correlated to the input signal, and is difficult to remove through standard DSP noise reduction techniques. To minimize this effect, the CLC935 employs ECL "compatible" outputs rather than larger swing TTL compatible outputs. Additional measures to reduce output-to-input coupling have resulted in some slight differences when interfacing to the CLC935 as compared with true ECL.

The most significant difference is that the CLC935 **does not** require standard ECL output terminations. Most ECL circuits require a 50Ω terminating resistor from each output to a -2.0V bias supply (this can be implemented with a Thevenin equivalent resistor network between ground and the -5.2V supply). These terminations, when coupled with very low ECL output impedance, allow transmission lines to be driven at very high speeds. Unfortunately, typical ECL output terminations tend to dissipate an appreciable amount of dc power while also creating significant ground currents during switching. A typical Thevenin equivalent termination consumes an average current of 25mA. This yields 130mW per termination, which when multiplied by the 12 bits results in more than 1.5W being devoted to the terminations alone.

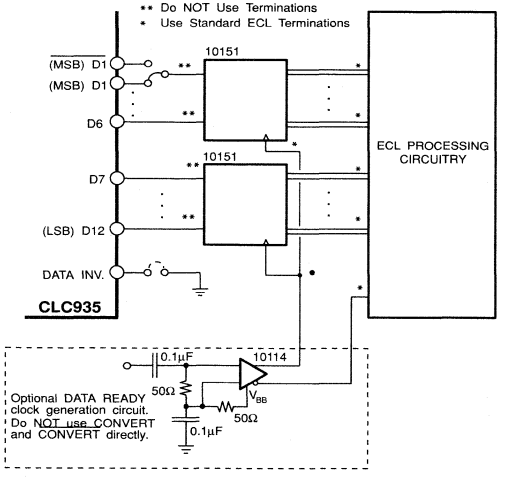


CLC935 Internal ECL Termination Circuit

The CLC935 outputs are 10KH ECL logic compatible with internal constant-current pull-downs, and are designed to be connected directly to 10KH level inputs with no external termination. The power dissipation in each termination is the 6mA standing current, multiplied by the 5.2V supply, or 31mW per output. For a 12-bit converter, this represents 375mW. When compared to external Thevinen terminations, the power savings is 1.2W.

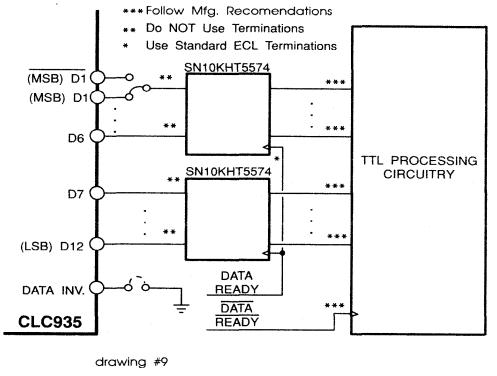
Output Latching and Level Translation

Parasitic capacitances and inductances should be minimized, when interfacing to the 935 outputs. Output latches (10176) or buffers should be placed as close as practical to the output pins. If these output latches drive a significant trace load on the same board as the converter, differential output latches (10E151) and trace routing should be used.



Recommended Output Buffering Circuits

In many systems, DSP and other forms of processing will employ TTL or CMOS circuitry. The output logic levels of the CLC935 will need to be translated to match those of the processing circuitry. Several options and translators exist to perform this task. Special care must be used if "10125" type circuits are used since these devices are not particularly suited to a high-resolution, low-noise, analog environment. Other options include the 105574 .



ECL to TTL/CMOS Level Translator Options

Power supplies, Grounding, and Bypassing

To obtain the best possible performance from any high-speed device, the design engineer must pay close attention to power supplies, grounding and bypassing. This applies not only to the A/D converter itself but throughout the system as well.

The recommended supply decoupling scheme is as follows: One 0.01µF to 0.033µF chip capacitor at every supply pin, with a +6.8µF to +10µF tantalum for each of the four main supplies feeds (within a few inches of the ADC). Note that supply feeds with excessive digital switching noise may require separate filtering using ferrite beads, additional capacitance, or split supplies. Proper bypassing of all other integrated circuits, especially logic circuits, should minimize power supply and ground transients.

All of the CLC935 grounds are internally connected. A single low-impedance ground plane is recommended for the CLC935. Split analog and digital grounds are not recommended for the CLC935. The SIGNAL GND is used internally for the track-and-hold and buffering amplifiers, while the other GROUND pins are essentially power supply returns.

The SIGNAL GND pins (pins 39 & 40) are very sensitive nodes, and should have a solid, low-impedance, ground connection. The path that the input signal and its return currents follow must be isolated from other circuitry. Single-point grounding at the converter should minimize common impedance paths which would allow other signals to directly couple into the analog input, affecting accuracy.

Thermal Considerations

The CLC935 dissipates approximately 5.2W. The following strategies can be applied to minimize junction temperatures:

a) A thick copper ground plane ... an appreciable amount of heat is conducted out of the A/D through its leads.
b) A copper or aluminum stand-off between the ground plane and the bottom of the CLC935 package (thermal paste may be useful).
c) A SIL PAD® between the ground plane and the bottom of the CLC935 package . To maximize heat conduction leave a patch of exposed (no solder mask) ground plane under the CLC935.
d) Moving air over the A/D converter.

Evaluation Board and Printed Circuit Board Layout

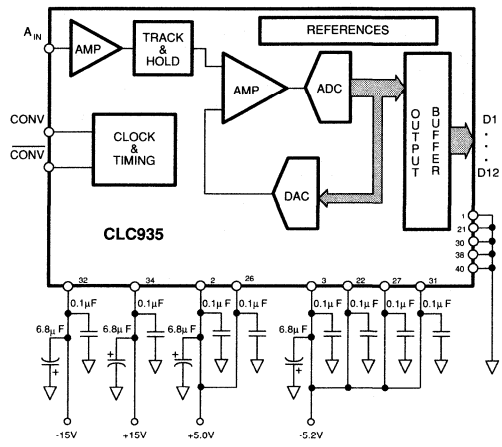
The keys to a successful CLC935 layout are a substantial low-impedance ground plane, short connections (in and out of the converter), and proper power supply decoupling. The use of a socket for the CLC935 is specifically not recommended in the final system design.

The CONVERT clock line traces should be equal length. If they are not equal, the edges may not arrive at the A/D at the same time, which may allow the clock signals to more easily couple into the analog input.

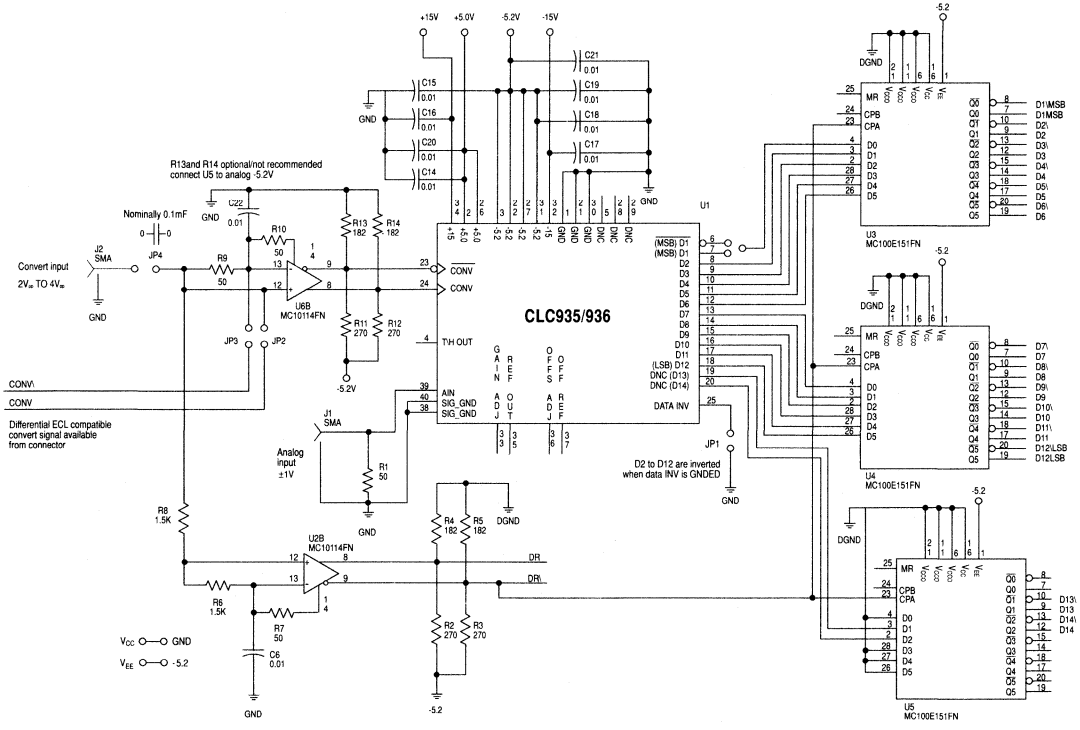
An evaluation board is available for the CLC935 (assembled - "E935PCASM", or bare board - "730025"). The evaluation board can be used to quickly evaluate the performance of the CLC935. Use of the evaluation board as a model is highly recommended.

Applications Support

Comlinear Corporation maintains a staff of applications engineers who are available for design and applications assistance. They can be reached at (303) 226 0500.



Recommended Power Supply Decoupling Scheme



Complete System Circuit

Comlinear Corporation

12-Bit, 20MSPS A/D Converter

CLC936

APPLICATIONS:

- radar processing
- infrared processing/ electronic imaging
- instrumentation
- medical imaging
- transient-signal recorders

FEATURES (typical):

- 71dB spurious free signal range; f_{IN}=4.97MHz
- no missing codes guaranteed
- 0.7LSB differential linearity
- small package (2.28in^2)

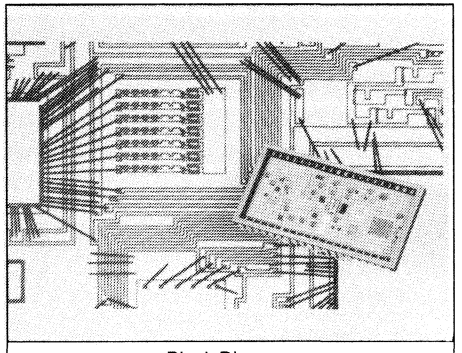
DESCRIPTION:

The CLC936 is a 12-bit analog-to-digital converter hybrid, including voltage references, track-and-hold, and 12-bit quantizer with ECL compatible outputs. The CLC936 has been especially optimized for a Spurious-Free-Signal-Range of better than 70dB. The CLC936 is constructed using advanced thin-film hybrid technology in a fully certified MIL-STD-1772 facility.

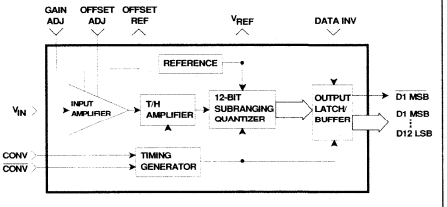
Comprehensive dynamic testing on every part ensures that system performance goals will be met, including spurious-free-signal-range (SFSR) of 73dB@407kHz and 65dB@9.68MHz. This, coupled with an SNR specification of 64dB@9.68MHz, means that the CLC936 is ideally suited for use in areas such as radar and instrumentation signal processing.

The CLC936 incorporates a complete two-pass subranging architecture, constructed from several high-speed building blocks. A broadband (135MHz) input amplifier buffers input signals and provides an accurate drive signal to the on-board track-and-hold. Laser trimmed gain and offset circuits assure accurate matching unit to unit. The latched outputs of the CLC936 mean that only a convert clock, analog input, and power supplies are required for operation; internal logic generates all required timing signals.

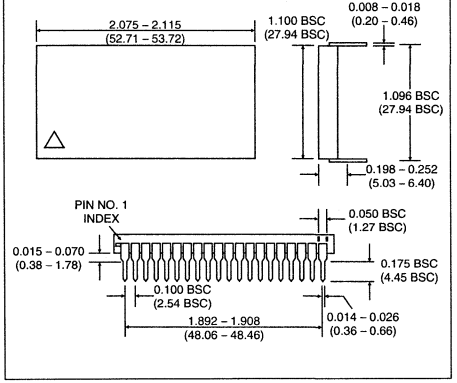
The CLC936AC is specified over a temperature range of 0°C to +70°C, while the CLC936A8C is specified over a range of -55°C to +125°C. Both devices are packaged in 40-pin, 1.1in wide, ceramic DIPs (note: leads are side brazed for easy access and inspection). Contact factory for availability of "gull-wing" surface-mount versions.



Block Diagram



Package Dimensions



Ordering Information		
CLC936AC	0°C to +70°C	industrial version
CLC936A8C	-55°C to +125°C	MIL-STD-883, class B

Both versions of the CLC936 are manufactured in Comlinear's MIL-STD-1772 certified facility in Fort Collins, Colorado, U.S.A.

Comlinear Corporation * **4800 Wheaton Drive, Fort Collins, CO 80525** * **(303) 226-0500** * **FAX (303) 226-0564**

DS936.00

January 1993

Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_2$ = -15.0V; $-V_{EE}$ = -5.2V; unless specified)

PARAMETER[1]	CONDITIONS	TYP	MAX & MIN RATINGS						UNITS	SYMBOL
			CLC936AC			CLC936A8C				
Case Temperature		+25°C	0°C	+25°C	+70°C	-55°C	+25°C	+125°C		
DYNAMIC CHARACTERISTICS										
small signal bandwidth	V_{IN} = 1/4 FS	135	95	100	100				MHz	SSBW
large signal bandwidth	V_{IN} = FS	125	75	75	75				MHz	LSBW
slew rate		450	300	300	300				V/µs	SR
overvoltage recovery time	V_{IN} = 2FS	14	25	25	25				ns	OR
effective aperture delay		-0.4	-1.5	-2.0	-2.0				ns	TA
aperture jitter		1.25	2.5	2.0	2.0				ps(RMS)	AJ
NOISE and DISTORTION (20MSPS)										
* signal-to-noise ratio										
(not including harmonics)	407kHz; FS	65.6	61.0	63.0	63.0				dB	SNR1
	4.978MHz; FS	64.3	60.0	62.0	62.0				dB	SNR2
	9.685MHz; FS	64.0	60.0	60.0	60.0				dB	SNR3
* in-band harmonics										
	407kHz; FS-1dB	-73.2	-66.0	-66.0	-66.0				dBc	IBH1
	4.978MHz; FS-1dB	-71.0	-65.0	-65.0	-62.0				dBc	IBH2
	9.685MHz; FS-1dB	-65.0	-60.0	-60.0	-60.0				dBc	IBH3
* spurious-free-signal-range										
	407kHz; FS-1dB	73.2	66.0	66.0	66.0				dB	SFSR1
	4.978MHz; FS-1dB	71.0	65.0	65.0	62.0				dB	SFSR2
	9.685MHz; FS-1dB	65.0	60.0	60.0	60.0				dB	SFSR3
intermodulation distortion (f_1=4.95MHz@FS-6.5dB; f_2=5.05MHz@FS-6.5dB)		75							dBc	IMD
noise-power-ratio (dc to xxMHz white noise; xxMHz slot)	FS-12dB								dB	NPR
DC ACCURACY and PERFORMANCE										
differential non-linearity	dc; FS	0.7	1.0	1.0	1.0				LSB	DNL
integral non-linearity	dc; FS	1.3	2.0	2.0	2.0				LSB	INL
missing codes		0	0	0	0				codes	MC
bipolar offset error		3.0	12	10	15				mV	VIO
temperature coefficient			300		250				µV/°C	DVIO
bipolar gain error		1.2	2.2	2.0	2.2				%FS	GE
temperature coefficient			0.07		0.05				%FS/°C	DVIO
ANALOG INPUT PERFORMANCE										
analog input bias current		10	45	25	35				µA	IBN
temperature coefficient		100	250		100				nA/°C	DIBN
analog input resistance		80	50	50					kΩ	RIN
analog input capacitance		3.5	5.5	5.5	5.5				pF	CIN
POWER REQUIREMENTS										
* supply current ($+V_{CC}$ = +5.0V)	20MSPS; no load	127	160	160	160				mA	ICC
* supply current ($-V_{EE}$ = -5.2V)[4]	20MSPS; no load	770	960	960	960				mA	IEE
* supply current ($+V_1$ = +15.0V)	20MSPS; no load	12	20	20	20				mA	I1
* supply current ($-V_2$ = -15.0V)	20MSPS; no load	38	50	50	50				mA	I2
nominal power dissipation[4]	20MSPS; no load	5.4							W	PD

Note 1: Parameters preceded by an * are 100% tested. AC units are tested at 25°C and guaranteed at 0°C and 70°C.

Note 2: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Note 3: Junction temperature rise above case = 16°C; θ_{CA}=16°C/W; θ_{CA}=7°C/W@500LFPM. Use of a SIL-PAD® #550007, from Berquist (1-800-347-4572), can lower case-to-ambient rise; θ_{CA} = 12°C/W@still air, 12in² ground-plane; θ_{CA}=3.4°C/W@100LFPM, 12in² ground-plane.

Note 4: Planned product improvements are expected to lower -5.2V supply current, as well as nominal power dissipation.

Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_2$ = -15.0V; $-V_{EE}$ = -5.2V; unless specified)

PARAMETER[1]	CONDITIONS	TYP	MAX & MIN RATINGS						UNITS	SYMBOL
			CLC936AC			CLC936A8C				
Case Temperature		+25°C	0°C	+25°C	+70°C	-55°C	+25°C	+125°C		
DIGITAL INPUTS										
input voltage	logic LOW		-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	V	VIL
	logic HIGH		-1.1	-1.1	-1.1	-1.1	-1.1	-1.1	V	VIH
input current	logic LOW		1.0	1.0	1.0	1.0	1.0	1.0	mA	IIL
	logic HIGH		1.0	1.0	1.0	1.0	1.0	1.0	mA	IIH
DIGITAL OUTPUTS										
output voltage	logic LOW		-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	V	VOL
	logic HIGH		-1.1	-1.1	-1.1	-1.1	-1.1	-1.1	V	VOH
TIMING										
maximum conversion rate			20	20	20	20	20	20	MSPS	CR
minimum conversion rate		0	0	0	0	0	0	0	MSPS	CRM
data hold time		6	3	4	3	3	4	3	ns	THLD
output propagation delay		10	15	15	15	15	15	15	ns	TDV

Recommended Operating Conditions

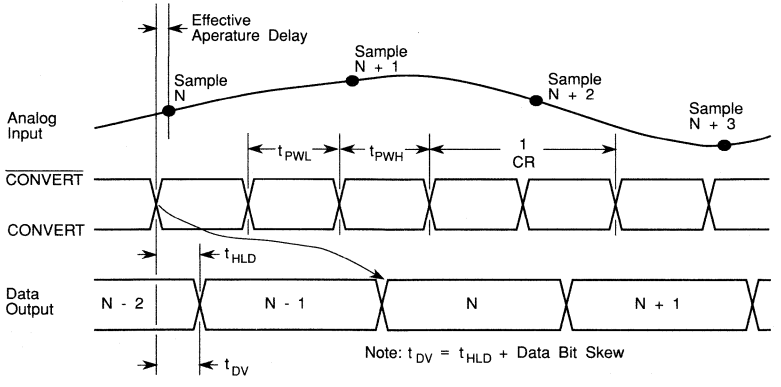
positive supply voltage ($+V_{CC}$)	+5V
positive supply voltage ($+V_1$)	+15V
negative supply voltage ($-V_{EE}$)	-5.2V
negative supply voltage ($-V_1$)	-15V
differential voltage between any two GND's	<10mV
analog input voltage range (Full Scale)	±1V
digital output current sinking	6mA(max)
sourcing	6mA(max)
digital input voltage range	-2.0V to 0.0V

Absolute Maximum Ratings[2]

positive supply voltage ($+V_{CC}$)	-0.5 to +7.0V
positive supply voltage ($+V_1$)	-0.5 to +18V
negative supply voltage ($-V_{EE}$)	+0.5 to -7.0V
negative supply voltage ($-V_1$)	+0.5 to -18.0V
differential voltage between any two GND's	200mV
analog input voltage range	$-V_{EE}$ to $+V_{CC}$
DIGITAL input voltage range	+0.5V to $-V_{EE}$
gain and offset adjust voltage range	$-V_{EE}$ to $+V_{CC}$
output short circuit duration (one pin to ground)	Infinite
Junction Temperature	+175°C
Operating Temperature Range[3]	
CLC936AC	0°C to +70°C
CLC936A8C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Solder Duration (+300°C)	10 sec

10

Timing Diagram



Understanding A/D Dynamic Specifications

Analog-to-Digital converters are specified in many ways. As a component achieves higher performance, its specifications and their definitions can become more critical. Fortunately, the vast number of converter applications can generally be placed into one of two classes. These are processed data and non-processed data applications. The distinction seems quite simple but the split implies a completely different approach in specifying A/D converters for a given application.

The processed data area includes the frequency domain applications which employ Fourier processing (FFT). Also in this category are the highly averaged applications, usually concerned with low noise. In each case, the converter's data is averaged or convolved mathematically. This processing reduces the apparent noise level in the output data. For FFTs, the noise is simply spread over a large number of frequency bins. For simple averaging approaches, the gaussian distribution of noise is greatly reduced, appearing to increase the converter's resolution. Processed applications include radar, network and spectrum analyzers, communications receivers, etc.

The non-processed applications tend to take the converter's data in its original form with very little processing. This means that the noise reduction benefits of the processed applications are not seen. The non-processed area is composed primarily of time domain applications like imaging, DSO's, ultrasound, etc.

The processed vs. non-processed issue has several implications in terms of converter specifications. For the non-processed (time domain) systems the dominant converter specifications deal with noise (SNR) and converter accuracy (DNL). The converter's quantization noise and input stage noise dominate converter accuracy . The harmonic distortion (primarily INL) of the converter is generally of little interest given that most time domain applications present data for visual analysis and tend to focus on "local" accuracy rather than over the full input range. "Local" accuracy is best described through the standard noise measurements, such as SNR and DNL.

In the frequency domain application areas, the noise of the converter is processed to the point where, for almost all systems, it is no longer of issue. This is manifested as a reduction in the apparent noise floor. The actual RMS noise is not reduced, but is spread over more and more frequency bins as processing levels are increased. Unfortunately, the harmonic distortion performance of the converter is not affected by increased processing. This makes the harmonic performance, or more specifically the spurious performance, the dominant error source for frequency domain applications. SFSR becomes the dominant specification for determining converter performance in the frequency domain.

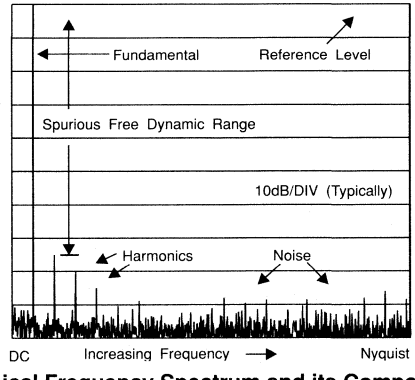
Signal-to-Noise Ratio (SNR) is the ratio of the power contained in the fundamental signal compared to the power contained in the entire noise floor. That is to say all individual noise components are added together to arrive at an integrated noise power. For SNR, harmonic power is excluded from the noise measurement. SNR is particularly important in time domain applications like digital image processing and infrared imaging, where conversion accuracy can be heavily degraded by integrated noise.

Signal-to-Noise-and-Distortion (SINAD) is the ratio of the fundamental signal power to the power at all other frequencies. This includes all noise as well as all harmonics. SINAD is a worst case specification for A/D converters, combining variables from both frequency and time domains. The value of SINAD in high-performance converter applications is not clear since it does not accurately predict the best converter for a given application. Because applications tend to fall into time domain/non-processed or frequency domain/processed applications, those specifications more directly related to the application should be the primary focus in selecting the converter.

Total Harmonic Distortion (THD) is the combined power of a specified number of harmonics, compared to the power of the fundamental signal. Harmonics are located at predictable frequencies, spaced at integer multiples of the fundamental signal. For example, a 1MHz fundamental would generate harmonics at 2MHz, 3MHz, 4MHz, ... and so on. In practice, only the first five harmonics contribute significantly to THD, although more may be included in the measurement. THD does not tend to apply well in frequency domain applications which are by their nature very SFSR oriented. In time domain applications, THD is indicative of full-scale input range distortion, however the high-performance time domain applications are generally most interested in local distortion performance. Local distortion and accuracy is dominated by DNL. The use of THD for applications requiring local performance is not likely to yield accurate or repeatable results in selecting the correct converter.

Spurious-Free-Signal-Range (SFSR) is the "clean" dynamic range of the converter, free from harmonic and spurious signals. SFSR is ratio of the power of the fundamental compared to the power of the next largest component in the frequency spectrum. The SFSR specification is especially important to frequency domain applications which perform Fourier transforms to analyze the converter's output data. Processed applications like radar and network analyzers are typical areas where SFSR offers a direct prediction of converter's performance at both the system and component levels. SFSR is the single best specification for selecting a converter to be used in a frequency domain application.

In-Band Harmonics (IBH) is the ratio of the power of the fundamental compared to the power of the single largest harmonic. This specification is very similar to SFSR, but since it only considers a fairly limited number of harmonics, it is potentially an incomplete gauge of converter performance. SFSR is more stringent and should be used whenever possible in lieu of IBH.



Typical Frequency Spectrum and its Components

Discussion of CLC936 Plots and Specifications

Some of the performance plots that follow require more explanation than is feasible in the caption. This section goes into more detail as to how these plots were generated, and how they might be interpreted. Additional information can be found in the application note AD-01 ... Designing with High-Performance A/D converters"

Spectral Plots
The output frequency spectrum is shown for input frequencies of 404KHz, 1.85MHz, 4.978MHz and 9.685MHz. All of these plots were generated with a 20MSPS Clock. Four thousand point (4K) FFT's were taken, using a Blackmann-Harris window and the power spectra were averaged over 10 cycles to accentuate the harmonics and reduce variance in the noise level. The plots show the frequency spectrum from dc to the 10MHz Nyquist frequency for 20MSPS.

SFSR and SNR vs Input level Plots
As the signal level is reduced from full scale, the noise level remains relatively constant. This results in a backward declining straight line shown as SNR vs Input Amplitude. In some converters the 'noise' is not independent of the input signal level and hence the line may not be straight. The 74dB theoretical limit on SNR is shown with the -1dB/dB backward declining slope for reference. The CLC936 noise performance parallels this reference, and indicates that noise performance is relatively uniform for all analog input levels.

The SFSR performance is somewhat less uniform. As the ratio of the largest non-fundamental frequency component relative to the fundamental, it is more susceptible to random variations in the spectrum. The input power was measured at the A/D converter. For each amplitude a 4K point FFT was taken and analyzed to determine the SNR and SFSR. The vertical scale is measured in dBc, this is dB relative to the test signal, and the horizontal scale is dB-FS which is dB relative to the converter's full-scale analog input range.

Two Tone Linearity Spectrum
In a linear system, the input signal can be viewed mathematically as a superposition of sinusoids (Fourier Transform). The system output can be predicted by the superpositioning of the individual effects on each of the sinusoid inputs. For example, if a linear network is presented with a single tone signal F_1 and the result is an attenuation by a factor A_1, and it is then presented with another frequency F_2 attenuated by A_2 through the system, then the expected output for an input of F_1+F_2 would be $A_1F_1 + A_2F_2$.

If the network is not linear, the output will contain frequency components in addition to those present at the input. The most common frequencies likely to be present in the output are at $MF_1 \pm NF_2$, where M and N are integers, and F_1 and F_2 are the two input frequencies. In the *two-tone linearity* plot, the input to the CLC936 consists of 4.95MHz and 5.05MHz superpositioned sinusoids. Intermodulation terms on the order of -80dBc confirm the CLC936's excellent linearity.

SNR, and SFSR vs Input Frequency
These plots shows the variation in converter performance relative to analog input frequency. Input frequencies to about 65MHz (the Full-Power-Bandwidth) are included, and should be useful for over-sampling applications. Beyond the full-power-bandwidth, performance for large signals degrades quickly. The small-signal-bandwidth (measured with analog inputs below $200mV_{PP}$) performance does not degrade until around 135MHz.

SFSR vs Conversion Rate
There are several critical timing processes inside the converter, including the track time, the time allowed for settling of internal nodes, and time to perform the coarse and fine quantizations. When a rising edge of CONVERT is detected, a pre-timed sequence of events is set into motion. Accordingly the performance of the CLC936 is very independent of clock rate, up to the specified speed of 20MSPS, after which performance can degrade rapidly.

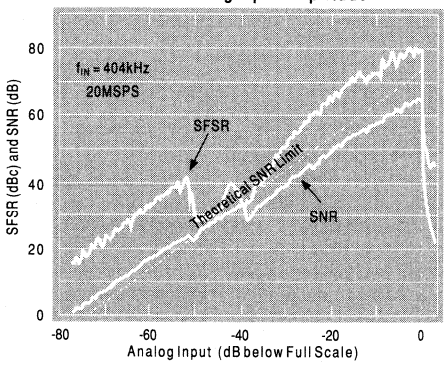
Digital output skew plot
The digital outputs make their transition T_{DV}ns after the rising edge of the CONVERT signal. The actual time to this transition varies slightly from output bit to output bit. The amount of this variation is small , and well within the timing needs for this type of system. In the *Bit Skew* plot, all 12 output bits are shown for various transitions. As can be seen, the total variation, bit-to-bit, is about 2ns.

Pulse response plots
This plot has been generated with a $1V_{PP}$ flat top pulse input signal with a 600ps rise time and a 20.000549MHz repetition rate. The input signal is effectively aliased to 549Hz when sampled at 20MSPS.

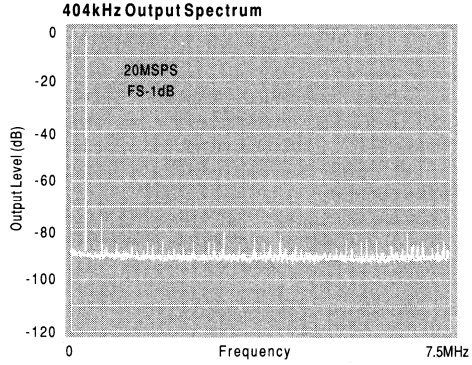
A sequence of 4096 samples will now represent an equivalent time window of 10ns. Any slew rate limitations, ringing or other non-idealities in the A/D analog input stage will now be apparent in the aliased output signal. As can be seen from the plots, the only non-ideality is a bandwidth limitation, which limits the time to an accurate sample to about 7ns. If your input signal is a step function, such as a CCD output or T/H output, this means that the sample should be taken at least 7ns after the start of the transition.

Typical Performance Characteristics (T_A = +35°C, 20MSPS unless specified)

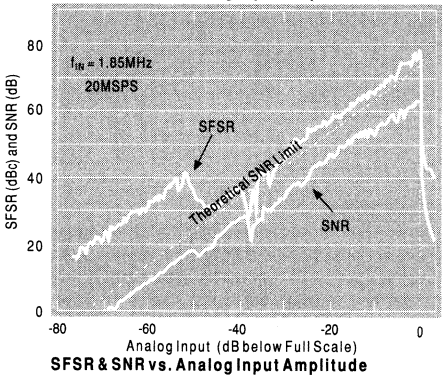
SFSR & SNR vs. Analog Input Amplitude



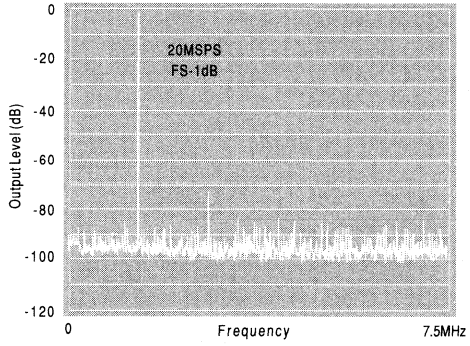
404kHz Output Spectrum



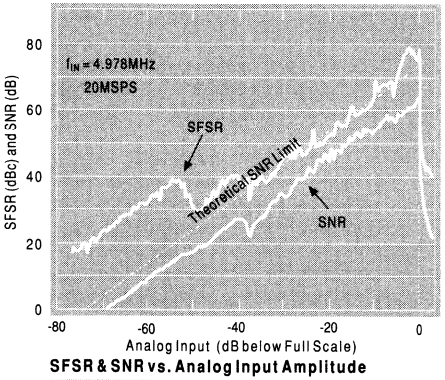
SFSR & SNR vs. Analog Input Amplitude



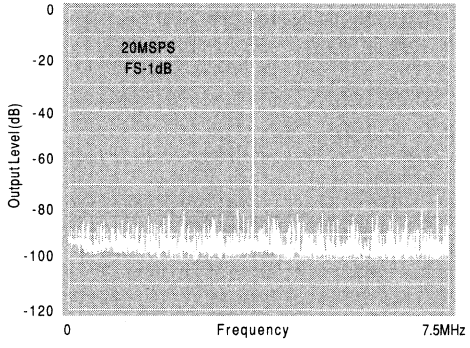
1.85MHz Output Spectrum



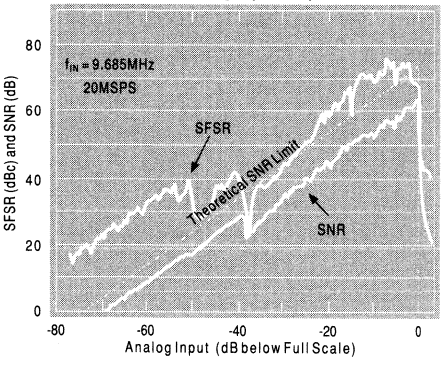
SFSR & SNR vs. Analog Input Amplitude



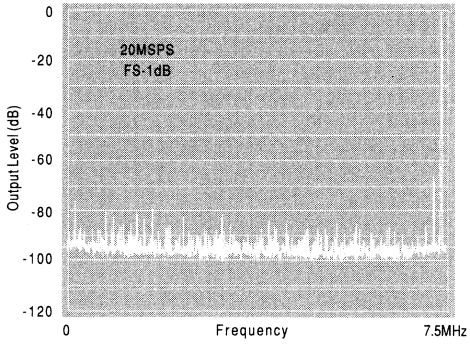
4.978MHz Output Spectrum



SFSR & SNR vs. Analog Input Amplitude

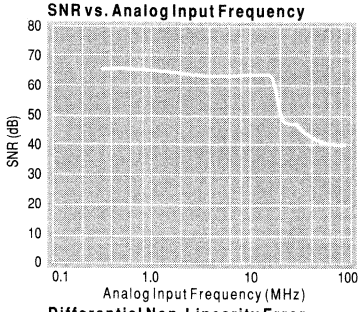


9.685MHz Output Spectrum

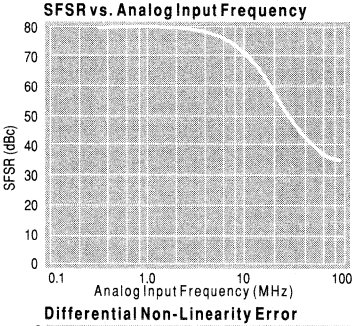


Typical Performance Characteristics (T_A = +35°C, 20MSPS unless specified)

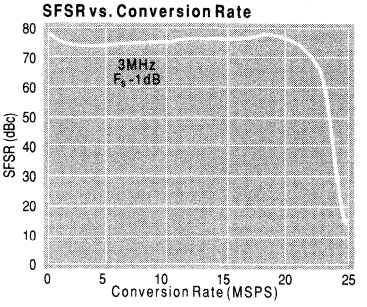
SNR vs. Analog Input Frequency



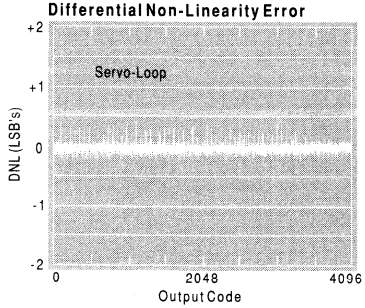
SFSR vs. Analog Input Frequency



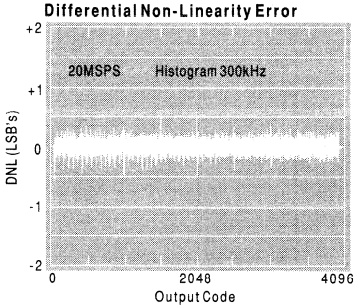
SFSR vs. Conversion Rate



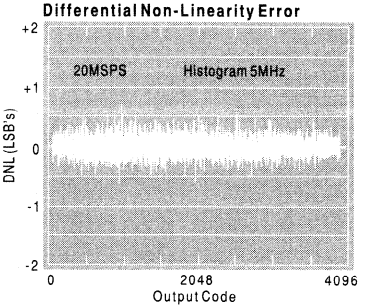
Differential Non-Linearity Error



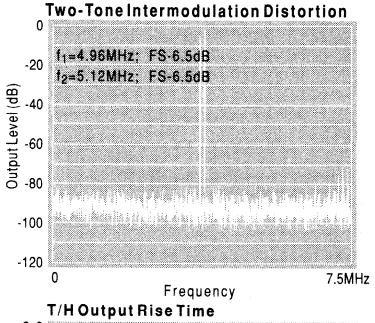
Differential Non-Linearity Error



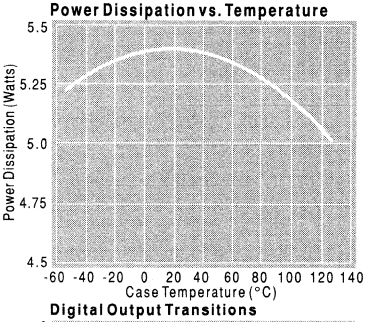
Differential Non-Linearity Error



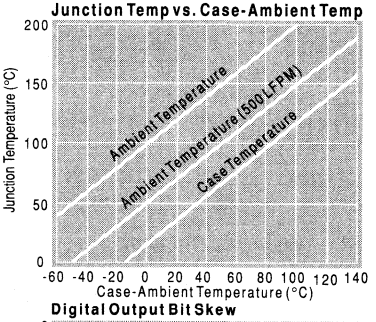
Two-Tone Intermodulation Distortion



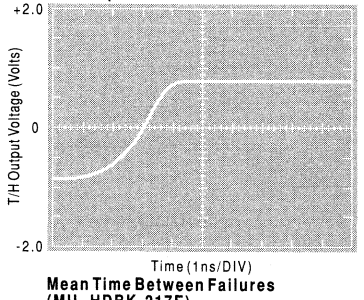
Power Dissipation vs. Temperature



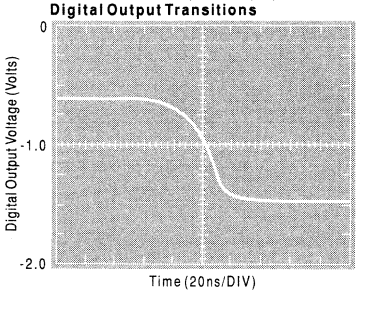
Junction Temp vs. Case-Ambient Temp



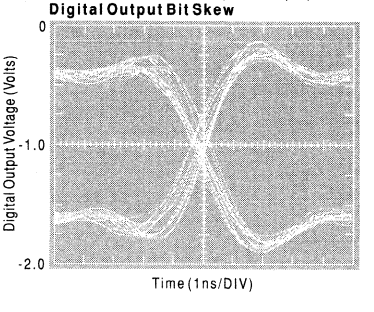
T/H Output Rise Time



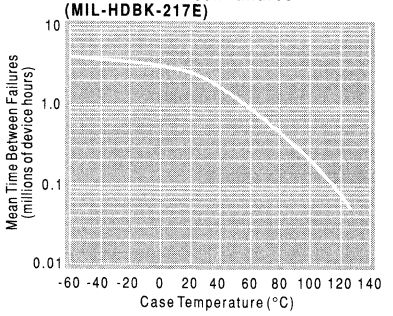
Digital Output Transitions



Digital Output Bit Skew



Mean Time Between Failures (MIL-HDBK-217E)



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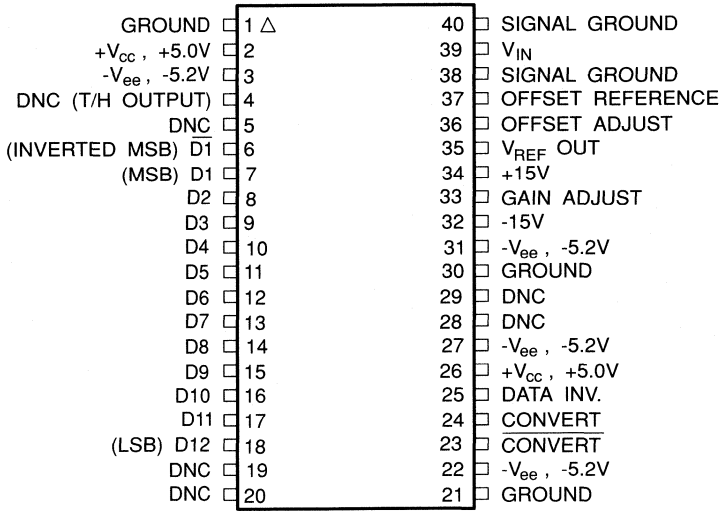
CLC936 Pinout



Pin Description and Usage

ECL-Level Digital Inputs

CONVERT, $\overline{\text{CONVERT}}$ — *Pins 23, 24*
"Differential Convert Command" initiates a new conversion cycle on the rising edge of CONVERT.

DATA INV — *Pin 25*
DATA INVERT is an active HIGH (grounded) ECL input which causes the data outputs [D2 to (LSB) D12] to be inverted. In normal operation, DATA INV is left floating or tied to ECL logic LOW.

ECL-Level Digital Outputs

(MSB) D1-D12 — *Pins 7 to 18*
Digital Data Outputs. D1 is the MSB; D12 is the LSB. In their normal state, the digital outputs offer Offset Binary output coding.

$\overline{\text{(MSB) D1}}$ — *Pin 6*
Inverted version of the MSB, used for 2's Complement coding.

Analog Input

V_{IN} — *Pin 39*
Analog input with a $2V_{PP}$ input range from +1V to -1V.

Gain Adjust — *Pin 33*
The GAIN ADJUST has a +4V to +1V input range and scales the analog input full-scale range by -10% to +10% respectively. If unused, Gain Adjust should be left floating.

Offset Adjust — *Pin 36*
The OFFSET ADJUST has a GROUND to OFFSET REFERENCE input range and scales the analog input offset by ±0.1V. If unused, Offset Adjust should be left floating.

Offset Reference — *Pin 37*
The OFFSET REFERENCE tracks gain adjustments and is used for offset voltage adjust.

Miscellaneous

V_{REF} — *Pin 35*
V_{REF} is a highly stable +2.500V voltage reference. (Recommended current drain ≤2mA.)

D.N.C — *Pins 5, 19, 20, 28, 29*
Do Not Connect.

DNC (T/H Output) — Pin 4
Internal Track-and-Hold output voltage test point. Do not Connect.

Power and Ground

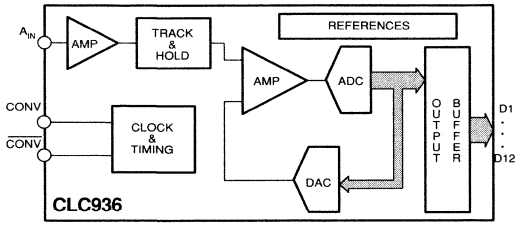
+5V, Pins 2,26; +15V, Pin 34; -5.2V, Pins 3, 22, 27, 31; -15V, Pin 32; GROUND, Pins 1, 21, 30, 38, 40.

Applications Information

In high-speed data acquisition systems, overall performance is usually determined by the A/D converter. Accordingly, special attention should be given to the converter, its operation, and its environment. To assist in this process, information on these critical items has been included in this data sheet. Additional information on using high-performance A/D converters can also be found in Comlinear Corporation application note AD-01.

Principle of Operation

The CLC936 is a complete two step, subranging A/D converter, with input buffering, internal track-and-hold, quantizer, and all necessary voltage references. The block diagram for the converter is shown below.

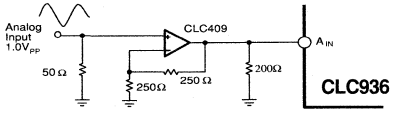


CLC936 Functional Block Diagram

The conversion cycle is initiated on the rising edge of the CONVERT signal. The analog input is sampled by the track-and-hold amplifier and is then digitized with an 8-bit digitizer. The 6 MSBs of this conversion are the "coarse-quantization", which drive a 14-bit accurate DAC to match the input level. The DAC output is then subtracted from the original analog input to generate an error signal, which is then digitized. The two digitized results are combined to form the 12-Bit accurate output. Error correction and output buffering are also provided by the CLC936.

Analog Input Driving Circuits

The high dynamic range of the CLC936 places high demands on any analog processing circuitry that precedes the converter. This is particularly true in the area of harmonic distortion where the CLC936's performance often exceeds -72dBc. Fortunately the CLC936 employs an internal buffer for the analog input, and external buffering circuits are usually not required. Both the CLC207 and the CLC409 amplifiers can be configured for better than -80dBc harmonic distortion (note that the CLC409 does not support 12-bit settling performance necessary for "time domain" applications). This makes them ideal choices for any analog signal conditioning or buffering that may be required.



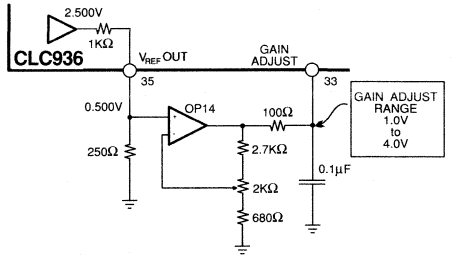
Analog Input Buffering

Gain Adjust

The CLC936 input range can be adjusted ±10% from its nominal ±1V range. The input range is controlled by adjusting the gain of the internal input buffer. This gain is controlled by the applied voltage at the GAIN ADJUST (pin33). The relationship between applied voltage at pin 33 and the analog input range is:

$$\text{analog input range} = \pm [2V + (0.129)(V_{\text{GAIN ADJUST}} - 2.5V)]$$

GAIN ADJUST pin(33) Voltage	Analog Input Range
1.0V	$1.8V_{PP}$
2.5V or open	$2.0V_{PP}$
4.0V	$2.2V_{PP}$

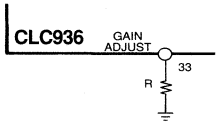


Analog Input Range Adjust Circuit

A resistor from GAIN ADJUST to ground provides a second method of adjusting the analog input range. This technique will decrease the converter's gain and increase the analog input range.

$$R = \frac{774 - 4{,}800\Delta}{\Delta}$$

Where Δ is the gain change factor,i.e 0.01 equals 1% change.



Alternate Input Range Adjust Circuit

Offset Adjust

Typically the center of the ±1V analog input range is laser trimmed to 0V during construction. By applying a voltage at the OFFSET ADJUST (pin 36), the analog input offset can be adjusted approximately ±100mV around ground. The applied voltage at pin 36 can range from GROUND to $V_{\text{OFFSET REFERENCE}}$. If the OFFSET REFERENCE (pin 37) voltage is used to generate the applied OFFSET ADJUST voltage, adjustments in the analog input range *offset* will track any adjustments made to the analog input range *gain*. Analog input range gain and offset adjustments are tightly coupled when the OFFSET REFERENCE is used to generate the OFFSET ADJUST applied voltage. Self-calibration techniques for adjusting offset and gain should use OFFSET REFERENCE in adjusting the offset.

Analog input offset and gain adjustments can be made independent of each other if the V_{REF} OUT (pin 35) is used to generate the applied OFFSET ADJUST voltage instead of the OFFSET REFERENCE voltage. If the V_{REF} OUT approach is adopted, the CLC936 offset and gain will be independent of each other, but will likely need an iterative adjustment approach where both offset and gain are successively adjusted until the desired result is obtained.

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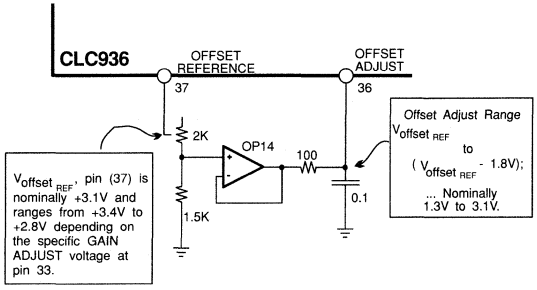
Offset Adjust Range pin (36)	Analog Input Offset
$V_{OFFSET\ REFERENCE}$	+100mV
open	0mV
GROUND	-100mV



Offset Adjust Circuit

The OFFSET ADJUST and GAIN ADJUST pins are very sensitive to noise; and should be bypassed to ground with 0.1µF ceramic capacitors. If the OFFSET ADJUST and GAIN ADJUST pins are not used, then they should be left floating.

CONVERT Clock Generation

All high-speed high-resolution A/D converters are sensitive to the CONVERT clock quality. With a full scale 7MHz analog input signal, the slew rate at the 0V crossing is 90LSB/ns. An error (jitter) of as little as 5ps in the clock edge will yield a 0.5LSB error at the A/D output. This is as great or greater than any other error source likely to be present. This type of clock error or clock jitter is most easily seen in the form of poor SNR (signal-to-noise ratio). If the SNR is below expectations, clock jitter should be investigated.

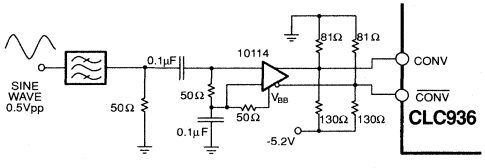
$$SNR_{MAX} = 20Log \left[\frac{1}{2\pi f_{in} jitter_{RMS}} \right]$$

where ...

$$jitter_{RMS} = \sqrt{(\text{clock } jitter_{RMS})^2 + (\text{analog } jitter_{RMS})^2}$$

It should also be noted that jitter in the analog input source will have the same detrimental effect on SNR. Analog input signal jitter is usually only a problem in evaluation setups, and does not generally present a problem in full systems.

Low-jitter crystal controlled oscillators make the best CONVERT clock sources. If the CONVERT clock is generated from another type of source, by gating, dividing or other method, it should be registered by the original clock as the last step. This should keep jitter terms from compounding.



Sine to ECL Conversion Circuit

For variable frequency CONVERT clocks, low-phase-noise frequency synthesizers like the Fluke 6080A or the HP8662 are good choices. Sinusoidal sources of this type will require a sine-to-ECL conversion circuit, such as the one above. This circuit operates consistently with low level inputs (0dBm), but is sensitive to noise (jitter) from the synthesizer. By maintaining a larger input level (>+6dBm), the 10114 jitter contribution can be greatly minimized.

Output Coding

The CLC936 is capable of producing four possible digital output formats: offset binary, two's complement, and their inverted versions. In offset binary the outputs count from 000h to FFFh, as the input varies from -FS (full-scale) to +FS. For two's complement output coding, the MSB in the offset binary format is inverted. On the CLC936, this is achieved by using the D1 (MSB) (pin 6) output rather than the D1(MSB) (pin 7). When using inverted coding formats, the data outputs D2 - D12(LSB) are inverted by tying DATA INV (pin 25) to an ECL logic HIGH (or grounding). For non-inverted operation DATA INV should be left floating, or tied to an ECL logic LOW.

Analog Input	Offset Binary	Two's Complement
+FS - 1 LSB	1111 1111 1111	0111 1111 1111
+FS - 2 LSBs	1111 1111 1110	0111 1111 1110
+FS - 3 LSBs	1111 1111 1101	0111 1111 1101
-	-	-
-	-	-
mid-scale + ½ LSB	1000 0000 0000	0000 0000 0000
mid-scale - ½ LSB	0111 1111 1111	1111 1111 1111
-	-	-
-	-	-
-FS + 2 LSBs	0000 0000 0010	1000 0000 0010
-FS + 1 LSB	0000 0000 0001	1000 0000 0001
-FS	0000 0000 0000	1000 0000 0000

Output Data and "Data Ready"

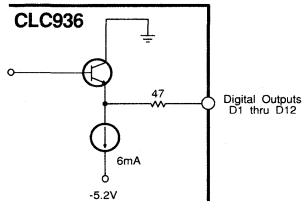
The CLC936 has one internal pipeline delay. This means that a sample taken on the rising edge of CONVERT (t_N) will appear at the output on the t_{N+1} clock cycle. The internally latched data from the previous conversion (t_{N-1}) is latched to the digital outputs on the rising edge of CONVERT. The previous output data is guaranteed to be valid for at least t_{HLD} after the rising edge of CONVERT and the new output data will be stable t_{DV} after the rising edge of CONVERT (see timing diagram).

Since the CLC936 has a synchronous interface, it does not require a separate Data Ready signal. The falling edge of the CONVERT should be used to generate the output latch clock signal, or Data Ready signal, as required by the system. This will limit the bulk of the digital switching noise to a period well away from the sensitive analog processing inside the converter. The use of the rising edge of CONVERT for Data Ready, and buffer clocking signals, is not recommended. Separate drivers for CONVERT and output latch strobing should be used to minimize corruption and jitter in the CONVERT signal.

Digital Interface and Termination Differences

All high-resolution A/D converters are susceptible to performance degradation if interference from the digital outputs is allowed to couple back to the analog input. Capacitive coupling back to the A/D input can result in increased harmonic distortion, or an elevated noise floor. This "noise" tends to be highly correlated to the input signal, and is difficult to remove through standard DSP noise reduction techniques. To minimize this effect, the CLC936 employs ECL "compatible" outputs rather than larger swing TTL compatible outputs. Additional measures to reduce output-to-input coupling have resulted in some slight differences when interfacing to the CLC936 as compared with true ECL.

The most significant difference is that the CLC936 **does not** require standard ECL output terminations. Most ECL circuits require a 50Ω terminating resistor from each output to a -2.0V bias supply (this can be implemented with a Thevenin equivalent resistor network between ground and the -5.2V supply). These terminations, when coupled with very low ECL output impedance, allow transmission lines to be driven at very high speeds. Unfortunately, typical ECL output terminations tend to dissipate an appreciable amount of dc power while also creating significant ground currents during switching. A typical Thevenin equivalent termination consumes an average current of 25mA. This yields 130mW per termination, which when multiplied by the 12 bits results in more than 1.5W being devoted to the terminations alone.

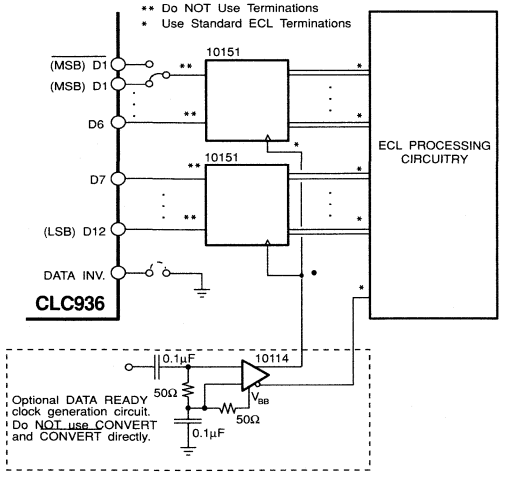


CLC936 Internal ECL Termination Circuit

The CLC936 outputs are 10KH ECL logic compatible with internal constant-current pull-downs, and are designed to be connected directly to 10KH level inputs with no external termination. The power dissipation in each termination is the 6mA standing current, multiplied by the 5.2V supply, or 31mW per output. For a 12-bit converter, this represents 375mW. When compared to external Thevinen terminations, the power savings is 1.2W.

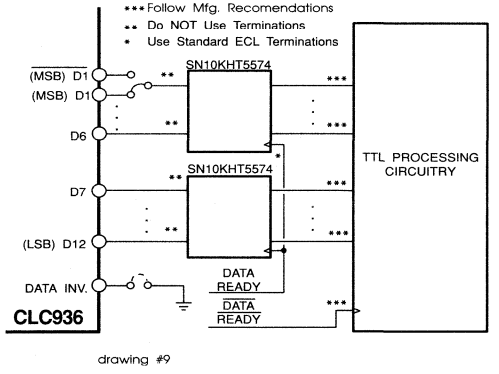
Output Latching and Level Translation

Parasitic capacitances and inductances should be minimized, when interfacing to the 936 outputs. Output latches (10176) or buffers should be placed as close as practical to the output pins. If these output latches drive a significant trace load on the same board as the converter, differential output latches (10E151) and trace routing should be used.



Recommended Output Buffering Circuits

In many systems, DSP and other forms of processing will employ TTL or CMOS circuitry. The output logic levels of the CLC936 will need to be translated to match those of the processing circuitry. Several options and translators exist to perform this task. Special care must be used if "10125" type circuits are used since these devices are not particularly suited to a high-resolution, low-noise, analog environment. Other options include the 105574 .



ECL to TTL/CMOS Level Translator Options

Power supplies, Grounding, and Bypassing

To obtain the best possible performance from any high-speed device, the design engineer must pay close attention to power supplies, grounding and bypassing. This applies not only to the A/D converter itself but throughout the system as well.

The recommended supply decoupling scheme is as follows: One 0.01µF to 0.033µF chip capacitor at every supply pin, with a +6.8µF to +10µF tantalum for each of the four main supplies feeds (within a few inches of the ADC). Note that supply feeds with excessive digital switching noise may require separate filtering using ferrite beads, additional capacitance, or split supplies. Proper bypassing of all other integrated circuits, especially logic circuits, should minimize power supply and ground transients.

All of the CLC936 grounds are internally connected. A single low-impedance ground plane is recommended for the CLC936. Split analog and digital grounds are not recommended for the CLC936. The SIGNAL GND is used internally for the track-and-hold and buffering amplifiers, while the other GROUND pins are essentially power supply returns.

The SIGNAL GND pins (pins 39 & 40) are very sensitive nodes, and should have a solid, low-impedance, ground connection. The path that the input signal and its return currents follow must be isolated from other circuitry. Single-point grounding at the converter should minimize common impedance paths which would allow other signals to directly couple into the analog input, affecting accuracy.

Thermal Considerations

The CLC936 dissipates approximately 5.4W. The following strategies can be applied to minimize junction temperatures:

a) A thick copper ground plane ... an appreciable amount of heat is conducted out of the A/D through its leads.
b) A copper or aluminum stand-off between the ground plane and the bottom of the CLC936 package (thermal paste may be useful).
c) A SIL PAD® between the ground plane and the bottom of the CLC936 package . To maximize heat conduction leave a patch of exposed (no solder mask) ground plane under the CLC936.
d) Moving air over the A/D converter.

Evaluation Board and Printed Circuit Board Layout

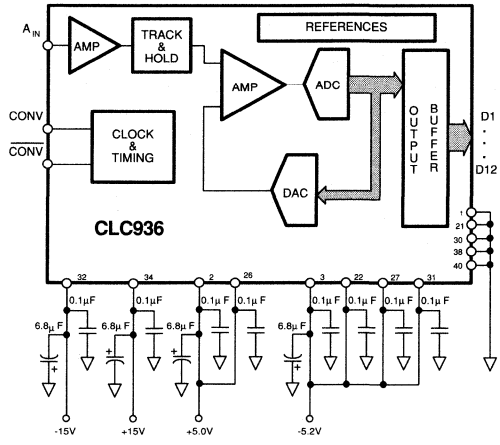
The keys to a successful CLC936 layout are a substantial low-impedance ground plane, short connections (in and out of the converter), and proper power supply decoupling. The use of a socket for the CLC936 is specifically not recommended in the final system design.

The CONVERT clock line traces should be equal length. If they are not equal, the edges may not arrive at the A/D at the same time, which may allow the clock signals to more easily couple into the analog input.

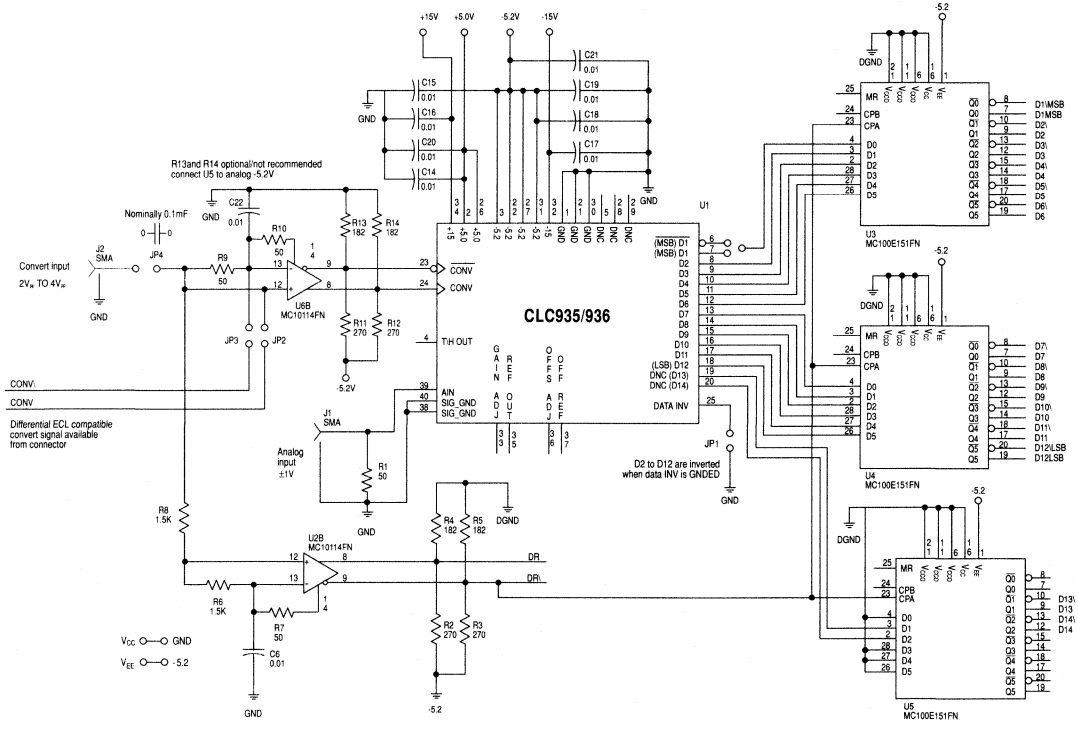
An evaluation board is available for the CLC936 (assembled - "E935PCASM", or bare board - "730025"). The evaluation board can be used to quickly evaluate the performance of the CLC936. Use of the evaluation board as a model is highly recommended.

Applications Support

Comlinear Corporation maintains a staff of applications engineers who are available for design and applications assistance. They can be reached at (303) 226-0500.



Recommended Power Supply Decoupling Scheme



Complete System Circuit

Comlinear Corporation

12-Bit, 25.6MSPS A/D Converter

CLC937

APPLICATIONS:

- radar processing
- FLIR processing/ electronic imaging
- instrumentation
- medical imaging
- transient-signal recorders

FEATURES (typical):

- 72dB spurious free signal range; f_{IN}=404kHz
- no missing codes guaranteed
- 0.7LSB differential linearity
- small package (2.28in²)

DESCRIPTION:

The CLC937 is a 12-bit analog-to-digital converter subsystem, including 12-bit quantizer, internal track-and-hold, references, and ECL compatible digital outputs. The CLC937 has been especially optimized for a Spurious-Free-Signal-Range of better than 70dB. The CLC937 is constructed using advanced thin-film hybrid technology in a fully certified MIL-STD-1772 facility.

Comprehensive dynamic testing on every part insures that system performance goals will be met, including spurious-free-signal-range (SFSR) of 65dB@9.22MHz. This, coupled with an SNR specification of 65dB@9.22MHz, means that the CLC937 is ideally suited for use in areas like radar and instrumentation signal processing.

The CLC937 incorporates a complete two-pass subranging architecture, constructed from several high-speed building blocks. A broadband (150MHz) input amplifier buffers input signals and provides an accurate drive signal to the on-board track-and-hold. Laser trimmed gain and offset assure accurate matching unit to unit. The latched outputs of the CLC937 mean that only a convert clock, analog input, and power supplies are required for operation; internal logic generates all required timing signals.

The CLC937AC is specified over a temperature range of 0°C to +70°C, while the CLC937A8C is specified over a range of -55°C to +125°C. Both devices are packaged in 40-pin, 1.1in wide, ceramic DIPs (note: leads are side brazed for easy access and inspection). Contact factory for availability of "gull-wing" surface-mount versions.

Ordering Information

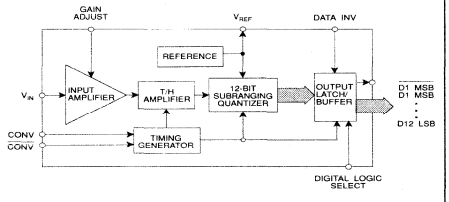
CLC937AC	0°C to +70°C	industrial version
CLC937A8C	-55°C to +125°C	MIL-STD-883, class B

Available summer of 1993.

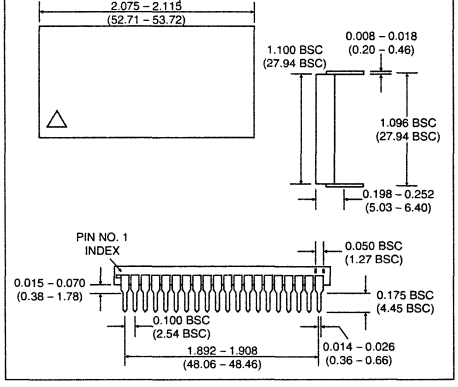
Both versions of the CLC937 are manufactured in Comlinear's MIL-STD-1772 certified facility in Fort Collins,Colorado, U.S.A.

Preliminary Data

Block Diagram



Package Dimensions



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Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_2$ = -15.0V; $-V_{EE}$ = -5.2V; unless specified)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS						UNITS	SYMBOL
			CLC937AC			CLC937A8C				
Case Temperature		+25°C	0°C	+25°C	+70°C	-55°C	+25°C	+125°C		
DYNAMIC CHARACTERISTICS										
small signal bandwidth	V_{IN} = 1/4 FS	150							MHz	SSBW
large signal bandwidth	V_{IN} = FS	150							MHz	LSBW
slew rate		350							V/µs	SR
overvoltage recovery time	V_{IN} = 2FS	14							ns	OR
effective aperture delay		0.4							ns	TA
aperture jitter		1.25							ps(RMS)	AJ
NOISE and DISTORTION (25.6MSPS)										
signal-to-noise ratio										
(not including harmonics)	404kHz; FS	66							dB	SNR1
	4.996MHz; FS	66							dB	SNR2
	9.220MHz; FS	65							dB	SNR3
in-band harmonics										
	404kHz; FS-1dB	-72							dBc	IBH1
	4.996MHz; FS-1dB	-70							dBc	IBH2
	9.220MHz; FS-1dB	-68							dBc	IBH3
spurious-free-signal-range										
	404kHz; FS-1dB	72							dB	SFSR1
	4.996MHz; FS-1dB	70							dB	SFSR2
	9.220MHz; FS-1dB	68							dB	SFSR3
intermodulation distortion (f_1=4.95MHz@FS-6.5dB; f_2=5.05MHz@FS-6.5dB)		75							dBc	IMD
noise-power-ratio (dc to xxMHz white noise; xxMHz slot)	FS-12dB								dB	NPR
DC ACCURACY and PERFORMANCE										
differential non-linearity	dc; FS	0.7							LSB	DNL
integral non-linearity	dc; FS	1.3							LSB	INL
missing codes		0	0	0	0	0	0	0	codes	MC
bipolar offset error		3.0							mV	VIO
temperature coefficient									µV/°C	DVIO
bipolar gain error		1.2							%FS	GE
temperature coefficient									%FS/°C	DVIO
ANALOG INPUT PERFORMANCE										
analog input bias current		10							µA	IBN
temperature coefficient		100							nA/°C	DIBN
analog input resistance		80							kΩ	RIN
analog input capacitance		3.5							pF	CIN
POWER REQUIREMENTS										
supply current ($+V_{CC}$ = +5.0V)	25.6MSPS; no load	380							mA	ICC
supply current ($-V_{EE}$ = -5.2V)[3]	25.6MSPS; no load	769							mA	IEE
supply current ($+V_1$ = +15.0V)	25.6MSPS; no load	3							mA	I1
supply current ($-V_2$ = -15.0V)	25.6MSPS; no load	42							mA	I2
nominal power dissipation[3]	25.6MSPS; no load	6.5							W	PD

Note 1: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Note 2: Junction temperature rise above case ≈ 16°C; θ_{CA}=16°C/W; θ_{CA}=7°C/W@500LFPM. Use of a SIL-PAD® #550007, from Berquist (1-800-347-4572), can lower case-to-ambient rise; θ_{CA} = 12°C/W@still air, 12in² ground-plane; θ_{CA}=3.4°C/W@100LFPM, 12in² ground-plane.

Note 3: Plan product improvements are expected to lower -5.2V supply current by 200mA, and nominal power dissipation by 1W.

Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_{EE}$ = -5.2V; $-V_1$ = -15.0V; unless specified)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS						UNITS	SYMBOL
			CLC937AC			CLC937A8C				
Case Temperature		+25°C	0°C	+25°C	+70°C	-55°C	+25°C	+125°C		
DIGITAL INPUTS										
input voltage	logic LOW		-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	V	VIL
	logic HIGH		-1.1	-1.1	-1.1	-1.1	-1.1	-1.1	V	VIH
input current	logic LOW		1.0	1.0	1.0	1.0	1.0	1.0	mA	IIL
	logic HIGH		1.0	1.0	1.0	1.0	1.0	1.0	mA	IIH
DIGITAL OUTPUTS										
output voltage	logic LOW		-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	V	VOL
	logic HIGH		-1.1	-1.1	-1.1	-1.1	-1.1	-1.1	V	VOH
TIMING										
maximum conversion rate		25.6							MSPS	CR
minimum conversion rate		0							MSPS	CRM
data hold time		TBD							ns	THLD
output propagation delay		TBD							ns	TDV

Recommended Operating Conditions

positive supply voltage ($+V_{CC}$)	+5V
positive supply voltage ($+V_1$)	+15V
negative supply voltage ($-V_{EE}$)	-5.2V
negative supply voltage ($-V_1$)	-15V
differential voltage between any two GND's	<10mV
analog input voltage range (Full Scale)	±1V
digital output current sinking	6mA(max)
sourcing	6mA(max)
digital input voltage range	-2.0V to 0.0V

Absolute Maximum Ratings[1]

positive supply voltage ($+V_{CC}$)	-0.5 to +7.0V
positive supply voltage ($+V_1$)	-0.5 to +18V
negative supply voltage ($-V_{EE}$)	+0.5 to -7.0V
negative supply voltage ($-V_1$)	+0.5 to -18.0V
differential voltage between any two GND's	200mV
analog input voltage range	$-V_{EE}$ to $+V_{CC}$
DIGITAL input voltage range	+0.5V to $-V_{EE}$
gain and offset adjust voltage range	$-V_{EE}$ to $+V_{CC}$
output short circuit duration (one pin to ground)	Infinite
Junction Temperature	+175°C
Operating Temperature Range[2]	
CLC937AC	0°C to +70°C
CLC937A8C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Solder Duration (+300°C)	10 sec

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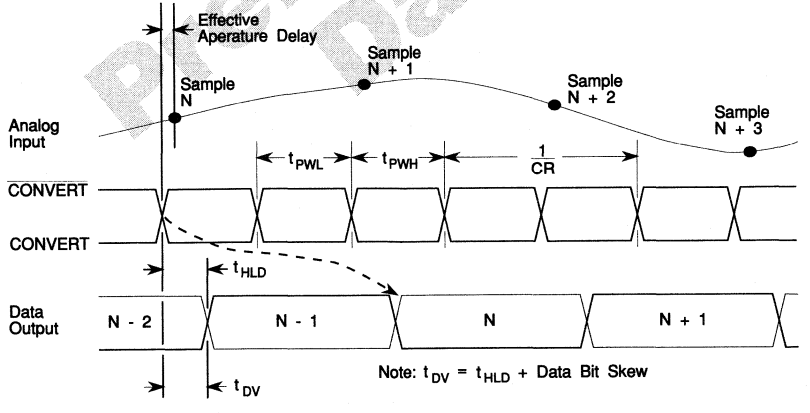
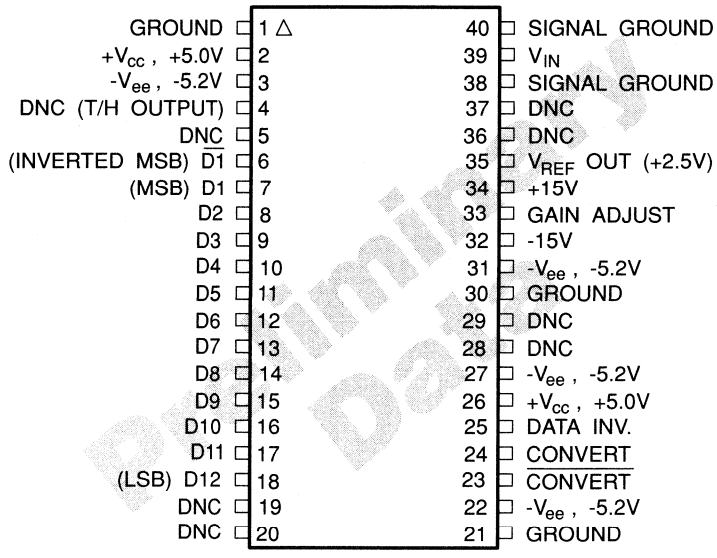
Timing Diagram



CLC937 Pinout



Pin Description and Usage

ECL-Level Digital Inputs

CONVERT, CONVERT — "Differential Convert Command" initiates a new conversion cycle on the rising edge of CONVERT.
Pins 23, 24

DATA INV — DATA INVERT is an active HIGH (grounded) ECL input which causes the data outputs [D2 to (LSB) D12] to be inverted. In normal operation, DATA INV is left floating or tied to ECL logic LOW.
Pin 25

ECL-Level Digital Outputs

(MSB) D1-D12 — Digital Data Outputs. D1 is the MSB; D12 is the LSB. In their normal state, the digital outputs offer Offset Binary output coding.
Pins 7 to 18

(MSB) D1 — Inverted version of the MSB, used for 2's Complement coding.
Pin 6

Analog Input

V_{IN} — Analog input with a $2V_{PP}$ input range from +1V to -1V.
Pin 39

Gain Adjust — The GAIN ADJUST has a +4V to +1V input range and scales the analog input full-scale range by -10% to +10% respectively. If unused, Gain Adjust should be left floating.
Pin 33

Miscellaneous

V_{REF} (+2.5V) — V_{REF} is a highly stable +2.500V voltage reference. (Recommended current drain ≤2mA.)
Pin 35

D.N.C — Do Not Connect.
Pins 5, 19, 20, 28, 29, 36,37

DNC (T/H Output) — Internal Track-and-Hold output voltage test point. Do not Connect.
Pin 4

Power and Ground

+5V, Pins 2,26; +15V, Pin 34; -5.2V, Pins 3, 22, 27, 31; -15V, Pin 32; GROUND, Pins 1, 21, 30, 38, 40.

Comlinear Corporation

12-Bit, 25.6MSPS A/D Converter

CLC950

APPLICATIONS:

- radar processing
- infrared/CCD imaging
- instrumentation
- medical imaging
- digital communications

FEATURES (typical):

- 72dBc spurious free dynamic range
- 69dB signal-to-noise ratio
- monolithic construction
- low power dissipation 1.5W
- complete subsystem design
- ±1V analog input range

DESCRIPTION:

The CLC950 is a complex monolithic 12-bit analog-to-digital converter subsystem, including 12-bit quantizer, track-and-hold, and on-board reference buffer. The CLC950 outputs are user selectable as either ECL or TTL compatible. The CLC950 has been especially optimized for high-dynamic range, low power operation with spurious performance in the low 70dBc range.

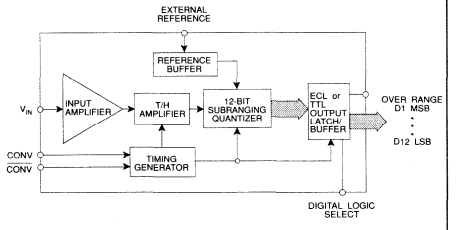
Comprehensive dynamic testing ensures that each part fully meets guaranteed specifications. Judicious power management and state-of-the-art track-and-hold design combine to provide a signal-to-noise ratio of approximately 69dB@10MHz analog input frequency. Spurious-free-dynamic range is approximately 72dBc@10MHz, significantly advancing ADC performance for high-speed monolithic 12-bit converters.

The CLC950 incorporates a proprietary quantizer architecture, which has been designed to minimize comparator count and the associated power dissipation penalty. The quantizer is combined with a high-dynamic range track-and-hold to form the heart of a full ADC sub-system, including necessary drive amplifiers and an on-board voltage reference buffer. Analog input signal, conversion clock, and power are all that are required for CLC950 operation.

The CLC950ACD is specified over the commercial temperature range of 0°C to 70°C, while the CLC950AID/A8D/A8L are extended temperature versions specified from -55°C to +125°C.

Advance Data

Block Diagram



Package Dimensions

Ordering Information

CLC950ACD	0°C to +70°C	Commercial DIP
CLC950AID	-55°C to +125°C	Industrial DIP
CLC950A8D*	-55°C to +125°C	MIL-STD-883 DIP
CLC950A8L*	-55°C to +125°C	MIL-STD-883 Surface Mount

Available spring 1994.

*Contact factory for availability of military versions.

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Electrical Characteristics ($+V_{CC}$ = +5.0V; $-V_{EE}$ = -5.2V; unless specified)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS						UNITS	SYMBOL
			CLC950ACD			CLC950AID/A8D/A8L[1]				
Case Temperature		+25°C	0°C	+25°C	+70°C	-55°C	+25°C	+125°C		
DYNAMIC CHARACTERISTICS										
small signal bandwidth	V_{IN} = 1/4 FS	200							MHz	SSBW
large signal bandwidth	V_{IN} = FS	175							MHz	LSBW
slew rate		300							V/µs	SR
overvoltage recovery time	V_{IN} = 2FS	TBD							ns	OR
effective aperture delay		-0.3							ns	TA
aperture jitter		1.6							ps(RMS)	AJ
NOISE and DISTORTION (25.6MSPS)										
signal-to-noise ratio										
(not including harmonics)	400kHz; FS	69							dB	SNR1
	12.49MHz; FS	68							dB	SNR2
in-band harmonics										
	400kHz; FS-1dB	-74							dBc	IBH1
	12.49MHz; FS-1dB	-72							dBc	IBH2
spurious-free-signal-range										
	407kHz; FS-1dB	74							dB	SFSR1
	12.49MHz; FS-1dB	72							dB	SFSR2
intermodulation distortion										
(f_1=2.3MHz@FS-6.5dB; f_2=2.4MHz@FS-6.5dB)		74							dBc	IMD
noise-power-ratio										
(dc to 8.2MHz white noise; 3.886MHz slot)	FS-12dB								dB	NPR
DC ACCURACY and PERFORMANCE										
differential non-linearity	dc; FS	0.5							LSB	DNL
integral non-linearity	dc; FS	1.0							LSB	INL
missing codes		0	0	0	0				codes	MC
bipolar offset error		4							mV	VIO
temperature coefficient									µV/°C	DVIO
bipolar gain error		1.2							%FS	GE
temperature coefficient									%FS/°C	DVIO
ANALOG INPUT PERFORMANCE										
analog input bias current		10							µA	IBN
temperature coefficient		100							nA/°C	DIBN
analog input resistance		150							kΩ	RIN
analog input capacitance		4							pF	CIN
POWER REQUIREMENTS										
supply current ($+V_{CC}$ = +5.0V)	25.6MSPS; no load	TBD							mA	ICC
supply current ($-V_{EE}$ = -5.2V)	25.6MSPS; no load	TBD							mA	IEE
nominal power dissipation	25.6MSPS; no load	1.5							W	PD

Note 1: Contact factory for military grade product availability.

Note 2: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Note 3: Junction temperature rise above case ≈ xx°C; θ_{CA}=xx°C/W; θ_{CA}=xx°C/W@500LFPM. Use of a SIL-PAD® #xxxxxx, from Berquist (1-800-347-4572), can lower case-to-ambient rise; θ_{CA} = xx°C/W@still air, 12in² ground-plane; θ_{CA}=xx°C/W@100LFPM, 12in² ground-plane.

Electrical Characteristics ($+V_{CC}$ = +5.0V; $-V_{EE}$ = -5.2V; unless specified)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS						UNITS	SYMBOL
			CLC950ACD			CLC950AID/A8D/A8L[1]				
Case Temperature		+25°C	0°C	+25°C	+70°C	-55°C	+25°C	+125°C		
DIGITAL INPUTS										
input voltage ECL mode	logic LOW		0.8	0.8	0.8				V	VIL
	logic HIGH		2.0	2.0	2.0				V	VIH
input current ECL mode	logic LOW		100	100	100				µA	IIL
	logic HIGH		100	100	100				µA	IIH
input voltage TTL mode	logic LOW		-1.5	-1.5	-1.5				V	VIL
	logic HIGH		-1.1	-1.1	-1.1				V	VIH
input current TTL mode	logic LOW		100	100	100				µA	IIL
	logic HIGH		100	100	100				µA	IIH
DIGITAL OUTPUTS										
output voltage ECL mode	logic LOW		-1.5	-1.5	-1.5				V	VOL
	logic HIGH		-1.1	-0.1	-0.1				V	VOH
output voltage TTL mode	logic LOW		0.4	0.4	0.4				V	VOL
	logic HIGH		2.4	2.4	2.4				V	VOH
TIMING										
maximum conversion rate			25.6	25.6	25.6				MSPS	CR
minimum conversion rate		0	0	0	0				MSPS	CRM
data hold time		TBD							ns	THLD
output propagation delay		TBD							ns	TDV

Recommended Operating Conditions

positive supply voltage ($+V_{CC}$)	+5.0V
negative supply voltage ($-V_{EE}$)	-5.2V
differential voltage between any two GND's	10mV
analog input voltage range	±1V
digital output current sinking (ECL mode)	6mA(max)
sourcing (ECL mode)	6mA(max)
digital input voltage range (ECL mode)	-2.0V to 0.0V
digital input voltage range (TTL mode)	0V to $+V_{CC}$

Absolute Maximum Ratings[2]

positive supply voltage ($+V_{CC}$)	-0.5V to +6.0V
negative supply voltage ($-V_{EE}$)	+0.5V to -6.0V
differential voltage between any two GND's	200mV
analog input voltage range	$-V_{EE}$ to $+V_{CC}$
DIGITAL input voltage range (ECL)	0V to $-V_{EE}$
output short circuit duration (one pin to ground)	Infinite
Junction Temperature	+175°C
Operating Temperature Range[3]	
CLC950ACD	0°C to +70°C
CLC950AID/A8D/A8L[1]	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Solder Duration (+300°C)	10 sec

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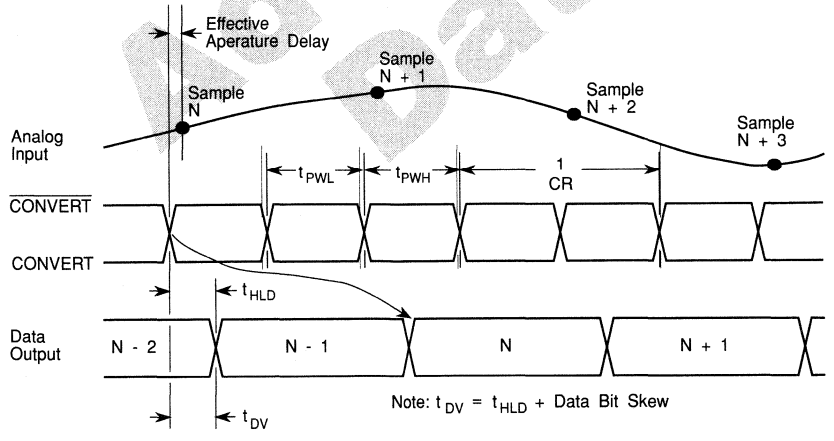
Timing Diagram



CLC950 Pinout

Pin Description and Usage

Application Notes
Contents

Current-Feedback Amplifiers

The use of clever circuit architectures and the development of high-speed complementary BJT processes make it possible to achieve monolithic speeds and bandwidths hitherto available only in hybrid form.

—Sergio Franco, San Francisco State University
1600 Holloway Avenue, San Francisco, CA 94132

In their effort to approximate the ideal op amp, manufacturers must not only maximize the open-loop gain and minimize input-referred errors such as offset voltage, bias current, and noise, but must also ensure adequate bandwidth and settling-time characteristics. Amplifier dynamics are particuularly important in applications like high-speed DAC buffers, subranging ADCs, S/H circuits, ATE pin drivers, and video and IF drivers.[1]

Being basically voltage-processing devices, op amps are subject to the speed limitations inherent to voltage-mode operation, stemming primarily from the stray capacitances of nodes and the cutoff frequencies of transistors. Particularly severe is the effect of the stray capacitances between the input and output nodes of high-gain inverting stages because of the Miller effect which multiplies the stray capacitance by the voltage gain of the stage.

On the other hand, it has long been recognized that current manipulation is inherently faster than voltage manipulation. The effect of stray inductances in a circuit is usually less severe than that of its stray capacitances, and BJTs can switch currents much more rapidly than voltages. These technological reasons form the basis of emitter-coupled logic, bipolar DACs, current conveyors, and the high-speed amplifier topology known as *current-feedback*.[2]

For true current-mode operation, all nodes in the circuit should ideally be kept at fixed voltages to avoid the slow-down effect by their stray capacitances. However, since the output of the amplifier must be a voltage, some form of high-speed voltage-mode operation must also be provided at some point. This is achieved by employing gain configurations that are inherently immune from the Miller effect, such as the common-collector and the cascode configurations, and by driving the nodes with push-pull stages to rapidly charge/discharge their stray capacitances.

To ensure symmetric rise and fall times, the npn and pnp transistors must have comparable characteristics in terms of cutoff frequency f_t. Traditionally, monolithic pnp's have been plagued by much poorer performance characteristics than their npn counterparts. However, the recent development of truly complementary high-speed processes makes it possible to achieve monolithic speeds that were hitherto available only in hybrid form.

The advantages of the current-feedback topology are best appreciated by comparing it against that of the conventional op amp.[3,4]

The Conventional Op Amp

The conventional op amp consists of a high input-impedance differential stage followed by additional gain stages, the last of which is a low output-impedance stage. As shown in the circuit model of Fig. 1a, the op amp transfer characteristic is

$$V_o = a(jf)V_d \qquad (1)$$

where V_o is the output voltage; $V_d = V_p - V_n$ is the differential input voltage; and $a(jf)$, a complex function of frequency f, is the open-loop gain.

Connecting an external network as in Fig. 1b creates a feedback path along which a signal in the form of a *voltage* is derived from the output and applied to the noninverting input. By inspection.

$$V_d = V_i - \frac{R_1}{R_1 + R_2} V_o \qquad (2)$$

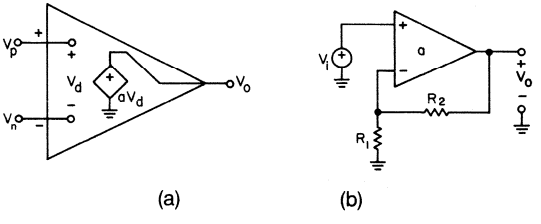


Fig. 1: Circuit model of the conventional op amp, and connection as a noninverting amplifier.

Substituting into Eq. (1), collecting, and solving for the ratio V_o/V_i yields the familiar noninverting amplifier transfer characteristic

$$A(jf) \triangleq \frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + 1/T(jf)} \qquad (3)$$

where $A(jf)$ represents the closed-loop gain, and

$$T(jf) = \frac{a(jf)}{1 + R_2/R_1} \qquad (4)$$

represents the loop gain.

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The designation *loop gain* stems from the fact that if we break the loop as in Fig. 2a and inject a test signal V_x with V_i suppressed, the circuit will first attenuate V_x to produce $V_n = V_x/(1 + R_2/R_1)$, and then amplify V_n to produce $V_o = -aV_n$. Hence, the gain experienced by a signal in going around the loop is $V_o/V_x = -a/(1 + R_2/R_1)$. The *negative* of this ratio represents the loop gain, $T \triangleq -(V_o/V_x)$. Hence, Eq. (4).

The loop gain gives a measure of how close A is to the ideal value $1 + R_2/R_1$, also called the *noise gain* of the circuit. By Eq. (3), the larger *T*, the better. To ensure substantial loop gain over a wide range of closed-loop gains, op amp manufacturers strive to make *a* as large as possible. Consequently, V_d will assume extremely small values since $V_d = V_o/a$. In the limit $a \to \infty$ we obtain $V_d \to 0$, that is, $V_n \to V_p$. This forms the basis of the familiar op amp rule: when operated with negative feedback, an op amp will provide whatever output voltage and current are needed to ideally force V_n to follow V_p.

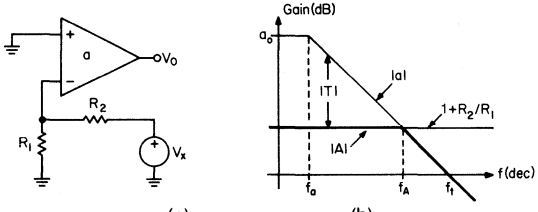

Fig. 2: Test circuit to find the loop gain, and graphical method to determine the closed-loop bandwidth f_A.

Gain-Bandwidth Tradeoff

Large open-loop gains can physically be realized only over a limited frequency range. Past this range, gain rolls off with frequency. Most op amps are designed for a constant rolloff of −20dB/dec, so that the open-loop response can be expressed as

$$a(jf) = \frac{a_o}{1 + j(f/f_a)} \qquad (5)$$

where a_o represents the *dc gain*, and f_a is the −3dB *frequency* of the open-loop response. Both parameters can be found from the data sheets. For example, the 741 op amp has $a_o \simeq 2 \times 10^5$ and $f_a \simeq 5$Hz.

Substituting Eq. (5) into Eq. (4) and then into Eq. (3), and exploiting the fact that $(1 + R_2/R_1)\, a_o \ll 1$, we obtain

$$A(jf) = \frac{1 + R_2/R_1}{1 + j(f/f_A)} \qquad (6)$$

where

$$f_A = \frac{f_t}{1 + R_2/R_1} \qquad (7)$$

represents the *closed-loop bandwidth*, and $f_t = a_o f_a$ represents the open-loop unity-gain frequency, that is the frequency at which $|a| = 1$. For instance, the 741 op amp has $f_t = 2 \times 10^5 \times 5 = 1$ MHz.

Equation (7) reveals a gain-bandwidth tradeoff. As we raise the R_2/R_1 ratio to increase the closed-loop gain, we also decrease its bandwidth in the process. Moreover, by Eq. (4), the loop-gain is also decreased, thus leading to a greater closed-loop gain error.

The above concepts can also be visualized graphically. Since Eq. (4) implies $|T|_{dB} \triangleq 20 \log |T| = 20 \log |a| - 20 \log (1 + R_2/R_1) \triangleq |a|_{dB} - (1 + R_2/R_1)_{dB}$, it follows that the loop gain can be found graphically as the *difference* between the open-loop gain and the noise gain. This is shown in Fig. 2b. The frequency at which the two curves meet is called the *crossover frequency*. At this frequency we have $T = 1\angle -90° = -j$, that is, $|A| = (1 + R_2/R_1)/\sqrt{2}$. Thus, the crossover frequency represents the −3dB frequency of the closed-loop response, that is, the closed-loop bandwidth f_A.

We now see that increasing the closed-loop gain shifts the noise-gain curve upward, thus reducing the loop gain, and causes the crosspoint to move up the $|a|$ curve, thus decreasing the closed-loop bandwidth. Clearly, the circuit with the widest bandwidth and the highest loop gain is also the one with the lowest closed-loop gain. This is the voltage follower, for which $R_2/R_1 = 0$, so that $A = 1$ and $f_A = f_t$.

Slew-Rate Limiting

To fully characterize the dynamic behavior of an op amp, we also need to know its *transient response*. If an op amp with the response of Eq. (5) is operated as a unity-gain voltage follower and is subjected to a suitably small voltage step, its dynamic behavior will be similar to that of an *RC* network. Applying an input step ΔV_i will cause the output to undergo an exponential transition with magnitude $\Delta V_o = \Delta V_i$, and with a time-constant $\tau = 1/(2\pi f_t)$. For the 741 op amp we have $\tau = 1/(2\pi \times 10^6) \simeq 170$ ns.

The rate at which the output changes with time is highest at the beginning of the exponential transition, when its value is $\Delta V_o/\tau$. Increasing the step magnitude increases this initial rate of change, until the latter will saturate at a value called the slew-rate (SR). This effect stems from the limited ability of the internal circuitry to charge/discharge capacitive loads, especially the compensation capacitor responsible for open-loop bandwidth f_a.

To illustrate, refer to the circuit model of Fig. 3, which is typical of many op amps.[4] The input stage is a transconductance block consisting of differential pair Q_1–Q_2 and current mirror Q_3–Q_4. The remaining stages are lumped together as an integrator block consisting of an inverting amplifier and the compensation capacitor *C*. Slew-rate limiting occurs when the transconductance stage is driven into saturation, so that all the current available to charge/discharge *C* is the bias current *I* of this stage. For example, the 741 op amp has $I = 20\ \mu$A and $C = 30$ pF, so that $SR = I/C = 0.67\ V/\mu s$. The step magnitude corresponding to the onset of slew-rate limiting is such that $\Delta V_i/\tau = SR$, that is, $\Delta V_i = SR \times \tau = (0.67\ V/\mu s) \times (170\ ns) = 116$ mV. As long as the step is less than 116 mV, a 741 voltage follower will respond with an exponential transition governed by $\tau \simeq 170$ ns, whereas for a greater input step the output will slew at a constant rate of $0.67\ V/\mu s$.

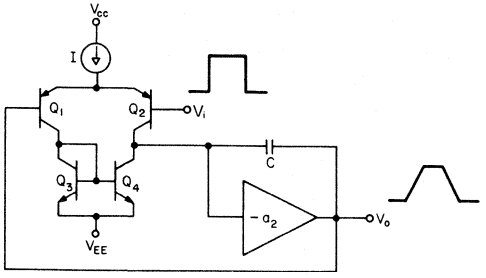

Fig. 3: Simplified slew-rate model of a conventional op amp.

In many applications the dynamic parameter of greatest concern is the *settling time*, that is, the time it takes for the output to settle and remain within a specified band around its final value, usually for a full-scale output transition. Clearly, slew-rate limiting plays an important role in the settling-time characteristic of the device.

The Current-Feedback Amplifier

As shown in the circuit model of Fig. 4, the architecture of the current-feedback amplifier (CF amp) differs from the conventional op amp in two respects:[2]

1. The input stage is a *unity-gain voltage buffer* connected across the inputs of the op amp. Its function is to force V_n to follow V_p, very much like a conventional op amp does via negative feedback. However, because of the low output impedance of this buffer, current can easily flow in or out of the inverting input, though we shall see that in normal operation this current is extremely small.

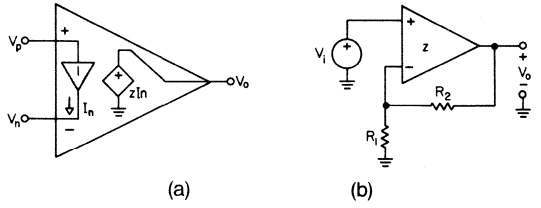

Fig. 4: Circuit model of the current-feedback amplifier, and connection as a noninverting amplifier.

2. Amplification is provided by a *transimpedance amplifier* which senses the current delivered by the buffer to the external feedback network, and produces an output voltage V_o such that

$$V_o = z(jf)I_n \qquad (8)$$

where $z(jf)$ represents the *transimpedance gain* of the amplifier, in V/A or Ω, and I_n is the current out of the inverting input.

To fully appreciate the inner workings of the CF amp, it is instructive to examine the simplified circuit diagram of Fig. 5a. The input buffer consists of transistors Q_1 through Q_4. While Q_1 and Q_2 form a low output-impedance push-pull stage, Q_3 and Q_4 provide V_{BE} compensation for the push-pull pair, as well as a Darlington function to raise the input impedance.

Summing currents at the inverting node yields $I_1 - I_2 = I_n$, where I_1 and I_2 are the push-pull transistor currents. Two Wilson current mirrors, consisting of transistors Q_9–Q_{10}–Q_{11} and Q_{13}–Q_{14}–Q_{15}, reflect these currents and recombine them at a common node, whose equivalent capacitance to ground has been designated as *C*. By mirror action, the current through this capacitance is $I_C = I_1 - I_2$, that is

$$I_C = I_n \qquad (9)$$

The voltage developed by *C* in response to this current is then conveyed to the output via a second buffer, consisting of Q_5 through Q_8. The salient features of the CF amp are summarized in block diagram form in Fig. 5b.

When the amplifier loop is closed as in Fig. 4b, and whenever an external signal tries to imbalance the two inputs, the input buffer will begin sourcing (or sinking) an imbalance current I_n to the external resistances. This imbalance is then conveyed by the Wilson mirrors to capacitor *C*, causing V_o to swing in the positive (or negative) direction until the original imbalance I_n is neutralized via the negative feedback loop. Thus, I_n plays the role of error signal in the system.

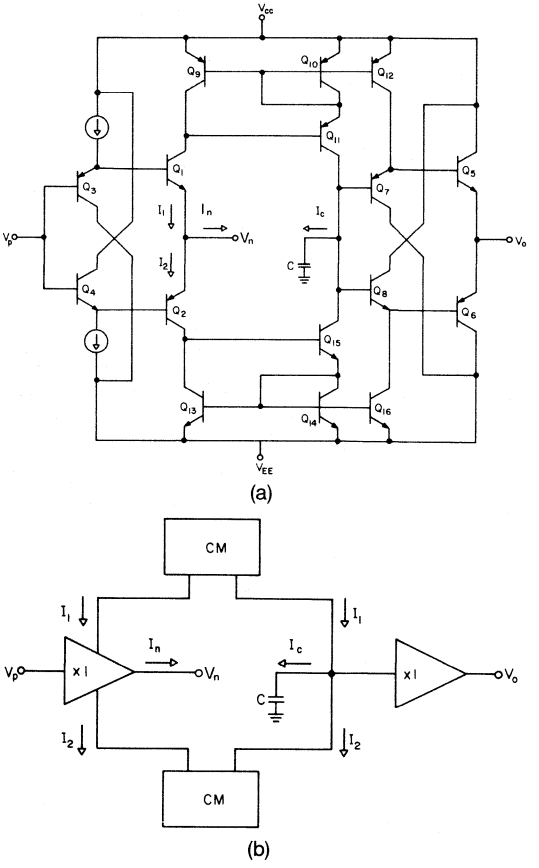

Fig. 5: Simplified circuit diagram and block diagram of a current-feedback amplifier. *(Courtesy of Comlinear Corporation.)*

To obtain the closed-loop transfer characteristic, refer again to Fig. 4b. Summing currents at the inverting node yields

$$I_n = \frac{V_n}{R_1} - \frac{V_o - V_n}{R_2} \qquad (10)$$

since the buffer ensures $V_n = V_p = V_i$ we can rewrite as

$$I_n = \frac{V_i}{R_1 \parallel R_2} - \frac{V_o}{R_2} \qquad (11)$$

confirming that the feedback signal V_o/R_2 is now in the form of a *current*. Substituting into Eq. (8), collecting, and solving for the ratio V_o/V_i yields

$$A(jf) \triangleq \frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + 1/T(jf)} \qquad (12)$$

where $A(jf)$ represents the *closed-loop gain* of the circuit, and

$$T(jf) = \frac{z(jf)}{R_2} \qquad (13)$$

represents the *loop gain*. This designation stems again from the fact that if we break the loop as in Fig. 6a, and inject a test voltage V_x with the input V_i suppressed, the circuit will first convert V_x to the current $I_n = -V_x/R_2$, and then convert I_n to the voltage $V_o = zI_n$, so that $T \triangleq -(V_o/V_x) = z/R_2$, as expected.

In an effort to ensure substantial loop gain to reduce the closed-loop gain error, manufacturers strive to make z as large as possible relative to the expected values of R_2. Consequently, since $I_n = V_o/z$, the inverting-input current will be very small, though this input is a low-impedance node because of the buffer. In the limit $z \to \infty$ we obtain $I_n \to 0$, indicating that a CF amp will provide whatever output voltage and current are needed to ideally drive I_n to zero. Thus, the conventional op amp conditions $V_n = V_p$ and $I_n = I_p = 0$ hold for CF amps as well.

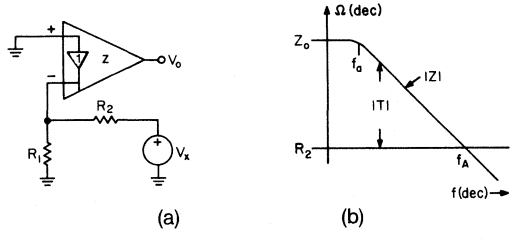

Fig. 6: Test circuit to find the loop gain, and graphical method to determine the closed-loop bandwidth f_A.

No Gain-Bandwidth Tradeoff

The transimpedance gain of a practical CF amp rolls off with frequency according to

$$z(jf) = \frac{z_o}{1 + j(f/f_a)} \qquad (14)$$

where z_o is the *dc value* of the transimpedance gain, and f_a is the frequency at which rolloff begins. For instance, from the data sheets of the CLC401 CF amp (Comlinear Co.) we find $z_o = 710$ kΩ, and $f_a = 350$ kHz.

Substituting Eq. (14) into Eq. (13) and then into Eq. (12), and exploiting the fact that $R_2/z_o \ll 1$, we obtain

$$A(jf) = \frac{1 + R_2/R_1}{1 + j(f/f_A)} \qquad (15)$$

where

$$f_A = \frac{z_o f_a}{R_2} \qquad (16)$$

represents the *closed-loop bandwidth*. for R_2 in the kΩ range, f_A is typically in the 100 MHz. Retracing previous reasoning, we see that the noise-gain curve is now R_2, and that f_A can be found graphically as the frequency at which this curve meets the $|z|$ curve, see Fig. 6b.

Comparing with Eqs. (6) and (7), we note that the closed-loop gain expressions are formally identical. However, the bandwidth now depends only on R_2 rather than on the closed-loop gain $1 + R_2/R_1$. Consequently, we can use R_2 to select the bandwidth, and R_1 to select the gain. The ability to control gain independently of bandwidth constitutes a major advantage of CF amps over conventional op amps, especially in automatic gain control applications. This important difference is highlighted in Fig. 7.

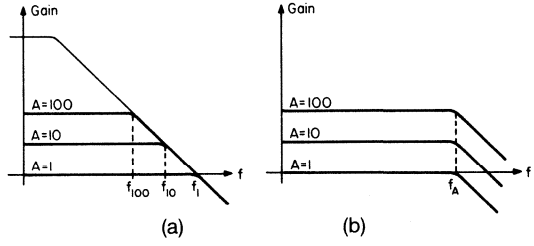

Fig. 7: Comparing the gain-bandwidth relationship of conventional op amps and current-feedback amplifiers.

Absence of Slew-Rate Limiting

The other major advantage of CF amps is the inherent absence of slew-rate limiting. This stems from the fact that the current available to charge the internal capacitance at the onset of a step is proportional to the step regardless of its size. Indeed, applying a step ΔV_i induces, by Eq. (11), an initial current imbalance $I_n = \Delta V_i/(R_1 \parallel R_2)$, which the Wilson mirrors then convey to the capacitor. The initial rate of charge is, therefore, $I_c/C = I_n/C = \Delta V_i/[(R_1 \parallel R_2)C] = [\Delta V_i(1 + R_2/R_1)]/(R_2C) = \Delta V_o/(R_2C)$, indicating an exponential output transition with time-constant $\tau = R_2C$. Like the frequency response, the transient response is governed by R_2 alone, regardless of the closed-loop gain. With R_2 in the kΩ range and C in the pF range, τ comes out in the ns range.

The *rise time* is defined as the amount of time t_r it takes for the output to swing from 10% to 90% of the step size. For an exponential transition, $t_r = \tau \times \ln(0.9/0.1) = 2.2\tau$.

For example, the CLC401 has $t_r = 2.5$ ns for a 2V output step, indicating an effective τ of 1.14 ns. The time it takes for the output to settle within 0.1% of the final value is $t_s = \tau \ln 1000 \simeq 7\tau$. For the CLC401, this yields $t_s \simeq 8$ ns, in reasonable agreement with the data sheet value of 10 ns.

The absence of slew-rate limiting not only allows for faster settling times, but also eliminates slew-rate related nonlinearities such as intermodulation distortion. This makes CF amps attractive in high-quality audio amplifier applications.

Second-Order Effects

The above analysis indicates that once R_2 has been set, the dynamics of the amplifier are unaffected by the closed-loop gain setting. In practice it is found that bandwidth and rise time do vary with gain somewhat, though not as drastically as with conventional op amps. The main cause is the non-zero output impedance of the input buffer, whose effect is to alter the loop gain and, hence, the closed-loop dynamics.

Referring to Fig. 8a and denoting this impedance as R_o, we note that the circuit first converts V_x to a current $I_{R2} = V_x/(R_2 + R_1 \| R_o)$, then it divides I_{R2} to produce $I_n = I_{R2} R_1/(R_1 + R_o)$, and finally it converts I_n to the voltage $V_o = zI_n$. Eliminating I_{R2} and I_n and letting $T = -V_o/V_x$ yields $T = z/Z_2$, where

$$Z_2 = R_2 \left(1 + \frac{R_o}{R_1 \| R_2} \right) \qquad (17)$$

Thus, the effect of R_o is to increase the noise gain from R_2 to $R_2[1 + R_o/(R_1 \| R_2)]$, see Fig. 8b, curve 1. Consequently, both bandwidth and rise time will be reduced by a proportional amount.

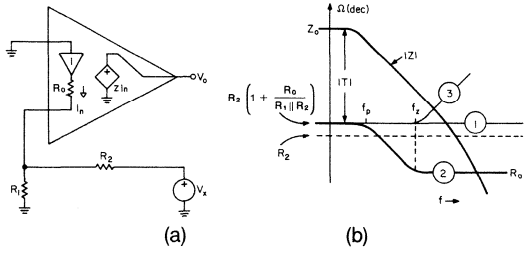

Fig. 8: Test circuit to investigate the effect of R_o, and noise-gain curves for the case of: (1) purely resistive feedback, (2) a capacitance in parallel with R_2, and (3) the same capacitance in parallel with R_1.

Replacing R_2 with Z_2 in Eq. (16) yields, after simple manipulation,

$$f_A = \frac{f_t}{1 + \frac{R_o}{R_2}\left(1 + \frac{R_2}{R_1}\right)} \qquad (18)$$

where $f_t = z_o f_a / R_2$ represents the extrapolated value of f_A in the limit $R_o \to 0$. This equation indicates that bandwidth reduction due to R_o will be more pronounced at high closed-loop gains. As an example, suppose a CF amp has $R_o = 50\Omega$, $R_2 = 1.5$ kΩ, and $f_t = 100$ MHz, so that $f_A = 10^8/[1 + (50/1500)A_o] = 10^8/(1 + A_o/30)$, where $A_o = 1 + R_2/R_1$. Then, the bandwidths corresponding to $A_o = 1$, 10, and 100 are, respectively, $f_1 = 96.8$ MHz, $f_{10} = 75.0$ MHz, and $f_{100} = 23.1$ MHz. Note that these values still compare favorably with a conventional op amp, whose bandwidth would be reduced, respectively, by 1, 10, and 100.

If so desired, the external resistance values can be predistorted to compensate for the bandwidth reduction at high gains. Turning Eq. (18) around yields the required value of R_2 for a given bandwidth f_A and gain A_o.

$$R_2 = \frac{z_o f_a}{f_A} - R_o A_o \qquad (19)$$

while the required value of R_1 for the given gain A_o is

$$R_1 = \frac{R_2}{A_o - 1} \qquad (20)$$

As an example, suppose we want the above amplifier to retain its 100 MHz bandwidth at a closed-loop gain of 10. Since with $R_2 = 1.5$ kΩ this device has $z_o f_a / R_2 = 100$ MHz, it follows that $z_o f_a = 10^8 \times 1500 = 1.5 \times 10^{11}\ \Omega \times$ Hz. Then, the above equations yield $R_2 = 1.5 \times 10^{11}/10^8 - 50 \times 10 = 1$ kΩ, and $R_1 = 1000/(10 - 1) = 111\ \Omega$.

Besides the dominant pole at f_a, the open-loop response of a practical amplifier presents additional poles above the crossover frequency. As shown in Fig. 8b, the effect of these poles is to cause a steeper gain rolloff at this frequency, further reducing the closed-loop bandwidth. Moreover, the additional phase-shift due to these poles decreases the phase margin somewhat, thus causing a small amount of peaking in the frequency response, and ringing in the transient response.

Finally, it must be said that the rise time of a practical CF amp does increase with the step size somewhat, due primarily to transistor current gain degradation at high current levels. For instance, the rise time of the CLC401 changes from 2.5 ns to 5 ns as the step size is changed from 2V to 5V. In spite of second-order limitations, CF amps still provide superior dynamics.

CF Applications Considerations

Although the above treatment has focused on the non-inverting configuration, the CF amp will work as well in most other resistive feedback configurations, such as the inverting amplifier, the summing and differencing amplifier, I-V and V-I converters, and KRC active filters.[4] In fact, the derivation of the transfer characteristic of any of these circuits proceeds along the same lines as conventional op amps. Special consideration, however, require the cases in which the feedback network includes reactive elements, either intentional or parasitic.

Consider first the effect of a *feedback capacitance* C_2 in parallel with R_2 in the basic circuit of Fig. 8a. Letting $Z = R_2 \| (1/sC_2)$, the noise gain becomes $Z_2 = Z[1 + R_o/(R_1 \| Z)]$. After expanding, it is readily seen that the noise-gain curve has a pole at $f_p = 1/(2\pi R_2 C_2)$ and a zero at $f_z = 1/[2\pi(R_o \| R_1 \| R_2)C_2]$, as shown in Fig. 8b, curve 2. Consequently, the crossover frequency will be pushed into the region of substantial

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phase shift due to the higher-order poles of z. If the overall shift reaches $-180°$ at this frequency, then $T = 1\angle -180° = -1$ there, indicating that A will become infinite by Eq. (12), and the circuit will oscillate. Even if the phase shift fails to reach $-180°$, the closed-loop response may still exhibit intolerable peaking and ringing. Hence, capacitive feedback must be avoided with CF amps. To minimize the effect of stray feedback capacitances, manufacturers often provide R_2 internally.

CF Integrators

To synthesize the integrator function in CF form, which provides the basis for dual-integrator-loop filters and oscillators as well as other popular circuits, we must use configurations that avoid a direct capacitance between the output and the inverting input. One possibility is offered by the Deboo integrator,[4] which belongs to the class of KRC filters and is therefore amenable to CF realization. Its drawback is the need for tightly matched resistances, if lossless integration is desired. The alternative of Fig. 9 not only meets the given constraint, but also provides *active compensation*, a highly desirable feature to cope with Q-enhancement problems in dual-integrator-loop filters.[4] Using standard op amp analysis techniques, it is readily seen that the unity-gain frequency of this integrator is $f_0 = (R_2/R_1)/(2\pi RC)$.

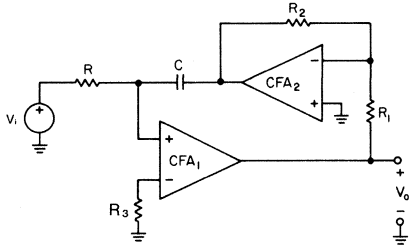

Fig. 9: Actively-compensated CF integrator.

Stray Input-Capacitance Compensation

Next, consider the effect of an *input capacitance* C_1 in parallel with R_1 in the basic circuit of Fig. 8a. Letting $Z = R_1 \| (1/sC_1)$, the noise gain is now $Z_2 = R_2[1 + R_0/(Z \| R_2)]$. After expanding, it is readily seen that the noise-gain curve has a zero at $f_z = 1/[2\pi(R_0 \| R_1 \| R_2)C_1]$, as shown in Fig. 8b, curve 3. If C_1 is sufficiently large, the phase of T at the crossover frequency will again approach $-180°$, bringing the circuit on the verge of instability. This is of particular concern in current-mode DAC output buffering, where C_1 is the output capacitance of the DAC, typically in the range of a few tens to a few hundreds of picofarads, depending on the DAC type.

Like a conventional op amp, the CF amp can be stabilized by using a feedback capacitance C_2 to introduce sufficient phase-lead to compensate for the phase-lag due to the input capacitance C_1. For a phase margin of 45°, choose the value of C_2 so that the noise-gain pole $f_p = 1/(2\pi R_2 C_2)$ coincides with the crossover frequency f_A, as shown in Fig. 10a. Using asymptotic Bode-plot reasoning,[4] it is easily seen that $f_A = [z_0 f_a f_z/(R_0 + R_2)]^{1/2}$, where $f_z = 1/[2\pi(R_0 \| R_2)C_1]$. Imposing $f_p = f_A$ yields

$$C_2 = \left(\frac{R_0}{2\pi R_2 z_0 f_a} C_1 \right)^{1/2} \qquad (21)$$

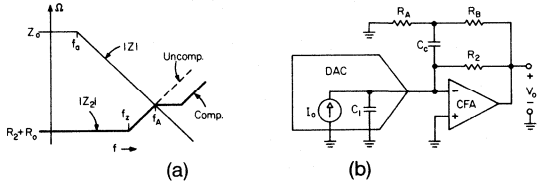

Fig. 10: DAC output capacitance compensation.

To cope with impractically low values of C_2, it is convenient to drive C_2 with a voltage divider as in Fig. 10b, since this will scale the value of C_2 to the more practical value

$$C_c = \left(1 + \frac{R_B}{R_A} \right) C_2 \qquad (22)$$

It can be shown that for this technique to be effective we must choose $R_B \ll R_2$. As an example, suppose a DAC having $C_1 = 100$ pF feeds the CF amp considered earlier. Then, Eq. (21) yields $C_2 = [50 \times 100 \times 10^{-12}/(2\pi \times 1.5 \times 10^3 \times 1.5 \times 10^{11})]^{1/2} = 1.88$ pF. To scale it to a more practical value, use [5] $R_A = 50\Omega$ and $R_B = 500\Omega$. Then, $C_c = (1 + 500/50)\,1.88 \simeq 21$ pF. This estimate may require some fine tuning to optimize the transient response.

Additional useful application hints can be found in Ref. [5].

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Application Note 103-1

"Flash" Analog to Digital Converters: Optimizing Performance

Wayne Lonowski

INTRODUCTION

Flash analog-to-digital converters have gained popularity due to their extremely high conversion rates and their potential for use in digitizing wideband analog signals. Flash converters have a substantial speed advantage over other conversion techniques such as successive approximation and dual-slope integration. However, many of the problems encountered with slower speed A to D techniques are accentuated in flash applications, and a myriad of new considerations must be addressed.

This application note presents pertinent background information on A to D conversion as well as the basics of flash A to D techniques. Finally, this note addresses practical considerations vital to the successful implementation of a flash A to D converter.

BACKGROUND

There are a few fundamental considerations that are critical in any A to D conversion system. The first is sampling rate. Sampling rate establishes a ceiling on the frequency of the signals that the digitizer can process accurately. The Nyquist sampling criterion states that defining a sinusoidal input signal in terms of its frequency and amplitude requires at least two samples per cycle. As an example, in a system with a 10MHz sampling rate, the highest frequency component that the digitizer can accurately define is 5MHz.

A related topic is aliasing. The relationship of a continuous time Fourier transform of an analog signal and the fourier transform of a sequence derived by sampling that signal is such that the upper frequencies of the continuous time transform may be reflected into the lower frequencies of the sampled transform. This phenomenon, where a high frequency componenet takes on the identity of a lower frequency, is called aliasing (See Figure 1). To avoid this, the analog signal must be sampled at a rate at least twice the frequency of any signal (or its harmonics) which has an amplitude of at least one-half LSB.

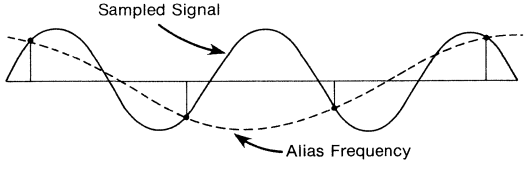

Figure 1: Inadequate sampling of the input waveform produces aliasing errors. If the sampling rate is slightly less than twice per cycle, an apparent low frequency sinusoid is created as part of the recovered signal.

This can impose some formidable restrictions. For example, for 8 bits of resolution, one-half LSB represents .2% of a full scale input. If an ideal square wave is being sampled, the first 635 harmonics have amplitudes of .2% or greater. Thus, if the fundamental frequency is 1MHz, the needed sampling rate is 2(635)(1MHz)=1.27 GHz! Fortunately, most applications have significantly lower harmonic levels so that sampling rates can be several times lower.

As a rule of thumb, signal components within [(n+1) (6dB)] of full scale are significant in an n-bit system. To digitize a 20MHz sine wave with a third harmonic at −54dB to 1/2 LSB accuracy and 8-bit resolution, 2(3(20MHz)) = 120MHz sampling rate is necessary.

FLASH A TO D CONVERTERS

A flash, or parallel, converter is composed of an array of parallel comparators, each representing one out of 2^n quantization levels. The analog signal is applied simultaneously to all of the comparator inputs as shown in Figure 2. The other input to each comparator is connected to a tap in a resistor divider network. The resistor network establishes reference voltages for each comparator.

The relationship between the number of comparator cells and the number of bits to be digitized is as follows:

4-bits	=	16 comparator cells
6-bits	=	64 comparator cells
8-bits	=	256 comparator cells
10-bits	=	1024 comparator cells

This technique provides a method for A to D conversion of signals in the tens of megahertz.

A technique used for high resolution A to D conversion is the two-stage approach, as illustrated in Figure 3. The most significant bits are developed by the first converter. These bits are fed to a D to A converter which develops a signal current equivalent to the value of these bits. This signal is then applied to an amplifier's summing node where it is nulled against the input signal (after correcting for propagation delay). Any remainder is amplified, then A to D converted by the second converter. This technique allows the use of 6 or 8-bit conveters to produce 10 to 12-bit (or more) conversions.

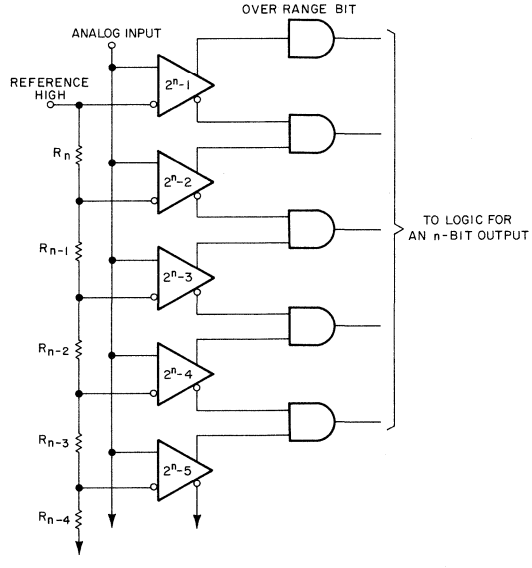

Figure 2: This is a simplified schematic of a flash A to D converter. The analog signal is applied to all of the comparator cells simultaneously allowing the entire conversion to be made at once.

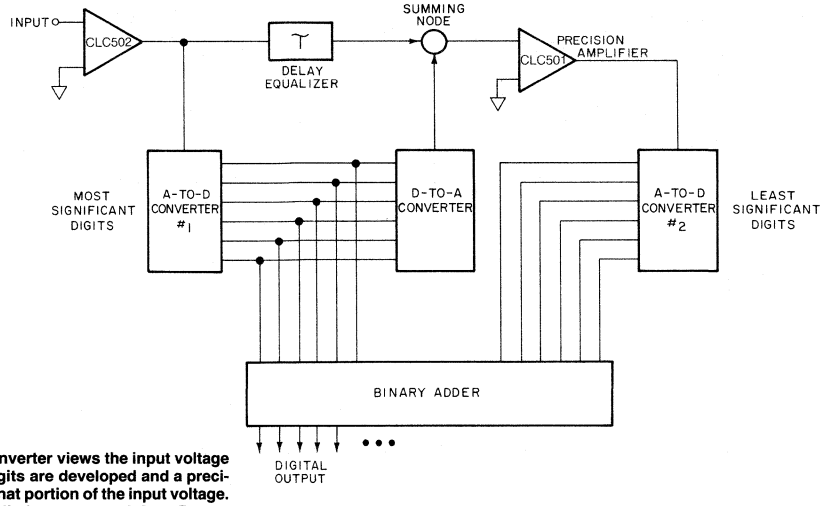

Figure 3: A two-stage flash A to D converter views the input voltage in two steps. The most significant digits are developed and a precision D to A converter is used to null that portion of the input voltage. The remainder is amplified and applied to a second A to D converter. The digitized results from both converters are combined in a binary adder to produce the final reading. The key is in the precision amplifier selected.

PRACTICAL CONSIDERATIONS

System Bandwidth

Some of the greatest challenges in high-speed A to D conversion involve the drive circuitry. Ideally, the analog signal path would have an overall bandwidth less than or equal to the Nyquist frequency (i.e. one-half of the sampling rate) to avoid aliasing problems. Due to a prior lack of commercially-available DC coupled amplifiers with sufficient high frequency performance, in many applications the amplifier has acted, by default, as the low pass (anti-aliasing) filter. To limit bandwidth, however, by selecting an imput amplifier with its rolloff point at or near the Nyquist frequency is a mistake. Phase becomes non-linear in most amplifiers at greater than one-third to one-half of the 3dB bandwidth. Group delay is, therefore, not constant and harmonics are delayed unequally. The net result is distortion, and degradation of the system's ability to accurately convert signals.

Thus, it is important to maintain amplifier bandwidth of at least three times the Nyquist rate to minimize gain and phase aberrations. Then, the anti-aliasing filter can be designed independently of the less precisely controlled transfer function poles of the amplifier and sample-hold. To attempt to do otherwise means that a custom filter must be designed for each samplehold and amplifier set.

Driving Capacitance

In a flash type converter, the input amplifier must drive a non-linear capacitance in parallel with a non-linear resistance. This non-linearity is due to the dramatic changes possible in the input impedance characteristics of the comparators, depending on whether they are in their on or off state. To minimize the consequences of changing capacitance, flash converter manufacturers recommend a fast settling, wide bandwidth, high slew rate, low output impedance driver. Comlinear amplifiers meet all of the these requirements.

Specifically, capacitance connected from the output of a closed-loop amplifier to ground can cause loop instability and even oscillation. The CLC409, however, remains stable even under these demanding circumstances. Experiments have shown that the circuit in Figure 4 will provide maximum bandwidth, flatness, and settling time when driving capacitances of up to 650pF.

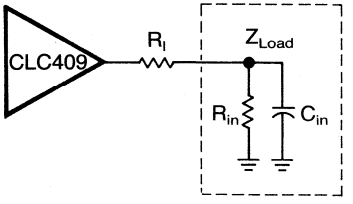

Figure 4: Experimental results indicate that this circuit offers the best bandwidth, flatness, and settling time for driving capacitive loads of up to 300pF in flash A to D converter applications.

R_1 serves to isolate the input capacitance, C_{in}, from the amplifier. This cuts down amplitude peaking. Although the optimum value of R_1 depends on converter parameters, the curve of Figure 5 gives a good first approximation. If $C_{in} = 50pF$, and R_1 value of 32Ω works very well.

As C_{in} gets larger, R_1 gets smaller to keep the RC pole at the highest possible frequency while maintaining peaking levels at less than 0.5dB. For example, when the amplifier drives 200pF, an R_1 value of 16Ω results in a -3dB bandwidth of 50MHz. Peaking is about 0.25dB, and settling time to 0.2% is about 15ns. Note that as R_1 decreases, overall gain increases.

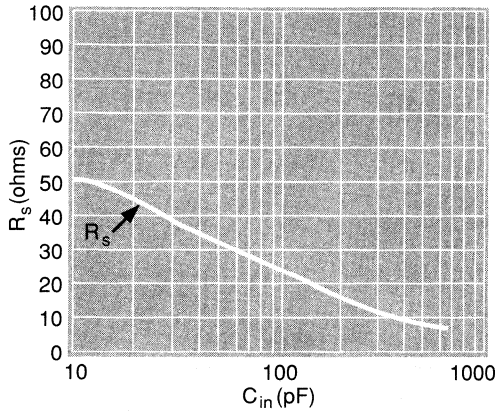

Figure 5: When the amplifier drives capacitive loads, resistor R_1 in Fig. 8 isolates it from the input capacitance, C_{in}. This curve will give a good first approximation for the value of R_1. The optimum value depends on several factors.

Settling Time

For A to D conversion of pulse waveforms, settling time of amplifiers and sample-holds is an important measure of waveform reproduction fidelity. These components must be able to settle to within one-half LSB of the correct value within the sample period allotted. Thus, for use with an 8-bit 100MHz flash A to D converter, settling to .2% within 10ns is necessary. This is a stringent requirement, but unless it is met the full capabilities of the flash A to D converter cannot be realized.

Slew Rate

Another consideration is the slew rate of the drive circuitry. The maximum slew rate for a sine wave is:

$dv/dt = 2\pi fA$ Volts/second

Therefore, to digitize a 5V peak sine wave at 20MHz, a slew rate of 630V/μs is needed. It is always a good idea to use an amplifier with much higher slew rate than that actually needed, because once an amplifier comes close to slew rate limiting, it becomes very non-linear and fails to settle properly.

Aperture Uncertainty

Ideally, digital conversion should occur at the center of the sampling window. However, noise can jitter the window aperture and create uncertainty as to its location in time. This causes uncertainty in the sample amplitude and is strongly dependent on signal slope, and hence on the frequency of the signal. So, while an A to D may have an impressive sample rate, unless its own aperture uncertainty (as well as that of the sample-hold) is low, the maximum frequency at which full n-bit accuracy can be obtained will decrease. For total aperture uncertainty of t, the maximum signal frequency that can be accurately digitized is $(3.14t2^{n+1})^{-1}$. Thus, for t = 20ps and n = 8, the maximum signal frequency is 31MHz.

This problem becomes severe when two high speed flash converters are combined in a two-stage converter which is designed to increase resolution. Not only does n become larger, maybe 10 to 12 in most cases, but t increases by at least a factor of two due to increased complexity. For example: two 6-bit flash A to D's which are capable of 100MHz sampling are to be used in such a system to give 10 bits of resolution, with t = 40ps. This limits the signal frequency to 3.9MHz if 10-bit accuracy is also required. If a 20MHz signal were to be digitized with this system, the result would have 10 bits of resolution but only 7.6 bits of accuracy. Note, however, that this is adequate for most applications, because resolution is usually of greater importance. This example illustrates why amplifiers and sample-holds with only 8 bits of accuracy work well in these systems.

Comparator Uncertainty

In parallel converters, comparator uncertainty may also become a limiting factor. An 8-bit converter capable of digitizing 2V must divide the voltage into 256 levels or 7.8mV per level. Given the typical comparator uncertainty of $\pm$2mV, this represents an uncertainty of 25%. The problem of comparator uncertainty becomes even more severe as resolution increases.

CONCLUSION

The need for higher speed analog-to-digital conversion is being answered by flash conversion techniques. However, these techniques have some critical considerations that must be understood and addressed if a successful converter is to be implemented. Many of these considerations relate back to the drive amplifier, making it a critical component in flash A to D applications. Due to their bandwidth, speed, and drive capabilities, Comlinear amplifiers are ideal for most flash converter applications.

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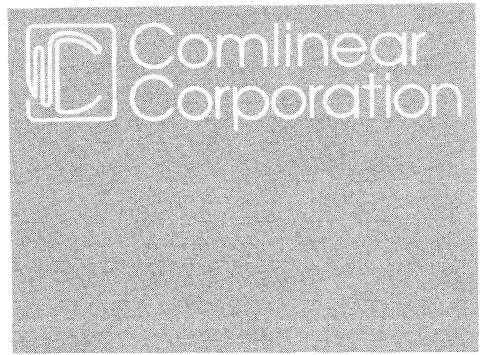


Designing with High-Speed Analog-to-Digital Converters

By: Mark Sauerwald

Introduction

State-of-the-art A/D converters push the very limits of performance by definition. This level of performance generally comes at a price: power dissipation, physical size, cost, etc. Balancing this situation is the fact that most systems are limited by the performance of lesser converters, and employing the very best converter is generally necessary to get the best overall system performance. By squeezing every last bit of performance out of a converter, the system specifications can be enhanced and great savings may be possible.

This guide to designing with high-performance A/D converters, should help to ensure that every design will "be all that it can be". This application note is split into several sections, many of these sections are built upon the others. Accordingly, the application note should be read through rather than just focusing on specific sections that explain a particular issue.

Power Supplies, Grounding and Bypassing

Without proper grounds, an A/D converter is incapable of providing quality data. What therefore constitutes a 'good ground'? Unfortunately, this is a question whose answer is difficult to nail down, since it varies from system to system. Ideally, a single ground plane with 0Ω impedance, both AC and DC, back to a power supply would be used in every system. In reality there is a finite impedance, and since the ground currents vary, the ground potential varies as well. To keep these effects in check, both the impedance to ground, and ground current variations in the path from the A/D converter back to the power supply, must be kept to a minimum.

To minimize the ground impedance seen by the power supply return currents, generous amounts of copper between the A/D and the power supply are the answer. In the best of situations, a layer of the printed circuit board would be dedicated to power supply grounding. Which layer should be used? The outer layers will often provide a higher measure of shielding , and may be preferable. In any case, 2oz/ft^2 or greater copper weight should be considered to lower the low-frequency ground plane impedance and keep ground plane potentials to a minimum.

The designer has less control over the variation in ground currents. In general analog circuits have a near constant current drain with time, while digital circuits experience much more variation, as transistors move in and out of saturation. Selection of the logic family will have a significant impact. Best for the A/D is a logic family which employs non-saturating transistor designs such as ECL. Worst is CMOS, which only draws supply current during clock edges.

Given that digital switching transients are composed largely of high-frequency components, total ground plane copper weight will have little effect on the ground impedance seen by the transients. This is because high-frequency currents tend to travel only on the surface of conductors (skin-effect) and total surface area is more critical than total ground plane volume.

Be aware of your logic power requirements. Current surges can be decreased through extensive bypassing. Even though the digital logic may not need it, providing a bypass capacitor for every power pin will minimize interference from the digital circuits on the converter's power supply. Ceramic 0.1μF capacitors are recommended for each power pin in the system. Also, a larger electrolytic or tantalum capacitor (+5μF to +10μF) should be used on each of the power supply feeds on each printed circuit board in the system.

Since the impedance of an electrolytic or tantalum increases with increasing frequency above about 10kHz, large capacitors on the power supplies do not eliminate the need for the per-pin ceramic capacitors which are primarily there to reduce high frequency transients. Chip capacitors have several advantages over the through-hole variety. They are smaller, and can often be placed closer to the pin that they are trying to bypass. Since they have no leads, series inductance is lower.

Many of the undesirable effects seen on A/D converter boards containing significant amounts of digital circuitry can be avoided by employing "single point" grounding. At a minimum, the analog and the digital supply and return currents should take separate paths back to the power supply. See figures 1a and 1b for the right and wrong way to do this. In figure 1a, the time varying power and ground currents are multiplied by the trace impedance between the A/D and the power source, increasing the ground potential fluctuations seen by the converter. In figure 1b, the impedance of the common portion of the current paths is much smaller, minimizing the effect on the A/D.

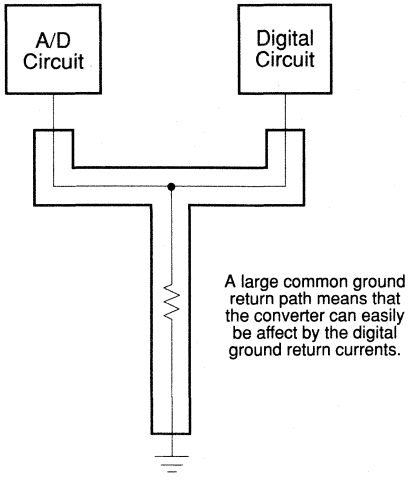


Figure 1a: Common ground Approach

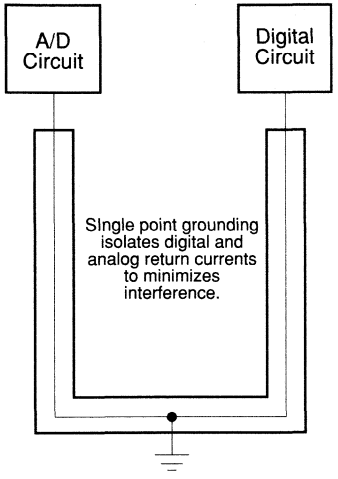


Figure 1b: Single-Point Grounding Approach

To further extend this method electrically, adding a series inductance in the path unique to the A/D converter's supply feeds will further isolate the digital supply's ability to corrupt the A/D converter's supplies. On Comlinear evaluation boards, a ferrite bead is used to this end. Since inductors limit surge currents, extra attention must be given to distributed supply decoupling to prevent "starving" high-speed circuits of supply current during switching.

On many boards where the A/D converter is forced to share its supplies with an appreciable amount of digital circuitry, separate ground planes are used for the digital and analog circuitry. In this situation, the digital ground plane should not extend beneath the A/D converter, the analog ground plane, or any other analog circuitry. Capacitive coupling between the typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to track down and fix.

Many A/D converters are capable of corrupting their own power supplies, if it is not adequately bypassed itself. A 5μF to 10μF tantalum or electrolytic capacitor should be placed within a couple of inches of the A/D converter, with 0.1μF ceramic chip capacitors placed as close as possible to each of the converter's power supply pins. Since chip capacitors are smaller than their leaded counterparts, they are easier to locate close to the supply pins, providing lower lead inductance.

Printed Circuit Board Layout

As mentioned in the section on power supplies and grounding, the board layout can have a profound effect on the A/D converter's performance. Besides power supplies and grounding, there are other ways in which the converter's performance can be affected by board layout. A key to good performance lies in getting "uncorrupted" clock and analog input signals to the A/D converter. If the clock line has noise on it, or is capacitively coupling to another signal, a slight non-periodicity can be introduced into the sampling process. As discussed in the section on clocks, this is not good, and a seemingly minor contamination of the clock can cause very undesirable effects.

Once the analog input signal has been sampled, clock jitter is not a major concern, special care is necessary only between the clock source to the A/D converter. This path should be as short as practical, and the clock line should be kept as far away from other signal traces as is reasonable, especially high-frequency traces. If the clock must cross over another trace, it should do so at a 90° angle to minimize coupling.

If the A/D requires a differential clock signal, the trace lengths of the two lines should be equal. If the two clock traces are not equal length, the edges of the convert command may arrive at the A/D at different times. This would increase, rather than cancel, the capacitive coupling of the clock to the analog input.

The analog input to the A/D converter requires the same attention. Running the trace to the analog input near to or parallel to digital traces will degrade the quality of the input signal during sampling. Try to avoid getting the analog input trace near any digital signals, if it must cross a digital path, try to make the crossing at 90°.

Use of a Balun for Impedance Control

When the converter is in a harsh environment, or at the end of a long transmission line, there may be an appreciable amount of common mode noise between the ground and input signal. Much of this common mode noise can be eliminated through the use of a balun (figure 2). A balun is a 1:1 transformer which forces equal currents in the signal and ground paths, forming a common mode choke. When a Balun is used, it will modify the frequency response of the system, adding insertion loss at both high and low frequencies. A balun such as the T2.5-6 from Mini-Circuits will allow for less than 0.2dB of loss for frequencies from 60kHz up to over 10MHz. Other transformers will have different frequency characteristics and should be selected after considering the application requirements.

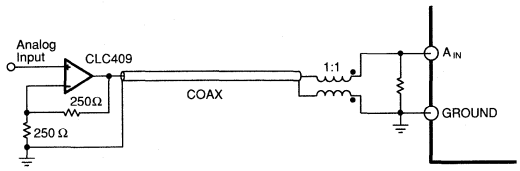


Figure 2: Balun Minimizes Common-Mode Noise

Analog Input Driving Circuits

Most hybrid A/D converters, and all of Comlinear's 12-bit converters, have their own internal buffers. In many cases no amplifier is required to drive the A/D converter analog input. If, however, there is need for an analog input driver circuit for gain or other signal conditioning, the CLC207 and CLC409 are very low distortion amplifiers (figure 3). Both have been optimized for high-gain applications, and can be configured for better than -80dBc harmonic suppression.

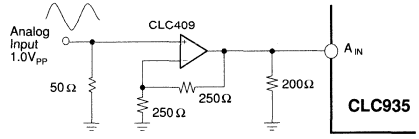


Figure 3: Analog Input Buffering

Digital Interface

If there is significant digital processing to be applied to the A/D output, it is suggested that a separate circuit board be used for the A/D so that the large number of digital signals do not degrade A/D's performance. If this is not practicable, then the following guidelines should be followed:

1) Use a non-saturating, low swing, logic family ... such as ECL. If ECL logic can be used, select the slowest possible TTL logic family; the slower edge rates will couple less effectively to the analog circuitry.

2) Make the system completely synchronous, using the same clock for the A/D converter and digital processing. A/D converters are most susceptible to interference in the middle of the conversion cycle, clock edges at this time are very undesirable.

3) Physically and electrically isolate the digital logic from the A/D converter and the analog circuitry as much as possible. Bypass power supplies that are in common both with capacitors to ground and series inductors as suggested in the section on power supplies.

4) Employ latches or buffers on the A/D converter digital outputs. This will prevent digital noise from entering and corrupting the conversion process through the outputs themselves. The performance of nearly all high performance A/D converters is degraded when driving high fanout loads or significant trace lengths.

Convert Clock Generation

All high-speed high-resolution A/D converters are sensitive to the convert clock quality. With a full scale 7MHz analog input signal, the slew rate at the 0V crossing is 14LSB/ns (for a $2V_{PP}$ analog input signal). An error (jitter) of as little as 35ps in the clock edge will yield a 0.5LSB error at the A/D converter output. This is as great or greater than any other error source likely to be present. This type of clock error or clock jitter is most easily seen in the form of poor SNR (signal-to-noise ratio). If the SNR is below expectations, clock jitter should be investigated.

$$SNR_{MAX} = 20Log \left[\frac{1}{2\pi f_{in} jitter_{RMS}} \right]$$

where ...

$$jitter_{RMS} = \sqrt{(\text{clock } jitter_{RMS})^2 + (\text{analog } jitter_{RMS})^2}$$

It should also be noted that jitter in the analog input source will have the same detrimental affect on SNR. Analog input signal jitter is usually only a problem in evaluation setups, and does not generally present a problem in full systems.

Low-jitter crystal controlled oscillators make the best convert clock sources. If the convert clock is generated from another type of source, by gating, dividing or other method, it should be registered by the original clock as the last step. This should keep jitter terms from compounding.

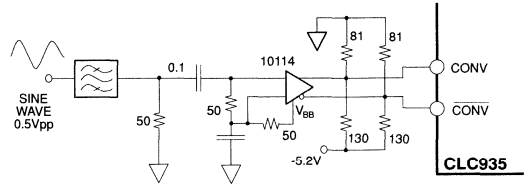


Figure 4: Sine to ECL Conversion Circuit

For variable frequency convert clocks, low-phase-noise frequency synthesizers like the Fluke 6080A or the HP8662 are good choices. Sinusoidal sources of this type will require a sine-to-ECL conversion circuit (figure 4), such as the one above. This circuit operates consistently with low level inputs (0dBm), but is sensitive to noise (jitter) from the synthesizer. By maintaining a larger input level (>+6dBm), the effects of jitter can be greatly minimized.

Thermal Considerations

Many high performance A/D converters dissipate an appreciable amount of power, up to 6W in some cases. The following strategies can be applied to prevent overheating:

a) ... a thick copper ground plane ... an appreciable amount of heat is conducted out of the A/D through its leads.

b) ... a copper stand-off between the ground plane and the bottom of the package (thermal paste may be useful).

c) ... a SIL PAD® between the ground plane and the bottom of the package . To maximize heat conduction leave a patch of exposed (no solder mask) ground plane under the A/D converter.

d) ... moving air over the A/D converter.

Evaluating a high performance A/D converter
Since the A/D converter is an expensive component, and one which can have a great effect upon the system performance. The best approach is to evaluate performance in the target system. This is not always feasible, and often clouds the line between converter and system quality. If the design is an upgrade of an existing design, try to modify the existing system, using an evaluation board to replace the old data converter.

If it is not practical to employ the final system as an evaluation platform, the converter should be operated under conditions as close as possible to those of the intended use. Match the clock rate; use input signals that are comparable in size and bandwidth to those in the final system.

If the system uses an 11MSPS clock, A/D performance with an 11MSPS clock may be better or worse than performance at the rated speed. Many manufacturers define the same specification differently, or test the parameter differently, it is therefore dangerous to try and make a comparison of two devices based on data sheet specifications alone. If in the application, the converter is sampling a signal with 5MHz bandwidth, a test of D.C. linearity will not be particularly illuminating. SNR or SFSR (or any other test pertinent to the final application) may be more relevant to the application. Comlinear applications engineers stand ready to assist you in evaluating Comlinear or competitive A/D converters.

A/D Converter Specifications
As the speeds and resolutions of A/D converters have increased, A/D converters have found themselves in applications that once were entirely analog. In an attempt to make the transition from analog to digital easier for the design engineer, Comlinear specifies many parameters in ways that are similar to those of analog components intended for the same systems. Unfortunately since there is not a direct equivalence between the A/D and the analog function that it is replacing, the specifications do not have the same meaning as similarly named specifications for analog components. What follows is a listing of several of the parameters that are used in many A/D converter specification sheets, along with the definitions that Comlinear uses.

Small Signal Bandwidth
In testing small signal bandwidth, the input is a sinusoid with a peak-to-peak amplitude of +FS (one half of the Full-Scale range for a bipolar input converter). The input frequency of a sinusoid is raised until the amplitude represented by the digital output signal is 3dB lower than the input. This is the small signal bandwidth. In most systems other factors make conversion at such high analog input frequencies impractical. Distortion usually begins to dominate at frequencies well below the small signal bandwidth.

Large Signal Bandwidth
Same as small signal bandwidth, but this time the input sinusoid is at full power. Once again, other undesirable signal degradations will usually prevent the user from operating the A/D with input signals of this high frequency.

Effective aperture delay
There is a finite period of time between the edge (Comlinear converters begin the sampling process on the rising edge of the convert signal) of the convert signal and the instant at which the converter actually samples the input signal. This time is known as the effective aperture delay. To measure effective aperture delay, the converter samples a pulse input signal at the same frequency of the conversion process. The phase of the convert clock is adjusted so that the value on the output of the A/D represents the level at the 50% point of the edge of the input pulse. The time difference between the clock edge and the A/D input edge is then the effective aperture delay.

Aperture Jitter
The RMS deviation of effective aperture delay is known as aperture jitter. Since this clock jitter multiplied by the RMS slew rate of the input signal generates an output error, the value of the aperture jitter can be estimated by observing how the SNR decreases as a function of increasing input frequency.

DNL
Differential Non-Linearity is a measure of the uniformity of the code steps. To measure DNL, the threshold voltages of the A/D converter are measured, where the differences between adjacent thresholds is compared to the ideal size of the codes. The worst case error of the 4095 codes is the DNL.

INL
Integral Non-Linearity measures the worst case error that the converter can make. Since an ideal A/D converter will make errors of up to +LSB, this portion of the error is not counted in the INL measurement.

FREQUENCY DOMAIN SPECIFICATIONS
Several high-speed A/D converter specifications are more appropriate to frequency domain applications. In these, the A/D converter input is a pure sinusoidal signal. A record of the A/D output is taken and is then transformed into the frequency domain by use of a Fourier transform (figure 5). The Fourier transform is then examined to determine the values of SNR, THD, IBH, SINAD, and SFSR.

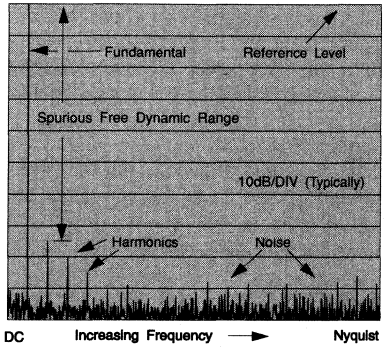


Figure 5: Typical Spectral Plot in the Frequency Domain

SNR - [Σ of the Noise (less Harmonics) : Fundamental] Signal-to-Noise Ratio is a measure of the broad band noise that is introduced into the signal by the A/D converter and the sampling process. The magnitude of the input sinusoid is compared to the sum of all other frequencies, except for those representing harmonics of the fundamental frequency. The ratio of the signal to the sum of the individual noise components is the SNR.

THD - [Σ Harmonics (10 to 50 Harmonics) : Fundamental] Total-Harmonic-Distortion is measured in a similar fashion to SNR, except that in the analysis, the fundamental is compared to the sum of the harmonics. Since some of the harmonics lie outside the dc to $F_S/2$ range, they will the aliased back into the base band.

IBH - [Largest Harmonic component : Fundamental] IBH is the ratio of the fundamental to the largest harmonic.

SINAD - [Σ of the noise and Harmonics : Fundamental] SINAD is similar to SNR except that the harmonics are not ignored.

SFSR - [Largest Harmonic or Noise component : Fundamental] SFSR is the ratio of the fundamental to the highest spur (noise or harmonic) in the frequency domain. This is very similar to IBH since the highest spur is usually harmonically related to the input.

Two Tone Intermodulation Distortion -
[Largest Harmonic or IMD component : Fundamental] The input to the A/D Converter consists of the sum of two sinusoids with a small difference in their frequencies. As an example, a converter with a 15MSPS clock might be tested with inputs at 5.1MHz and 5.2MHz. Non linearities in the converter will cause the input frequencies and their harmonics to mix, generating products at the frequencies Nf_1+Mf_2 where N and M are integers and f_1 and f_2 are the input frequencies. Many of these products will lie outside the dc to $f_S/2$ band, but their images will alias back into the baseband. The two tone I.M.D. is the ratio of the input signal to the largest of these unwanted products.

NPR - *Depth of notch in an "all hostile" noise environment* Noise Power Ratio is determined by providing the A/D converter with a "band limited" white noise input signal, with a narrow range of the spectrum removed from the input (this is the "all frequencies hostile" except the notch). The ratio of the power level in the spectrum to that in the notch, is the NPR (see figure 6). NPR is a useful specification for systems in which the input comprises several independent signals separated in the frequency domain. The NPR will predict how much adjacent channels will interfere with each other.

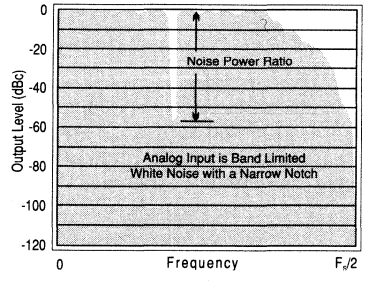


Figure 6: Typical Noise Power Ration Spectrum

Evaluation Boards
An evaluation board available for all of Comlinear's A/D converters. The evaluation board can be used to quickly evaluate the performance of these converters, saving time and effort. Use of the evaluation board, as a proven circuit layout, is highly recommended.

Applications Support
Comlinear Corporation maintains a staff of applications engineers who are available for design and applications assistance. They can be reached at (303) 226 0500.

Mini-Circuits P.O. Box 350166, Brooklyn, New York 11235. Phone: (718) 934 4500

SIL-PADs are manufactured by
BERGQUIST 5300 Edina Industrial Blvd. Minneapolis, MN 55435 Phone: (612) 835 2322

Application Note OA-07

Current-Feedback Op Amp Applications Circuit Guide

Scott Evans

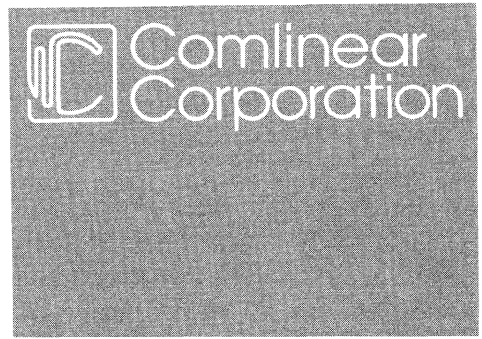


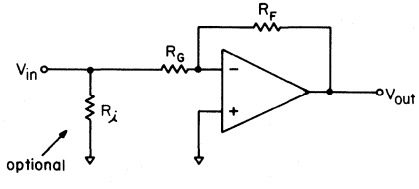
TABLE OF CONTENTS

INTRODUCTION

No two high-speed applications are the same—or at least it seems that way. Nonetheless, while every system has its particular requirements, many of the design techniques are common among different designs. This application note illustrates design techniques utilizing current-feedback op amps and the practical circuits where they are used. The circuits should work well with any Comlinear op amp if appropriate adjustments are made for different feedback resistance values.

Inverting Gain

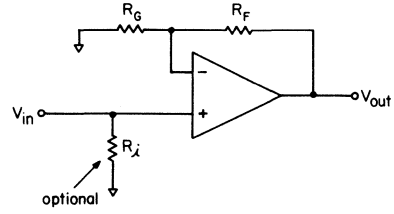
As with voltage-feedback op amps, the ratio of the feedback resistor to the gain-setting resistor determines the voltage gain in current-feedback op amp circuits. With current feedback, however, dynamic performance is largely independent of the voltage gain. (See application note AN300-1 for a technical discussion of current-feedback.) Also, the optimum feedback resistor value for a current-feedback op amp is indicated in the data sheet.



$$V_{out} = -\frac{R_F}{R_G} V_{in}$$

For in input impedance of 50Ω, select $R_i \| R_G = 50\Omega$.

Non-Inverting Gain

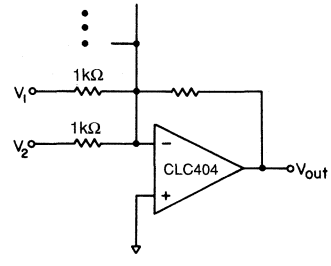


$$V_{out} = \left(1 + \frac{R_F}{R_G}\right) V_{in}$$

R_i sets the input impedance.

Summing Amplifier

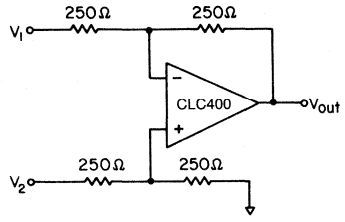
Current-feedback op amps are the natural choice in summing applications since the bandwidth and other key specs are relatively unaffected by high gain settings. (The parallel combination of all the input resistors yields a small effective gain-setting resistance and hence a large effective gain setting.)



$$V_{out} = -(V_1 + V_2 \ldots)$$

Differential Amplifier

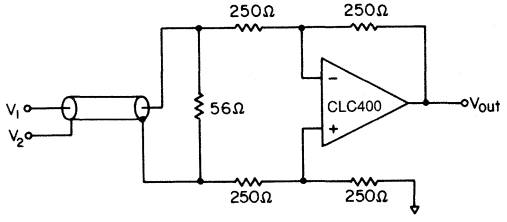
Be sure to obey common-mode input voltage limits shown in the op amp data sheet. If large, saturating input signals are expected, use an overdrive-protected op amp and appropriate protection circuitry.



$V_{out} = V_2 - V_1$

Differential Line Receiver

This circuit provides good common mode rejection and 50Ω termination for signals which need to be transmitted through coaxial lines.

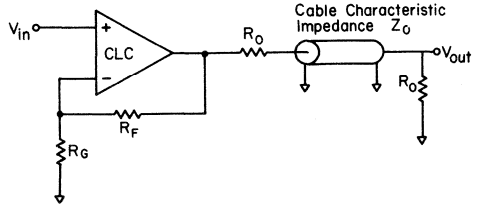


$V_{out} = V_2 - V_1$

Differential input resistance is 50Ω.

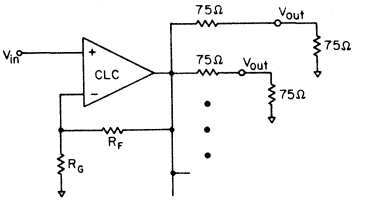
Coaxial Cable Driver

Proper transmission line driving techniques are important when high-speed signals have to travel more than a few inches. The back-matching and terminating resistors, R_o, are chosen to match the characteristic impedance of the coaxial line. If the load is well-matched to the transmission line impedance, the back-matching resistor may be omitted for greater voltage swing. (Remember that back matching creates a voltage divider which attenuates the output signal by 50%.)



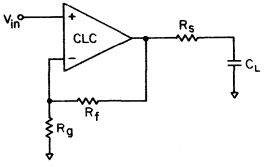
$R_O = |Z_O|$

Distribution Amplifier



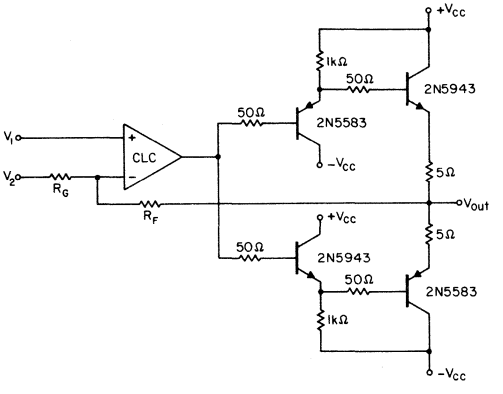
Driving Capacitive Loads

The damping resistor, R_s, reduces pulse-response overshoot and frequency-response peaking caused by the load capacitance. The value of R_s may be found on some of the op amp data sheets or may be found experimentally.



Output Current Booster

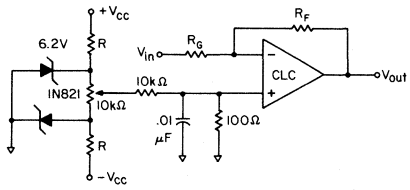
This circuit provides up to 400mA of output current. Since the output buffer circuit introduces additional phase lag, the feedback resistor, R_f, may have to be increased above the data sheet recommendation to decrease loop gain and thus improve stability. The gain-setting resistor, R_g, is then chosen for the desired gain.



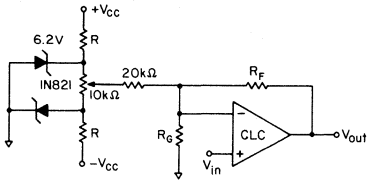
$$V_{out} = V_1\left(1+\frac{R_f}{R_g}\right) - V_2\left(\frac{R_f}{R_g}\right)$$

Simple Offset Adjustment

The Zener diode biasing resistor, R, should be chosen to provide a diode current of 7.5mA.



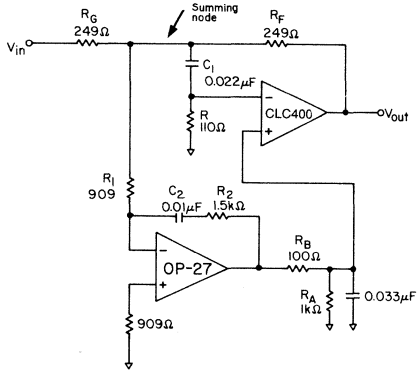
Inverting



Non-Inverting

Composite Amplifier for Low Offset and Drift (#1)

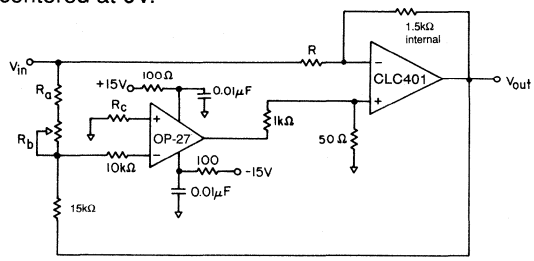
This composite circuit provides both high speed and good DC performance and unlike most composite circuits, it provides good settling performance (17ns to 0.1%). In operation, the OP-27 op amp drives its output such that the summing node is driven to 0V (which is the normal case for an inverting gain circuit). Thus, the circuit output takes on the high-performance DC characteristics of the OP-27. At high frequencies, the high-speed op amp takes over to provide good AC performance.



Select
$R_2C_2 = 15\mu s$
$R_1C_2 = 9.09\mu s$
$R = R_F \parallel R_G \parallel R_1$
$RC_1 = 2.5\mu s$

Composite Amplifier for Low Offset and Drift (#2)

This composite circuit is useful with those products which have the feedback resistor connected internally to both the input and output. R_b is adjusted for minimum output voltage at the OP-27 when V_{out} is a 70kHZ square wave of $10V_{pp}$ centered at 0V.

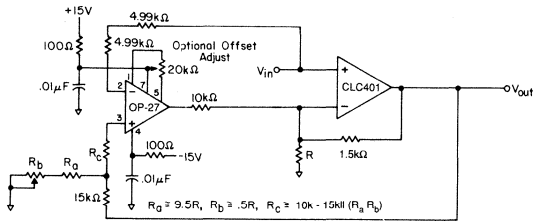


$$V_{out} = -\left(\frac{1500}{R}\right) V_{in}$$

$R_a \cong 9.5R$
$R_b \cong 0.5R$
$R_c \cong 10K + 15K \parallel (R_a + R_b)$

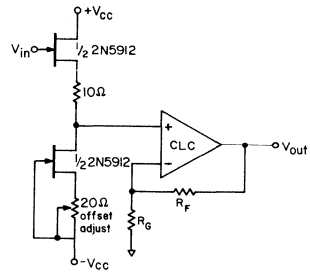
Non-Inverting Composite Amplifier

As with the previous circuit, R_b is chosen for minimum output voltage at the OP-27 when V_{out} is a 70kHz square wave of $10V_{pp}$ centered at 0V.



FET-Input Circuit

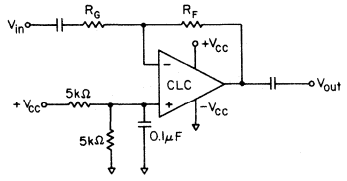
A FET-input circuit is useful when a greater input impedance is desired or when bias currents or noise currents need to be reduced.



$$V_{out} = V_{in}\left(1 + \frac{R_f}{R_g}\right)$$

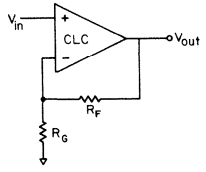
AC-coupled Amplifier (with Single-Supply Biasing)

The voltage divider circuit at the non-inverting input biases the op amp input and output at the supply midpoint. For those op amps having a bias pin, these pins should also connect to the supply midpoint bias circuit.



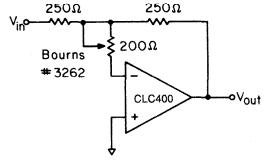
Reducing Bandwidth

Bandwidth and loop stability is controlled by R_f. Increasing R_f reduces bandwidth according to the approximate relationship: $\frac{BW_2}{BW_1} \cong \frac{R_{f1}}{R_{f2}}$



Adjustable Bandwidth

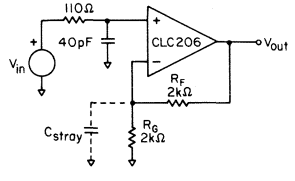
By increasing the inverting input impedance (which is normally very low) of a current feedback op amp, the bandwidth of the op amp can be reduced. The bandwidth of the circuit below can be varied over a range of 60MHz to 160MHz.



Reducing Frequency-Response Peaking

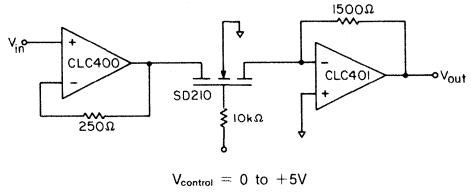
(due to stray capacitance in parallel with R_g)

The low-pass filter at the non-inverting input cancels the frequency-response zero caused by C_{stray}. At low non-inverting gains, the CLC231 or CLC400 will provide a flatter frequency response without the need for the low-pass filter (because they can be used with lower feedback resistor values).



Adjustable Gain Using a FET

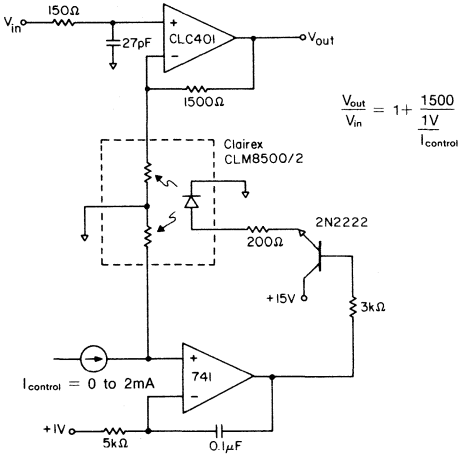
This circuit provides a 26dB adjustment range and a gain flatness of 1dB from DC to 50MHz. An SD210 FET provides low on-resistance with minimal capacitive loading.



$V_{control}$ = 0 to +5V

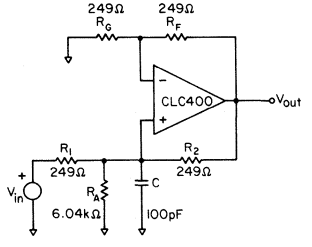
Adjustable Gain Using a Photoresistor

This circuit provides a 12dB adjustment range and a gain flatness of 1dB from DC to 20MHz. The 741 circuit improves temperature stability and repeatability of the photoresistor circuit.



Integrator (#1)

With current-feedback op amps, it is important to keep large capacitance values out of the inverting feedback loop in order to maintain stability.



For stable operation,

$\frac{R_2}{R_1 \parallel R_A} \geq \frac{R_F}{R_G}$

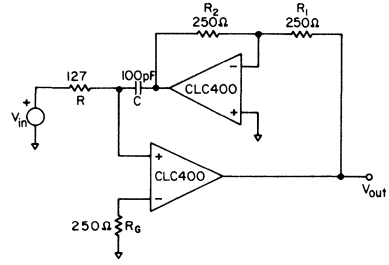
All resistors are 1%

$V_{out} \cong V_{in} \frac{1 + \frac{R_F}{R_G}}{sR_1C}$

$V_{out} \cong V_{in} \frac{2\pi\,(12.8MHz)}{s}$

Integrator (#2)

This integrator provides higher dc gain than #1. For the values shown, the dc gain is 55dB. Higher values can be obtained by reducing R_g, however, the ratio of R_g to R_1 should remain constant for adequate loop stability. Much of the output noise is directly proportional to R_1 so that higher dc gain is obtained at the expense of higher noise. This circuit does not have the stability problem that is related to resistor matching as does integrator #1.

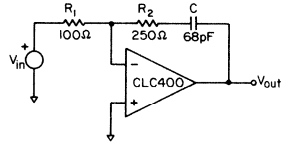


$$V_{out} = V_{in}\,\frac{\frac{R_2}{R_1}}{sRC}$$

$$\cong V_{in}\,\frac{2\pi\,(12.7MHz)}{s}$$

Integrator with Zero

In this circuit, feedback capacitance is acceptable because the op amp relies upon the value of the feedback resistor for stability.



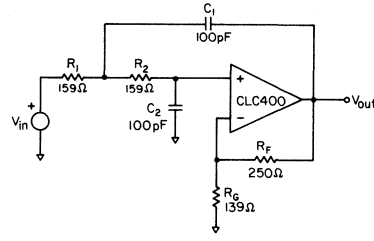
$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}\,\frac{s+\frac{1}{R_2C}}{s}$$

Active Filter Circuits

The following five circuits illustrate how current-feedback op amps provide high-performance active filter functions. The "KRC" realization is used (see references at the end of the ap note) since it doesn't require reactive elements in the (negative) feedback path, which would compromise stability.

When the filter cutoff frequency is small relative to the amplifier bandwidth, the transfer functions shown will provide good accuracy. However, as with any active filter circuit, the group delay through the op amp becomes significant for cutoff frequencies greater than about 10% of the op amp bandwidth. For such designs, computer analysis tools and an iterative design approach is helpful.

Low-Pass Filter (10MHz, Q = 5)



$$\frac{V_{out}}{V_{in}} = \frac{\frac{K_o}{R_1R_2C_1C_2}}{s^2 + s\left[\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1-K_o}{R_2C_1}\right] + \frac{1}{R_1R_2C_1C_2}}$$

$$K_o = 1 + \frac{R_F}{R_G} \qquad \omega_o^2 = \frac{1}{R_1R_2C_1C_2}$$

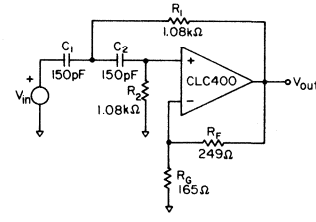
$$Q = \frac{1}{\sqrt{\frac{R_2C_2}{R_1C_1}} + \sqrt{\frac{R_1C_2}{R_2C_1}} + (1-K_o)\sqrt{\frac{R_1C_1}{R_2C_2}}}$$

$R_1 = R_2 = R,\ C_1 = C_2 = C$:

$$\omega_o = \frac{1}{RC}$$

$$Q = \frac{1}{3 - K_o}$$

High-Pass Filter (1MHz, Q = 2)



$$\frac{V_{out}}{V_{in}} = \frac{K_o s^2}{s^2 + s\left[\frac{1}{R_2}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) + \frac{1-K_o}{R_1C_1}\right] + \frac{1}{R_1R_2C_1C_2}}$$

$$K_o = 1 + \frac{R_F}{R_G} \qquad \omega_o^2 = \frac{1}{R_1R_2C_1C_2}$$

$$Q = \frac{1}{\sqrt{\frac{R_1}{R_2}}\left(\sqrt{\frac{C_2}{C_1}} + \sqrt{\frac{C_1}{C_2}}\right) + \sqrt{\frac{R_2C_2}{R_1C_1}}\,(1-K_o)}$$

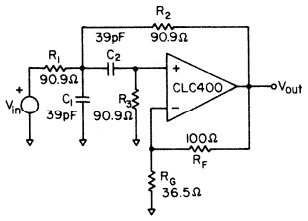
$R_1 = R_2 = R,\ C_1 = C_2 = C$:

$$\omega_o = \frac{1}{RC}$$

$$Q = \frac{1}{3 - K_o}$$

Band-Pass Filter (40MHz, Q = 4)

The component values shown are "predistorted" from the nominal design values to account for the 1.6ns op amp group delay, which is significant relative to the filter cutoff frequency.



$$\frac{V_{out}}{V_{in}} = \frac{s\frac{K_o}{R_1C_1}}{s^2 + s\left(\frac{1}{R_1C_1} + \frac{1}{R_3C_2} + \frac{1}{R_3C_1} + \frac{1-K_o}{R_2C_1}\right) + \frac{R_1 + R_2}{R_1R_2R_3C_1C_2}}$$

$$K_o = 1 + \frac{R_F}{R_G} \qquad \omega_o^2 = \frac{R_1 + R_2}{R_1R_2R_3C_1C_2}$$

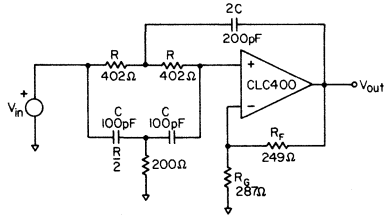
$$Q = \frac{\sqrt{\frac{R_2C_1(R_1 + R_2)}{R_1R_3C_2}}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_3}\left(1 + \frac{C_1}{C_2}\right) - K_o}$$

$R_1 = R_2 = R$, $C_1 = C_2 = C$:

$$\omega_o = \frac{\sqrt{2}}{RC}$$

$$Q = \frac{\sqrt{2}}{4 - K_o}$$

Band-Stop Filter (4MHz, Q = 4)



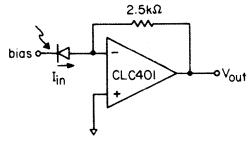
$$\frac{V_{out}}{V_{in}} = \frac{K_o\left(s^2 + \frac{1}{R^2C^2}\right)}{s^2 + 2\frac{s}{RC}(2 - K_o) + \frac{1}{R^2C^2}}$$

$$K_o = 1 + \frac{R_F}{R_G} \qquad \omega_{opole}^2 = \omega_{ozero}^2 = \frac{1}{R^2C^2}$$

$$Q_{pole} = \frac{1}{2(2 - K_o)}$$

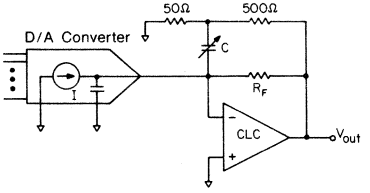
Photodiode Amplifier

The circuit below provides a transimpedance gain of −2.5kΩ to convert the photodiode current into a voltage.



D/A Converter Buffer Amplifier

Most high-speed, current-output D/A converters provide the best performance when driving little or no load impedance. The circuit below meets this requirement while also providing a transimpedance gain which converts the D/A output current into a voltage. The variable capacitor in the feedback loop should be adjusted for desired pulse response to compensate for the D/A output capacitance, which otherwise causes frequency-response peaking or instability. The 50Ω and 500Ω resistors reduce the effective value of the feedback capacitance so that a reasonable value capacitor may be used.

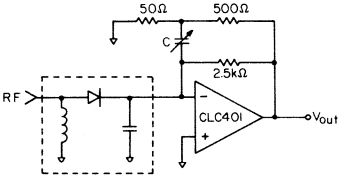


$$V_{out} = -IR_F$$

For example, with the CLC401, $R_F = 2.5k\Omega$ and a D/A output capacitance of 20pF, $C \cong 5pF$.

Tunnel Diode Detector Amplifier

See the D/A converter buffer circuit for circuit highlights.



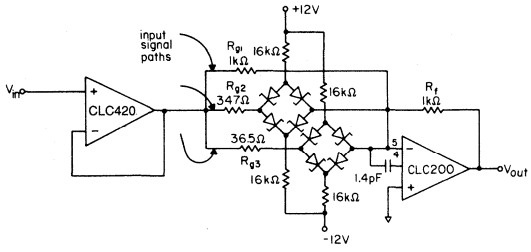
Non-Linear Transfer Functions

Current-feedback op amps are particularly useful in non-linear transfer function circuits. Since bandwidth and other key specifications are independent of gain-setting, the dynamic performance is relatively independent of signal level.

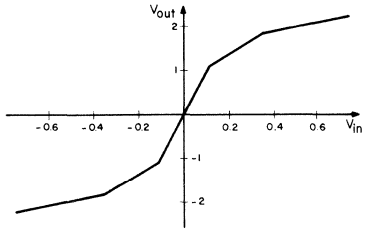
In analyzing the circuit, it is useful to identify the three input signal paths that contribute to the output voltage (the 1kΩ resistor and the two diode bridges). Each of these paths terminates at the inverting input—a point that is at virtual ground. Due to feedback, the current through the feedback resistor is equal to the sum of these input currents. The output voltage, therefore, is the product of the feedback resistor and the sum of the input currents.

The individual input currents are equal to the input voltage divided by the respective gain-setting resistor. However, in the signal paths containing the bridges, the current follows this linear relationship until it

limits at 12V/16kΩ. This is what leads to the non-linear gain. A more accurate analysis requires that the diode bulk and dynamic resistances be included.



Schottky bridges are Metelics

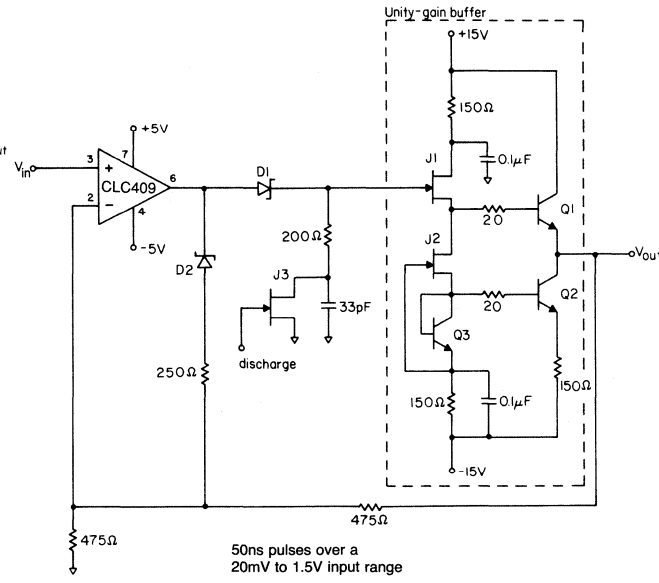


Peak Detector

The circuit shown in the next column can capture 50ns pulses over a 20mV to 1.5V input range. The circuit consists of three basic blocks: the op amp and diodes, the storage capacitor and discharge circuit, and the unity-gain buffer. The peak detecting action is caused by the conduction or non-conduction of the two diodes in the feedback loop.

When $V_{out} > V_{in}$, the op amp output swings in the negative direction until D2 conducts and the feedback path is completed and the op amp does not saturate.

When $V_{out} < V_{in}$, the op amp output swings in the positive direction causing D1 to conduct and the storage capacitor voltage to be charged through the 200Ω isolating resistor. This action continues until $V_{out} = V_{in}$ and equilibrium is established.



50ns pulses over a 20mV to 1.5V input range

D1,2	IN5711
Q1,2,3	MPS-H10
J1,2	2N5911
J3	2N4391

References:

A. Budak, *Passive and Active Network Analysis and Synthesis,* Houghton Mifflin Company, Boston, 1974.

IEEE Transactions on Circuits and Systems, Volume CAS-27, "Optimum Configurations for Single Amplifier Biquadratic Filters," number 12, pages 1155-1163, December 1980.

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Application Note OA-08

Differential Gain and Phase for Composite Video Systems

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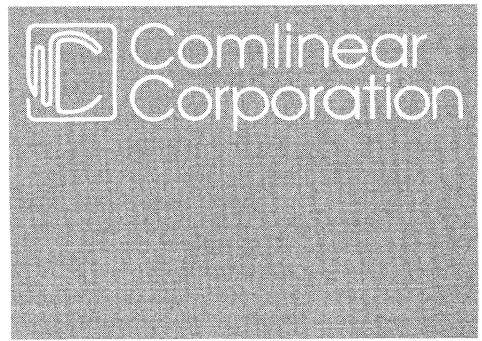


Differential Gain and Phase for Composite Video Systems

A critical performance characteristic for composite video systems relates to how well each device in the signal path maintains a constant small signal gain and phase for the relatively low level color carrier at 3.58MHz as the brightness (or luminance) signal is ramped through its allowed range. This is often specified as the differential gain and phase.

Figure 1 shows a typical composite video signal. The low frequency ramping shown in the test signal controls the brightness of the picture, while the 3.58MHz color carrier (or chrominance signal) riding on top of this controls the color. The amplitude of this carrier controls the color saturation while the phase shift of the carrier relative to the color burst sync. controls the hue. Any non-linearities in a device's gain or phase response as the luminance level is changed will show up as a distortion in the picture color. Note that the amplitudes shown on Figure 1 are those required at the load end of a doubly terminated 75Ω transmission line.

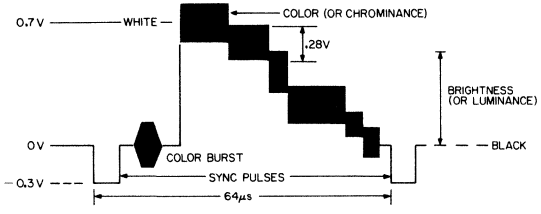


Figure 1

An amplifier's output DC level can have a profound effect on its small signal response. This is especially true for composite video signals when several parallel doubly terminated 75 ohm loads are driven from a single amplifier output causing the current to vary widely over the luminance range.

Differential gain can be defined as either the maximum percentage change in chrominance gain from the luminance black level to its white level or the peak-to-peak percentage gain change over the same luminance range. The peak-to-peak percentage gain change shall be used here.

Differential phase can be defined as either the maximum change in phase shift through a device, in degrees, from the luminance black level to its white level, or the peak-to-peak phase shift change over the same luminance range. The peak-to-peak change in degrees shall be used here.

Conceptually, the gain and phase response through an amplifier element at the chrominance frequency and amplitude is measured as the luminence, or output DC level, is ramped from its black level, typically 0 volts, to its white level, typically .7 volts. The peak-to-peak variation in the measured gain and phase is taken as the differential gain and phase of the device under test.

Although the perceptible level for differential gain and phase errors are well over the 1% and 1° levels, respectively, the cumulative errors of cascaded video channel devices are calling for individual amplifier errors to be well below the perceptible level. The traditional means of measuring differential gain and phase using a vector scope and/or waveform monitor allow measurements to be made down to approximately the .2% and .1° level. This level of resolution is inadequate for amplifiers intended for today's higher performance test and video distribution equipment. An alternative means of measuring this critical performance parameter using a network analyzer will be described.

Differential Gain and Phase Measurements Using a Network Analyzer

Using the self-calibration feature commonly available in network analyzers, exceptionally fine resolution of gain and phase changes from a reference trace can be determined. Figure 2 shows the overall test configuration used to measure several of the Comlinear amplifiers for differential gain and phase. Although a Hewlett-Packard 4195 spectrum/network analyzer was used to perform these measurements, as well as specific splitters, attenuators, and reflection/transmission test set, equivalent hardware configured to achieve the same result would, of course, be acceptable. The stand-alone programming capability of the HP4195, especially for the built-in DC bias source, make it particularly suitable for differential gain and phase testing. The 4195 has the capability of using the internal DC bias source as the independent variable for setting up its display trace, precisely the capability required for these tests.

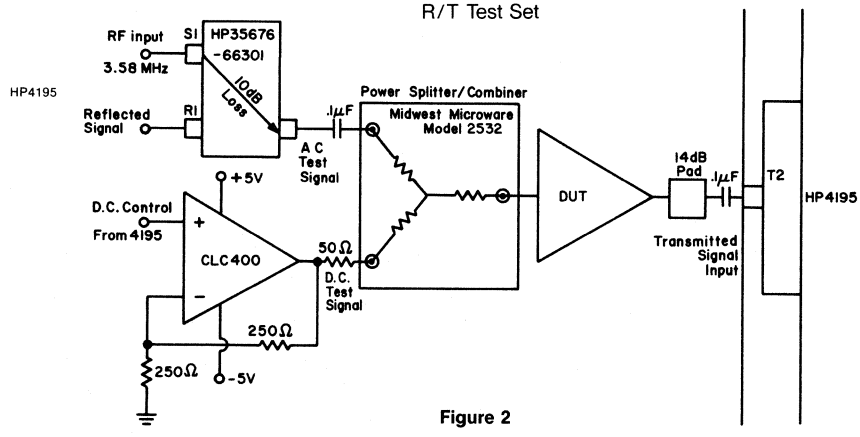


Figure 2

Figure 3 shows a typical configuration for the Device Under Test (DUT). The end goal for setting up the DUT stimulus is to generate at the output pin of the amplifier a 0 to 1.4V low-frequency ramp with a .56V_{pp} 3.58MHz sine wave riding on top of it. This will generate the amplitudes of Figure 1 at the load if we were driving a doubly terminated line. The peak-to-peak change in gain and phase for S21 measured over the DC input sweep, when corrected by a reference trace taken with the DUT replaced by a short, will yield a measure of the differential gain and phase.

Typical DUT Configuration

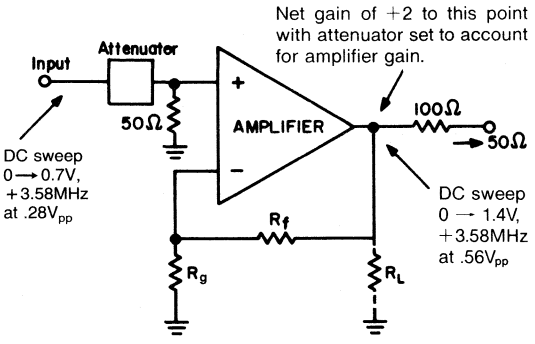


Figure 3

Note that although the test waveform of Figure 1 shows an entire luminance staircase sweep from white to black in less than 63μsecs, the 4195 will generate a considerably slower sweep to allow adequate S21 measurement time at each DC voltage setting. In doing the test this way, we are assuming that no additional device limitations will be encountered in increasing the luminance rate of change to that required by the most demanding video signals. This translates into a requirement for excellent amplifier pulse response which in turn implies adequate slew rate and broadband frequency response flatness (to limit pulse overshoot and ringing). An assessment of an amplifier's pulse response should be made independently to confirm that its response to slowly varying luminance levels is representative of that to the most rapidly varying signal.

Returning to Figure 2, each element of the test configuration will be described. Since we need to make a network analyzer measurement of a forward transmission characteristic, an S21 measurement, a reflected wave measurement must be made using a reflection/transmission test set. Many network analyzers have this built into their S-parameter test set. To minimize the reflected signal, a good 50Ω match is desired looking out of the R/T test set. Hence, the DC source and the DUT input are made to look like 50Ω on the other side of the power combiner. To minimize any receiver DC sensitivity, AC coupling is used to isolate the RF measurement paths.

The CLC400 is used to buffer the programmable DC source for two reasons. First, the source by itself does not have the current capability to drive the 100Ω load over the needed voltage range and, secondly, the CLC400 provides a more well-defined AC source impedance looking back into its output than the DC control output of the HP4195.

The power combiner provides a means of adding the desired AC and DC signals while maintaining a 50Ω matched environment. There is a 6dB loss for the AC signal through the splitter to the 50Ω DUT input impedance. With the AC coupling present at the 3.58MHz signal input to the splitter, there is, however, only a 3dB loss for the DC signal from the 4195 DC output pin to the 50Ω DUT input. Note that with the CLC400 buffer set up for a gain of 6dB, there is a net gain of 0dB from the CLC400 input to the splitter input and then a 3dB loss from there to the DUT input.

Turning now to Figure 3, the non-inverting input impedance is set to 50Ω to provide good matching to the power combiner output. For the low gain amplifier parts tested, the gain is set to +2 with $R_f = R_g$ and the input attenuator is not required. For the higher gain parts, operated at a linear gain of +20 (10x the low gain), a 20dB attenuator is used with the same DC sweep voltages and rf signal power to achieve the desired sweep at the output. The desired test voltage swings shown on Figure 3 at the output of the amplifier are double those shown on Figure 1 to account for the 6dB loss seen at the load in driving doubly terminated video transmission lines. The 100Ω series output resistor into the 50Ω 14dB attenuator provides the single load case of 150Ω while providing a good 50Ω source impedance to the network analyzer receiver input. Additional loading is simulated by connecting parallel 150Ω resistors to ground directly on the amplifier's output pin.

To make a differential gain and phase measurement for a particular part type, the DUT (including the 100Ω series output resistor, the input attenuator, and the 50Ω termination) is replaced by a short. Multiple DC voltage sweeps are then taken with the measured gain and phase averaged to develop a reference gain and phase flatness for the test configuration without the DUT in place. Replacing the DUT into the circuit and averaging multiple gain and phase measurements over the DC voltage sweep and subtracting the reference trace data from this will yield the gain and phase flatness for the device. Note that the absolute measured S21 will change going from the calibration to the DUT due to the 100Ω series output resistor. The absolute measured phase will also change due to the increased path length with the DUT in place. Except for non-linearities in the receiver, this won't matter since we are really only looking at the deviation from flatness for the corrected gain and phase measurements.

After performing the calibration, an example of which appears in Figure 4 with the gain shown in dB, a corrected measurement for the same short will yield a measure of the system resolution. This appears on Figure 5 and shows an approximate gain flatness resolution of .008% and a phase flatness resolution of .005°. These numbers result from taking twice the peak-to-peak variation shown in Figure 5 as an approximate measure of resolution. Note in Figure 4, the uncorrected calibration sweep, that while the gain appears fairly constant over the DC sweep, there is a relatively significant phase change of almost .02°. One possible source for this would be the slight change

in the impedance matching looking into the DC bias source out of the splitter, causing a slight change in the phase shift through the splitter. At any rate, using this data to correct the DUT measured data improves the resolution to the levels listed above. These resolution levels are considerably better than those achievable with a vector scope or a waveform monitor.

Uncorrected through Calibration

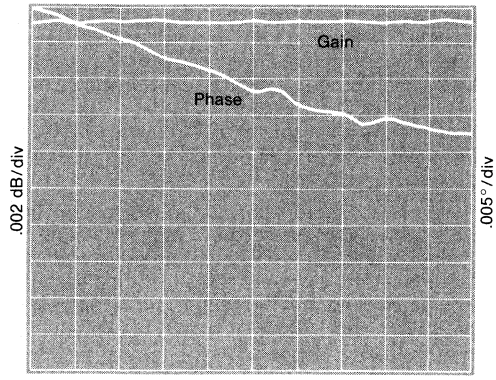


Figure 4

Corrected through Calibration

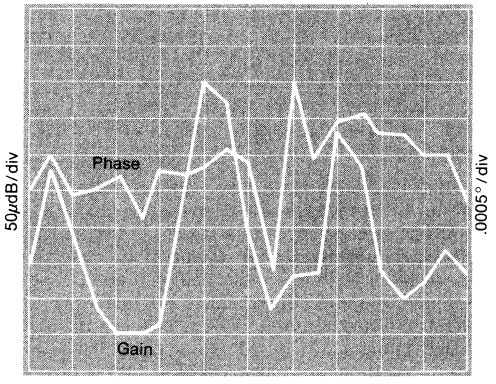
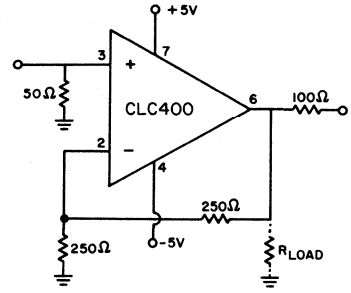


Figure 5

Measurement Results

Several amplifiers in Comlinear's product line seem particularly appropriate for composite video distribution. All of the products would actually show excellent differential gain and phase response at the 3.58MHz color carrier due to their exceptionally broad bandwidth and symmetric topologies. (Most devices utilize a Class AB output stage yielding excellent distortion relative to a Class A stage.)

The parts selected for testing included three low cost/size monolithic parts and a low gain hybrid amplifier. The DUT topologies used and the gain and phase plots vs. DC voltage for no additional loading attached (representing a single 150Ω load) are shown in Figures 6 through 10. The required stimulus levels for all of these tests, except the unity gain CLC110, was a DC sweep from 0 to .98V and an RF level = 7.8dBm. Both of these must be doubled to generate the desired output levels for the CLC110. The CLC400 DC buffer amplifier shown in Figure 2 will need to be run with +6V positive supply to accommodate the +4V output swing required for the CLC110 test. Although not shown on the DUT drawings, each test circuit included the recommended supply decoupling elements shown on that part's data sheet.



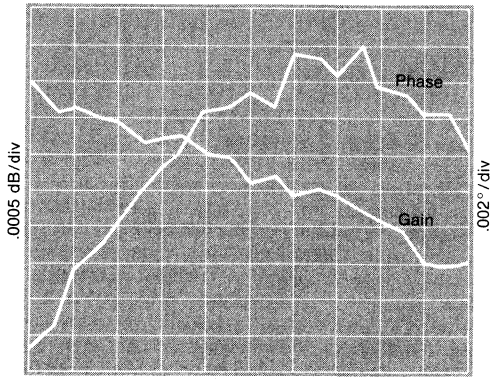
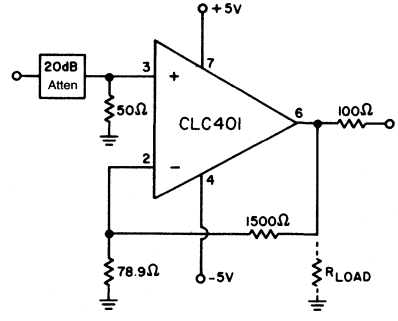


Figure 6

The CLC400, a monolithic amplifier optimized for low gain, showed the best overall differential gain and phase. With a single 150Ω load, the peak-to-peak gain variation was .03% while peak-to-peak phase variation was .02°. These are well above the system resolution levels but would present a considerable challenge measurement to a vector scope and/or a waveform monitor.



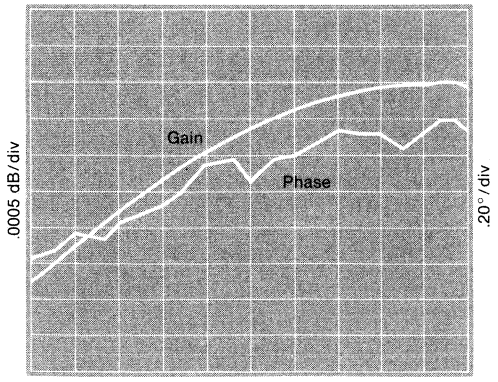
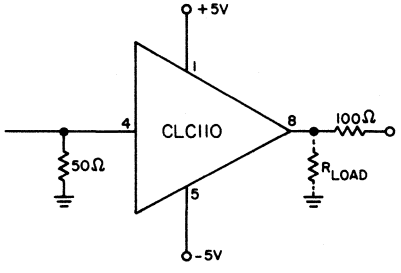


Figure 7

The CLC401 is a monolithic amplifier optimized for higher gains. Tested at a linear gain of +20, a 20dB attenuator is required to use the same stimulus levels into the DUT to produce the desired output swing. At a load of 150Ω, the peak-to-peak gain variation was .02% while peak-to-peak phase variation was .11°.



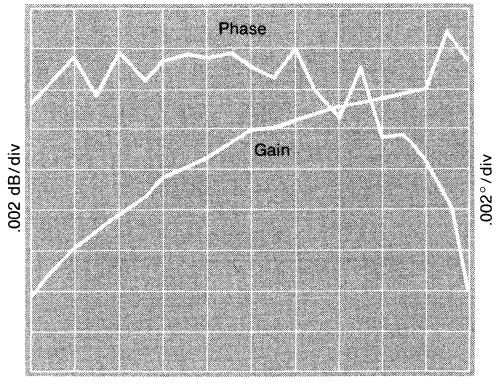
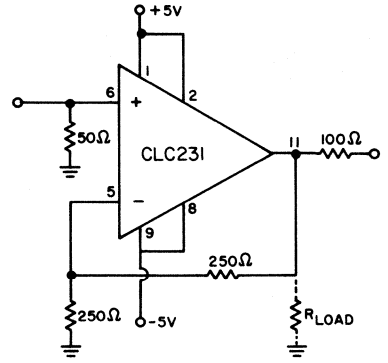


Figure 8

The CLC110 is a monolithic unity gain buffer with exceptional bandwidth and pulse response. The stimulus levels used for the CLC400 were doubled, both AC and DC, since this DUT has one-half the gain of the CLC400. With the nominal test load of 150Ω, the peak-to-peak gain variation was .17% while the peak-to-peak phase variation was .01°. Compared to the CLC400, this part offers better differential phase but poorer differential gain performance.



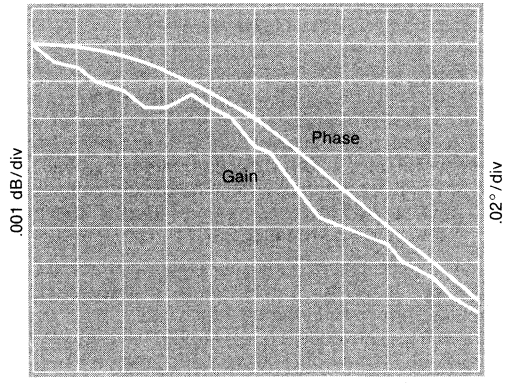
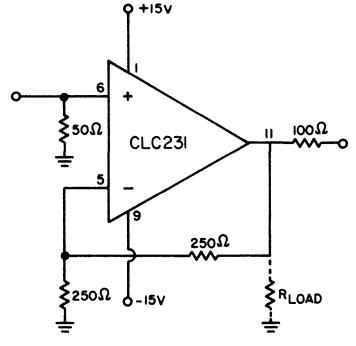


Figure 9

The CLC231 is a hybrid amplifier optimized for low gains. It also has the capability of operating at supplies down to ±5V with almost full AC performance if the two ladj pins are shorted to their respective supplies. The performance, however, is very poor relative to the CLC400. It was anticipated that the higher slew rate and output current capability of this hybrid part would enhance performance. It appears, however, that even in the single 150Ω case the differential gain is .09% while the differential phase is .14°.



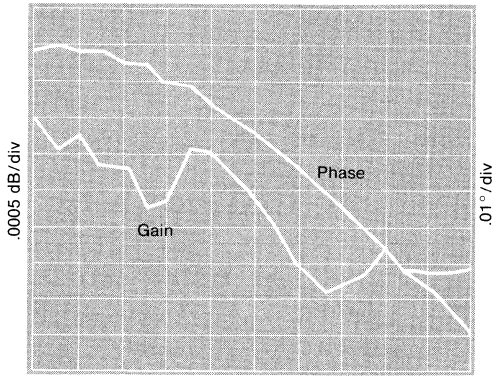


Figure 10

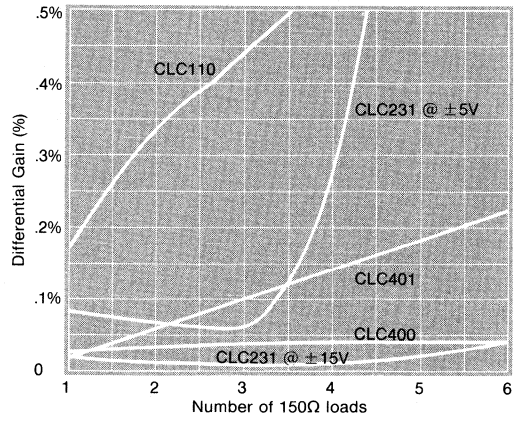


Figure 11

Operating the CLC231 at its recommended ±15V supplies, being careful to remove the shorts to the Iadj pins, yields excellent performance. At the nominal load of 150Ω, peak-to-peak gain variation was .03% and peak-to-peak phase variation was .08°. This compares very well to the CLC400 and may actually offer better performance for very high-speed luminance signals due to the higher slew rate offered by the CLC231.

All of the parts tested here offer slew rates in excess of 400V/μsec as well as excellent high-speed pulse fidelity. Increasing the luminance staircase rate to that used in actual composite video signals should have no effect on the differential gain and phase performance.

Figures 11 and 12 show the differential gain and phase vs. number of 150Ω loads for the five sets of tests performed here. Generally, for low gain applications, the CLC400 appears to yield the best overall performance for multiple loads. The CLC401 can be used successfully driving a limited number of loads in those cases where significant gain is required (as in receiving a signal on an exceptional length of cable). The CLC110 can offer some advantages in the differential phase performance if that is the key performance parameter. The CLC231 would be considered at ±15V supplies where multiple lossy lines need to be driven and the loss can be recovered by driving higher output levels at the CLC231 than achievable with the ±5V monolithic parts.

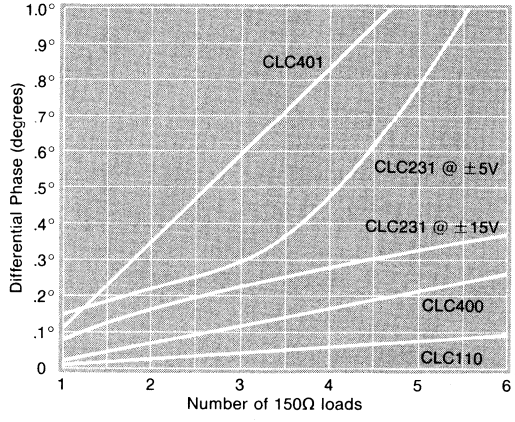


Figure 12

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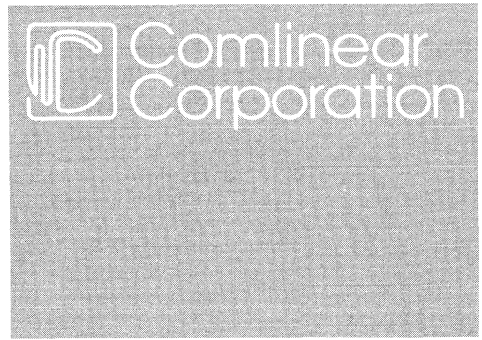
Application Note OA-12

Noise Analysis for Comlinear's Op Amps

Michael Steffes



Abstract: This application note develops the various descriptions of noise used by the industry and applies these terms to Comlinear's current feedback amplifier product line. In addition, a summary table of the equivalent input noise voltage and currents for the amplifiers available from Comlinear at the time of publication is also included (Appendix II). Finally, noise computational aids for analyzing the effect of 1/f noise and converting from small signal −3dB bandwidth to noise power bandwidth is included as Appendix I.

Understanding different descriptions of noise:
Probably the most perplexing aspect of noise analysis is the myriad of descriptions used by the industry for the same underlying phenomena. Different needs lead engineers into describing noise in many different ways. A few of these options are

1. Spot or integrated noise
2. Input or output referred noise
3. Noise powers or noise voltages and currents
4. Noise figure and/or noise temperature

Which form is used for each of these selections depends on what you are trying to accomplish. Spot noises are almost always used in calculating total noise since there is normally a common system bandwidth that will determine the integrated noise. Input noise is of interest for developing the input Signal/Noise ratio while output noise, especially integrated noise, is of interest when comparing the noise level to the ½ LSB of an A/D converter. Computations for developing equivalent noises considering multiple noise sources are always done by combining the powers and power gains, whereas the separate contributing noise sources are almost always defined in terms of currents and voltages. Noise figure and noise temperature are amplifier input noise descriptions common to the RF and communications field.

An example computational flow will illustrate how these various descriptions fit together. Taking the equivalent input spot noise voltages and currents as the starting point for any description of noise (see Figure 1), an equivalent output spot noise power may be computed by taking each voltage and current to the output through its appropriate gain and combining them as the sum of squared terms. Noise current terms always include an impedance in their gain expression to get all terms into squared voltage expressions. Strictly speaking, we should be developing these powers across some resistance. However, in all subsequent expressions the resistances drop out and we are left dealing with voltages, currents, and gains squared. In general, the separate noise sources are taken to be uncorrelated which is why we can combine them by simply adding their component powers. Having computed the total output noise power, the equivalent output spot noise voltage is obtained by taking the square root of this expression.

From this spot noise voltage at the output, all other noise descriptions may be derived. The integrated output noise voltage is obtained by multiplying the spot noise by the square root of the noise power bandwidth. (See Appendix I for a description of the Noise Power Bandwidth (NPB)). This yields an rms noise voltage at the output for that bandwidth. Taking this voltage times 6 will yield the approximate peak-to-peak voltage swing that would be seen on an oscilloscope for this NPB. Adjusting the scope bandwidth illustrates the importance of noise power bandwidth quite well.

Equivalent input spot noise voltages can be derived by taking this output spot noise voltage and dividing by the voltage gain (from whatever input point you wish to define) to the output. This is normally called input referring the output noise. Again, multiplying by the noise power bandwidth will yield the input referred integrated noise. This is normally left as an rms value (as opposed to a peak-to-peak noise). With an equivalent input noise voltage derived, the Noise Figure is developed by comparing this amplifier contributed noise to the source resistor noise.

In general, remember that computations combining noise sources together must be done with squared voltages, currents, and gains. Getting back to voltage or current is simply the square root of the sum of squared terms expression. Integrated noise is computed by multiplying noise power bandwidth (NPB) by the spot noise power (the sum of squared terms), or by multiplying the square root of the NPB by the noise voltages or currents.

Comlinear amplifier noise analysis:
For devices as flexible as Comlinear's current feedback op amps, one of the primary goals in specifying the noise is to do so in a fashion that provides enough information to predict the noise performance under any set of operating conditions. The best way to do this is to define an equivalent non-inverting input noise voltage and input noise currents for the non-inverting and inverting inputs. These are defined as spot noise voltages and currents over frequency, although in most applications, only the relatively constant high frequency (flatband) value is of any interest. These three terms form the most elemental of common denominators for the remaining types of noise descriptions. In any real measurement or application the resistors used to operate the amplifier correctly will also contribute noise. Although often neglected, these can make a significant noise contribution in some cases and must be considered for any complete noise analysis.

Figure 1

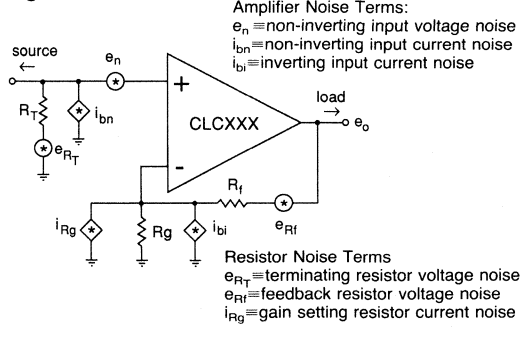
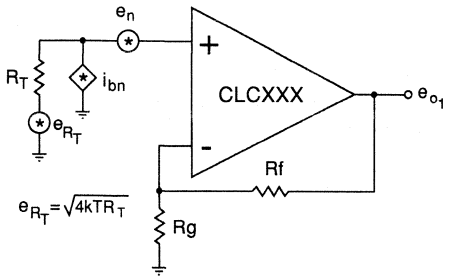


Figure 1 shows a non-inverting amplifier configuration with every noise source specified.

With all of the contributing noise sources defined, an output spot noise voltage may be found by using superposition for each of those sources. As with any other linear analysis, each noise source is considered separately by opening all other noise current sources and shorting all other noise voltage sources. Each source's contribution to the output noise is taken as the voltage squared generated by that source at the output. Figure 2a shows the contribution to the output of the noise sources appearing at the non-inverting input.



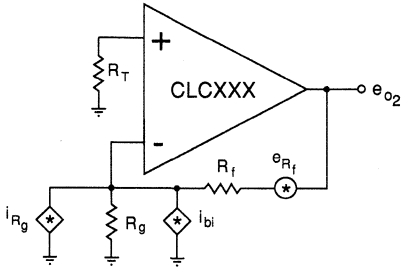
$$e_{o_1}^2=\left[e_n^2+(i_{bn}R_T)^2+4kTR_T\right]\left(1+\frac{R_f}{R_g}\right)^2$$

where
k≡Boltzman's constant = 1.38×10^{-23}J/°K
T≡°Kelvin
4kT = 16×10^{-21} Joules at T = 290°K

Figure 2a: Non-inverting noise sources

Note that we are assuming an infinite input impedance at the non-inverting node. This yields a gain of 1 to the non-inverting input for each voltage noise source and a gain of R_t for the non-inverting current noise. Each of these is squared and referred to the output by multiplying by the non-inverting voltage gain squared.

Figure 2b shows the output noise power contributions for the noise terms on the inverting side of the amplifier circuit.



with $i_{Rg}=\sqrt{\frac{4kT}{R_g}}$ and $e_{Rf}=\sqrt{4kTR_f}$

$$e_{o_2}^2=\left[(i_{bi}R_f)^2+(i_{Rg}R_f)^2+e_{Rf}^2\right]$$

$$\downarrow$$

$$=(i_{b_i}R_f)^2+\underbrace{\frac{4kTR_f^2}{R_g}+4kTR_f}$$

combined resistor noise power = $4kTR_f\left(1+\frac{R_f}{R_g}\right)$

then, $e_{o_2}^2=(i_{bi}R_f)^2+4kTR_f\left(1+\frac{R_f}{R_g}\right)$

Figure 2b: Inverting noise sources

With no signal at the non-inverting node, the inverting node is taken to be at 0 volts. We assume that the inverting input draws no current, (for current feedback amplifiers the loop gain drives it to 0 while for voltage feedback amplifiers the inverting node presents a high input impedance). With 0 volts across R_g, and no current into the inverting input, the two current noise sources must simply flow through R_f to appear at the output as voltages. Similarly, with 0 volts at the inverting node and no current path, the noise voltage of R_f appears as a voltage rise from zero to the output.

These two expressions for the component parts of the output noise power may now be combined for the total output noise power.

$$1+\frac{R_f}{R_g}\equiv A_V, \text{ non-inverting voltage gain}$$

Output noise power, e_o^2, is then:

$$e_o^2=e_{o_1}^2+e_{o_2}^2=\left[e_n^2+(i_{bn}R_T)^2+4kTR_T\right]A_v^2$$
$$+(i_{bi}R_f)^2+4KTR_fA_v$$

Output noise voltage is then:

$$e_o=\sqrt{e_{o_1}^2+e_{o_2}^2}=$$

$$e_o=\sqrt{\left[e_n^2+(i_{bn}R_T)^2+4kTR_T\right]A_v^2+(i_{bi}R_f)^2+4kTR_fA_v}$$

This yields a total output voltage noise per $\sqrt{Hz}$.

From this spot output noise voltage, all other descriptions of noise may be derived. The integrated output noise, or rms noise voltage in a given noise power bandwidth, can be derived by taking this spot output noise voltage times the square root of the noise power bandwidth (NPB). See Appendix I for an additional discussion of NPB.

Integrated output noise

$e_{o(rms)} = e_o \cdot \sqrt{NPB}$

peak-to-peak output noise voltage

$6 \cdot e_{o(rms)} = 6 \cdot e_o \cdot \sqrt{NPB}$

Having the rms output noise voltage, the peak-to-peak noise is taken to be 6 times this as a very conservative limit. (Reference 1, page 299)

The input spot noise is simply the output spot noise voltage divided by the voltage gain. If the input is defined to be at the non-inverting input we would divide by $A_v = 1 + R_f/R_g$.

Input spot noise voltage, e_n

$$e_n = \frac{e_o}{A_v} = \sqrt{e_n^2 + (i_{bn} R_T)^2 + 4kTR_T + \left(\frac{i_{bi} R_f}{A_v}\right)^2 + \frac{4kTR_f}{A_v}}$$

Again, this could be converted to both integrated and peak-to-peak swing as described for the output spot noise voltage. Note that since the final two terms under the radical contribute to the output noise independently of the desired signal gain, as that gain is increased, their impact on the equivalent input noise is reduced. In general, every measure of noise (except the separated component spot noise terms) is strongly dependent on the selection for the value of the feedback resistor and the desired signal gain setting. Thus, data sheet specifications for equivalent noise levels apply only for the test or specification setting used. Additionally, since the feedback resistor value plays such a large role in setting the frequency response for current feedback amplifiers, it cannot be set arbitrarily low to reduce the noise, and should be increased from its recommended value only while recognizing the impact this will have in the noise gain for the inverting current noise term.

The signal noise floor (SNF; specified in the data sheet specs) is simply the input spot noise voltage described as a power into 50 ohms referenced to 1mW. Basically, it is the input spot-noise voltage converted to dBm.

with, $e_{ni} \equiv$ equivalent input spot noise voltage

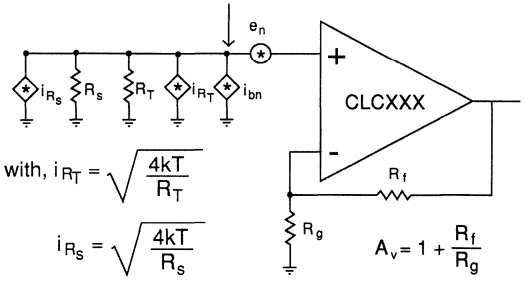
$$SNF = 10 \log \left[\frac{e_{ni}^2}{(50\Omega)\ (.001\ W)}\right] = 10 \log 20 + 20 \log e_{ni}$$

$SNF = (13.01 + 20 \log e_{ni})dBm$

The Noise Figure compares the power ratio of input signal/noise ratio to the output signal/noise ratio. One difference with the noise figure description is that the source resistor (R_s) must be included in the analysis. The input noise is taken as the noise power delivered to the input from the source resistor. The output noise is the total noise power at the output, including the source resistor noise, where gain for the non-inverting input noise current and terminating resistor noise include the presence of R_s. After manipulating the fundamental noise figure expression, it will reduce to $10 \cdot \log(1 + e_{ni}/e_s)$ where e_{ni} is the input noise power (including R_s in the gain for the current noise), but excluding its noise power, and e_s is the input noise power due to the source resistor and excluding all other sources (see Application Note OA-11 for a more complete analysis).

With an arbitrary R_T, Figure 3 shows how R_s will affect the calculation for the equivalent input noise power and what noise power the source resistor will deliver to the input. Comparing this to the earlier expression shows that the R_t and I_{bn} noise current gains are reduced by the parallel addition of R_s.

Input noise power definition point



e_{ni}^2 = input noise power excluding i_{R_s}

$$e_{ni}^2 = (i_{bn}^2 + i_{R_T}^2)\,(R_s \,||\, R_T)^2 + e_n^2 + \left(\frac{i_{bi} R_f}{A_v}\right)^2 + \frac{4kTR_f}{A_v}$$

substituting in for $i_{R_T}^2$

$$e_{ni}^2 = \left(i_{bn}^2 + \frac{4kT}{R_T}\right)(R_s \,||\, R_T) + e_n^2 + \left(\frac{i_{bi} R_f}{A_v}\right)^2 + \frac{4kTR_f}{A_v}$$

e_s^2 = input noise power delivered by the source resistor

$$e_s^2 = i_{R_s}^2 (R_s \,||\, R_T)^2 = \frac{4kT}{R_s}(R_s \,||\, R_T)^2$$

Figure 3

Taking these two expressions for the total input noise power due to the amplifier, e_{ni}, and the input noise power due to the source resistor, e_s, the noise figure expression may be developed.

$$NF = 10 \log \left(1 + \frac{e_{ni}}{e_s}\right)$$

$$NF = 10 \log \left[1 + \frac{\left(i_{bn}^2 + \frac{4kT}{R_T}\right)(R_T \,||\, R_s)^2 + e_{ni}^2 + \left(\frac{i_{bi} R_f}{A_v}\right)^2 + \frac{4kTR_f}{A_v}}{\frac{4kT}{R_s}(R_T \,||\, R_s)^2}\right]$$

Letting the input termination resistor, R_t, equal the source resistor (a very common situation where impedance matching is desired) simplifies this noise figure expression as follows:

with $R_T = R_s$, $R_T \,||\, R_s = \frac{R_s}{2}$ and

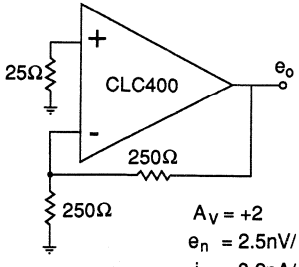
$$NF = 10 \log \left[1 + \frac{\left(i_{bn}\frac{R_s}{2}\right)^2 + kTR_s + e_n^2 + \left(\frac{i_{bi}R_f}{A_v}\right)^2 + \frac{4kTR_f}{A_v}}{kTR_s} \right]$$

$$NF = 10 \log \left[2 + \frac{\left(i_{bn}\frac{R_s}{2}\right)^2 + e_n^2 + \left(\frac{i_{bi}R_f}{A_v}\right)^2 + \frac{4kTR_f}{A_v}}{kTR_s} \right]$$

Conceptually, the 2 factor arises because we are taking a signal division by 2 at the input with a discrete (noisy) terminating resistor, while the remaining ratio is simply a comparison of the equivalent input noise power (excluding the source and terminating resistor noises) to the noise power delivered from the source resistor.

Example Calculations:
Let us now use the input spot noise terms for a pair of amplifiers (obtained from Appendix II) to develop each of these descriptions of noise.

Considering the CLC400 and CLC401 in their specifications test circuit:



$A_V = +2$
$e_n = 2.5nV/\sqrt{Hz}$
$i_{bn} = 3.2pA/\sqrt{Hz}$
$i_{bi} = 14pA/\sqrt{Hz}$

$$e_{o_1}^2 = \left[(2.5nV)^2 + [3.2pA(25\Omega)]^2 + (.63nV)^2\right] 2^2$$

$$e_{o_2}^2 = \left[[14pA(250\Omega)]^2 + 4kT(250\Omega)\,2\right]$$

$$e_o = \sqrt{e_{o_1}^2 + e_{o_2}^2} = \sqrt{(5.16nV)^2 + (4.5nV)^2}$$

$$e_o = 6.8nV/\sqrt{Hz}$$

Integrated output noise with NPB = 200MHz

$$e_o(rms) = 5.2nV\sqrt{200MHz} = 96.8\mu V_{rms}$$

Peak - Peak output noise voltage

$$e_o(p\text{-}p) = 6 \cdot 96.8\mu V_{rms} = .58mV$$

Input integrated noise

$$e_{ni}(rms) = \frac{e_o(rms)}{A_v} = \frac{73.5\mu V}{2} = 48.4\mu V$$

this agrees well with the data sheet typical spec. of $= 50\mu V$

Equivalent input spot noise voltage

$$e_{ni} = \frac{e_o}{A_v} = \frac{6.8nV/\sqrt{Hz}}{2} = 3.4nV/\sqrt{Hz}$$

Input Signal Noise Floor (1Hz Band)

SNF = 13.01 + 20log (e_{ni})
$= -156.4dBm$

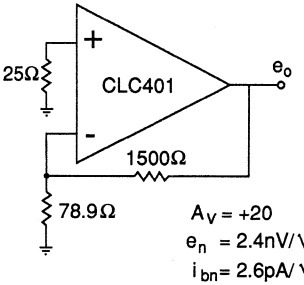
Approximately equal to the data sheet typical spec. of $-156dBm$

Integrated input Noise Floor is SNF + 10log(NPB)

Noise Figure with $R_s = R_t = 50\Omega$

$$NF = 10 \log \left[2 + \frac{[(3.2pA)25\,\Omega)]^2 + (2.5nV)^2 + \left[\frac{(14pA)\,(250\Omega)}{2}\right]^2 + \frac{4kT(250\,\Omega)}{2}}{kT(50\,\Omega)} \right]$$

NF = 17.7dB for the CLC400



$A_V = +20$
$e_n = 2.4nV/\sqrt{Hz}$
$i_{bn} = 2.6pA/\sqrt{Hz}$
$i_{bi} = 17pA/\sqrt{Hz}$

$$e_{o_1}^2 = \left[(2.4nV)^2 + [2.6pA(25\Omega)]^2 + 4kT(25\,\Omega)\right](20)^2$$

$$e_{o_2}^2 = \left[[17pA(1500\,\Omega)]^2 + 4kT(1500\,\Omega)\,20\right]$$

$$e_o = \sqrt{e_{o_1}^2 + e_{o_2}^2} = \sqrt{(49.7nV)^2 + (33.6nV)^2}$$

$$e_o = 60nV/\sqrt{Hz}$$

Integrated output noise with NPB = 150MHz

$e_o(rms) = 60nV\sqrt{150MHz} = .73mV_{rms}$

Peak - Peak output noise voltage

$e_o(p\text{-}p) = 6 \cdot 735\mu V_{rms} = 4.4mV$

Input integrated noise

$$e_{ni}(rms) = \frac{e_o(rms)}{A_v} = \frac{735\mu V}{20} = 36.8\mu V$$

this agrees well with the data sheet typical spec. of $35\mu V$

Equivalent input spot noise voltage

$$e_{ni} = \frac{e_o}{A_v} = \frac{60nV/\sqrt{Hz}}{20} = 3.0nV/\sqrt{Hz}$$

Input Signal Noise Floor (1Hz Band)

$SNF = 13.01 + 20\log(e_{ni})$
$= -157.4dBm$

Approximately equal to the data sheet typical spec. of $-158dBm$

Integrated input Noise Floor is SNF + 10log(NPB)

Noise Figure with $R_s = R_t = 50\Omega$

$$NF = 10\log\left[2 + \frac{[(2.8pA)25\,\Omega)]^2 + (2.4nV)^2 + \left[\frac{(17pA)(1500\Omega)}{20}\right]^2 + \frac{4kT(1500\,\Omega)}{20}}{kT(50\,\Omega)}\right]$$

NF = 16.5dB for the CLC401

Conclusions:

With the techniques described here and the data of Appendix II, any of the commonly used noise descriptions may be developed. Note that the noise figures developed in the example for the CLC400 and CLC401 are rather high, resulting from a relatively high equivalent input noise voltage. As described in Application Note OA-11, noise figure will decrease as the gain is increased and is in fact lower for inverting vs. non-inverting configurations above a certain gain unique to each part. Conversely, taking a part intended for high gains, such as the CLC401, and operating it at low gains will always yield much higher input noises and noise figures than a corresponding part intended for low gains. This results from the requirement that the feedback resistor (the gain term for the inverting bias current noise) be relatively high for higher gain parts using the current feedback topology.

A technique for reducing the noise figure by using an input transformer is described in Application Note OA-14 ("Improving Amplifier Noise Figure for High 3rd Order Intercept Amplifiers").

Reference 1 "Low Noise Electronic Design" Motchenbacher and Fitchen
Reference 2 "Analysis and Design of Analog Integrated Circuits" Gray and Meyer

Appendix I.

Including 1/f and Noise Power Bandwidth Effects

For signal processing applications that are bandlimited in such a way as to include the 1/f noise region as a significant part of the total NPB, the increase in noise seen at low frequencies and modeled as a 1/f increase in the equivalent input spot noise terms, must be considered. The discussion that follows will focus on the non-inverting voltage spot noise term, although similar considerations must be applied to the two current noise terms for a complete analysis.

If we consider the total input spot noise power to be the sum of a constant flatband value and a frequency-dependent term, we can write

e_t^2 = total input spot noise power

$$e_t^2 = e_n^2 + \frac{e_x^2}{f}$$

where e_x is unknown
and f = frequency in Hz
and e_n = flatband spot noise voltage

At some frequency we can observe that the total equivalent input noise power has doubled. Hence, at this frequency the two power contributions are equal. Given this frequency,

f_{3dB} = frequency at which spot noise power has doubled from the flatband value, or the spot voltage noise has increased $\sqrt{2}$

$$2e_n^2 = e_n^2 + \frac{e_x^2}{f_{3dB}}, \quad e_x^2 = f_{3dB}(e_{ni}^2)$$

$$\text{then, } e_T^2 = e_n^2 + \frac{f_{3dB}}{f}(e_n^2), \; e_T^2 = e_n^2\left(1 + \frac{f_{3dB}}{f}\right)$$

$$\text{and } e_T = e_n\sqrt{1 + \frac{f_{3dB}}{f}}$$ spot noise voltage including the 1/f noise region

If the spot noise expressions are of interest, this adjustment to the reported flatband values in Appendix II, along with the 1/f noise corner frequency, should be used at frequencies near or below the f_{3dB} frequency. If the noise integrated over a particular frequency range is of interest, it is best to develop an equivalent spot noise voltage over that frequency range first, and then multiply by the square root of the NPB. This equivalent input spot noise, including 1/f effects, is developed as the average noise power over that frequency range using the spot noise expression developed above.

$$e_{eq.}^2 = \frac{1}{f_2-f_1}\int_{f_1}^{f_2} e_n^2\left(1+\frac{f_{3dB}}{f}\right)df \qquad \begin{matrix} f_1 \rightarrow \text{lower frequency limit} \\ f_2 \rightarrow \text{upper frequency limit} \end{matrix}$$

$$e_{eq.}^2 = \frac{e_n^2}{f_2-f_1}\left[(f_2-f_1) + f_{3dB}\ln\left(\frac{f_2}{f_1}\right)\right] = e_n^2\left[1+\frac{f_{3dB}}{f_2-f_1}\ln\left(\frac{f_2}{f_1}\right)\right]$$

or, going back to equivalent spot voltage

$$e_{eq.} = e_n\sqrt{1+\frac{f_{3dB}}{f_2-f_1}\ln\left(\frac{f_2}{f_1}\right)}$$

Note that f_1 cannot be 0 in this expression. To evaluate the expression, use an arbitrarily low f_1 for DC coupled applications, typically 10Hz. Also note that this adjustment to the flatband e_{ni} is increasingly insignificant as f_2 extends well above f_{3dB}. The table below computes the adjustment factor to the flatband noise as the upper cutoff frequency (f_2) is extended beyond the 1/f noise corner (f_{3dB}).

Letting $f_1 = 10Hz$, $f_{3dB} = 10kHz$

f_2	$\sqrt{1+\frac{f_{3dB}}{f_2-f_1}\ln\left(\frac{f_2}{f_1}\right)}$
1kHz	6.9
10kHz	2.8
100kHz	1.4
1MHz	1.06
10MHz	1.006

Using the equivalent spot noise voltage (and currents), the integrated noise may be determined using the noise power bandwidth. For a given voltage transfer function over frequency, the NPB is that rectangular frequency span that encloses the same power as the network's frequency response (Reference 1). The relationship between the more commonly specified −3dB bandwidth and the noise power bandwidth depends on the response shape. For the single pole low pass response, the relationship is

$$H_{(s)} = \frac{w_o}{s+w_o} \text{ where } f_{-3dB} = \frac{w_o}{2\pi} = \text{-3dB point}$$

$$\frac{NPB}{f_{-3dB}} = 1.57$$

For a single pair of complex poles acting as a low pass filter,

$$H_{(s)} = \frac{w_o^2}{s^2 + s\frac{w_o}{Q} + w_o^2}$$

$$f_{-3dB} = \frac{w_o}{2\pi}\sqrt{\left(1-\frac{1}{2Q^2}\right)+\sqrt{\left(1-\frac{1}{2Q^2}\right)+1}}$$

$$\frac{NPB}{f_o} = Q\frac{\pi}{2} \qquad \text{where } f_o = \frac{w_o}{2\pi}$$

Comlinear's current feedback amplifiers are designed to have a Q=.707 at the gain and R_f value listed at the top of each part's specifications table. With Q=.707, the closed loop poles are at ±45° to the negative real axis (in the s-plane) and a maximally flat Butterworth response is achieved. Using Q=.707, and noting that $f_{-3dB} = f_o$ for this Q,

$NPB/f_{-3dB} = 1.11$ (this agrees with Reference 2, page 660)

For higher order filter responses, the NPB approaches the −3dB bandwidth. If a filter follows the amplifier, the NPB of the filter should be used.

Appendix II.

Input Spot Noise Component Terms for Comlinear Amplifiers

Listed below are the separate input noise terms measured for the family of both monolithic and hybrid amplifier products. These are defined as:

e_n = Non-inverting input noise voltage in $nV/\sqrt{Hz}$

i_{bn} = Non-inverting input noise current in $pA/\sqrt{Hz}$

i_{bi} = Inverting input noise current in $pA/\sqrt{Hz}$

(Also refer to Figure 1 in the noise analysis description)

The values reported represent the average measured for that term from 1MHz to 10MHz (note that the powers are averaged, then the voltage or current derived as the square root of that average power). 1MHz is generally above any 1/f effects while 10MHz is below any response rolloff effects for the amplifiers under test. The flatband region of performance is assumed to extend beyond 10MHz.

The reported flatband spot noise values are very consistent for a particular amplifier from part to part. The 1/f noise corner frequencies are consistently lower, and more consistent from part to part, for the hybrid amplifiers as opposed to the monolithic amplifiers. Variations in the 1/f noise corner frequencies have been observed for the monolithic amplifiers with the reported number an estimate of the typical and 100kHz a good measure of the maximum for most of the monolithic amplifiers. As described in Appendix I, for most broadband applications, the flatband value will dominate the overall noise performance with the 1/f corner location of secondary importance.

In some cases, the numbers reported here do not agree with those in the individual data sheets. Some of the earlier data sheet noise numbers were extracted from measured data neglecting the effect of the resistor noises. As described in the noise analysis, this can sometimes lead to significant errors.

The separated noise terms reported here should take precedence over those reported in the data sheet for the amplifiers considered.

Table I
Comlinear Monolithic Amplifier Equivalent Input Noise Components (typical value)

Part #	Non-inverting input noise voltage		Noninverting input noise current		Inverting input noise current		Comments
	e_n (nV/$\sqrt{Hz}$	1/f(kHz)	i_{bn}(pA/$\sqrt{Hz}$	1/f(kHz)	i_{bi}(pA/$\sqrt{Hz}$	1/f(kHz)	
CLC400	2.5	40	3.2	100	14	60	CFB, Low Gain
CLC401	2.4	30	2.6	30	17	45	CFB, High Gain
CLC402	1.7	60	26	120	19	150	CFB, Low Gain
CLC404	3.2	25	2.2	200	12	90	CFB, Medium Gain
CLC406	2.7	3	2.1	16	11	5	CFB, Medium Gain
CLC409	2.2	2	3.2	30	14	6	CFB, Low Gain
CLC410	2.5	10	2.7	10	14	20	CFB, Low Gain Disable pin left open
CLC411	2.7	9	5.2	5.0	17.4	2.0	CFB, Low Gain ±15V Supplies
CLC414	4.2	30	1.3	80	9.8	40	CFB, Medium Gain Quad, OP Amp Low Power
CLC415	3.0	2	2.0	11	11.5	3	CFB, Medium Gain Quad, OP Amp Wideband
CLC420	4.1	1.2	1.9	10	1.9	10	VFB
CLC422	2.4	.8	4.2	1.1	4.2	1.1	VFB
CLC425	1.05	5	1.6pA	10	1.6	10	VFB
CLC430	3.0	4	3.2	4	14.8	2	CFB, Low Gain ±15 V Supplies
CLC500	1.6	30	24	40	19	95	Clamp voltages at ±3V CFB, Low Gain
CLC501	2.4	50	8.4	120	19	55	Clamp voltages at ±3V CFB, High Gain
CLC502	1.7	85	24	50	20	90	Clamp voltages at ±3V CFB, Low Gain
CLC505	5.3	50	1.4	80	9.0	40	CFB, Medium Gain R_p=300kΩ, I_{cc}=1mA
CLC505	3.1	75	1.8	300	9.9	180	CFB, Medium Gain R_p=100kΩ, I_{cc}=1mA
CLC505	2.4	84	2.4	800	11.1	300	CFB, Medium Gain R_p=300kΩ, I_{cc}=1mA

When a revision is made, we will add parts to this table.

Notes: 1. Power supplies at ± 5V unless noted
2. Tested at 25°C ambient, 290°K used to get 4kT = 16E – 21J
3. Spot noise is average from 1MHz to 10MHz
4. 1/f = typical frequency at which spot noise power has doubled
5. CFB = Current Feedback Op Amp
6. VFB = Voltage Feedback Op Amp

Table II
Comlinear Hybrid Amplifier Equivalent Input Noise Components (typical value)

Part #	Non-inverting input noise voltage		Noninverting input noise current		Inverting input noise current		Comments
	e_n (nV/√Hz	1/f(kHz)	i_{bn}(pA/√Hz	1/f(kHz)	i_{bi}(pA/√Hz	1/f(kHz)	
CLC103	2.0	2.5	2.4	5.0	15.0	16.0	CFB, High Gain
CLC200	2.4	1.8	1.9	36.0	33.0	2.5	CFB, High Gain
CLC201	2.5	.7	3.0	2.8	30.0	.9	CFB, High Gain
CLC203	2.2	.9	2.5	3.3	11.4	2.3	CFB, High Gain
CLC205	1.8	1.7	2.5	2.7	18.3	7.0	CFB, High Gain
CLC206	1.8	5.0	2.7	3.8	19.6	9.0	CFB, High Gain
CLC207	1.7	1.4	2.6	3.0	21.0	6.0	CFB, High Gain
CLC220	2.4	2.0	2.6	8.0	30.0	.6	CFB, High Gain
CLC221	2.8	.6	2.8	4.5	34.0	.8	CFB, Low Gain
CLC231	2.8	1.3	2.7	7.0	23.0	1.1	CFB, Low Gain
CLC232	2.8	.9	2.7	2.3	20.0	1.0	CFB, Low Gain
CLC300A	2.8	.5	2.2	8.0	10.9	10.0	CFB, High Gain
CLC560 & CLC561	2.1	.4	2.8	.4	34.0	2.0	DriveR-*amps*™

When a revision is made, we will add parts to this table.

Notes: 1. Power supplies at ± 15V
2. Tested at 25°C ambient, 290°K used to get 4kT = 16E – 21J
3. Spot noise is average from 1MHz to 10MHz
4. 1/f = typical frequency at which spot noise power has doubled
5. CFB = Current Feedback Op Amp

Application Note OA-13

Current Feedback Amplifier Loop Gain Analysis and Performance Enhancements

Michael Steffes

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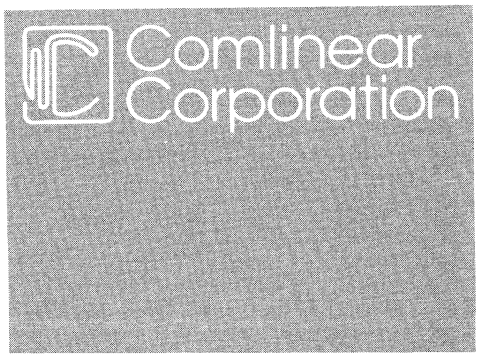


With the introduction of commercially available amplifiers using the current feedback topology by Comlinear Corporation in the early 1980s, previously unattainable gains and bandwidths in a DC coupled amplifier became easily available to any design engineer. The basic achievement realized by the current feedback topology is to de-couple the signal gain from the loop gain part of the overall transfer function. Commonly available voltage feedback amplifiers offer a signal gain expression that appears identically in the loop gain expression, yielding a tight coupling between the desired gain and the resulting bandwidth. This historically has led to the gain-bandwidth product idea for voltage feedback amplifiers. The current feedback topology transcends this limitation to offer a signal bandwidth that is largely independent of gain. This application note develops the current feedback transfer function with an eye towards manipulating the loop gain.

Current Feedback Amplifier Transfer Function Development

The equivalent amplifier circuit of Figure 1 will be used to develop the non-inverting transfer function for the current feedback topology. The current feedback topology is also perfectly suitable for inverting mode operation, especially inverting summing applications. The non-inverting transfer function will be developed, in preference to the inverting, since the inverting transfer function development is a subset of the non-inverting.

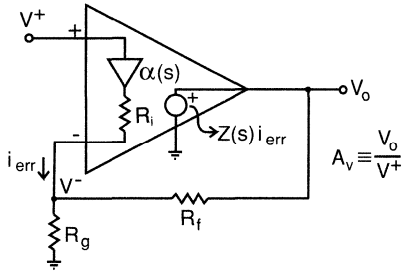


Figure 1: Current Feedback Amplifier Internal Elements

The amplifier's non-inverting input presents a high impedance to the input voltage, V^+, so as to not load the driving source. Any voltage appearing at the input node is passed through an open loop, unity gain, buffer that has a frequency dependent gain, $\alpha(s)$. $\alpha(s)$ is very neatly equal to 1 at DC (typically .996 or higher, but always < 1.00) and typically has a -3dB point beyond 500 MHz. The output of the buffer ideally presents a 0Ω output impedance at the inverting input, V^-. It actually shows a frequency dependent impedance, Z_i, that is relatively low at DC and increases inductively at high frequencies. For this development, we will only consider that Z_i is a small valued resistive impedance, R_i.

The intent of the buffer is to simultaneously force the inverting node voltage to follow the non-inverting input voltage while also providing a low impedance path for an error current to flow. Any small signal error current flowing in the inverting node, i_{err}, is passed through the buffer to a high transimpedance gain stage and on to the output pin as a voltage. This transimpedance gain, Z(s), senses i_{err} and generates an output voltage proportional to it. Z(s) has a very high DC value, a dominant low frequency pole, and higher order poles. When the loop is closed, the action of the feedback loop is to drive i_{err} to zero much like a voltage feedback amplifier will drive the delta voltage across its inputs to zero. Z(s) ideally transforms the error current into a zero ohm output impedance voltage source.

Figure 2 steps through the transfer function development including the effect of R_i. This analysis neglects the impact of a finite output impedance from Z(s) to the output, output loading interactions with that output impedance, and the effect of stray capacitance shunting R_g.

Start by summing currents at the V^- node of Figure 1

$$i_{err} + \frac{V_o - V^-}{R_f} = \frac{V^-}{R_g} \qquad \text{Eq. 1}$$

We also know that,

$$V^- = \alpha(s)\, V^+ - i_{err}\, R_i$$

and, $i_{err}\, Z_{(s)} = V_o$ then, $i_{err} = \frac{V_o}{Z_{(s)}}$

Multiply equation 1 through by R_f and isolate V^-

$$R_f\, i_{err} + V_o = V^- \left(1 + \frac{R_f}{R_g}\right)$$

Now substitute in for i_{err} and V^- from above

$$\frac{R_f\, V_o}{Z_{(s)}} + V_o = \left(\alpha(s)\, V^+ - \frac{V_o\, R_i}{Z_{(s)}}\right)\left(1 + \frac{R_f}{R_g}\right)$$

Gather V_o terms and solve for V_o / V^+

$$\frac{V_o}{V^+} = \frac{\alpha(s)\left(1 + \frac{R_f}{R_g}\right)}{1 + \frac{R_f + R_i\,(1 + R_f/R_g)}{Z_{(s)}}} \qquad \text{Eq. 2}$$

Figure 2. Current Feedback Amplifier Transfer Function

It is instructive to consider the separate parts of Equation 2 separately.

$\alpha(s)$ —> Frequency dependent buffer gain. Normally considered = 1

$1 + R_f / R_g$ —> Desired signal gain. Identical to voltage feedback non-inverting amplifier gain.

$$\frac{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}{Z_{(s)}} = \frac{1}{\text{Loop Gain}}$$

$$\text{Hence, Loop Gain (LG)} = \frac{Z_{(s)}}{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}$$

$$= \frac{\text{internal forward transimpedance}}{\text{feedback transimpedance}} \qquad \text{Eq. 3}$$

The loop gain expression is of particular interest here. If Z(s), the forward transimpedance, is much greater than $R_f + R_i(1+R_f/R_g)$, the feedback transimpedance, (as it is at low frequencies) then this term goes to zero leaving just the numerator terms for the low frequency transfer function. As frequency increases, Z(s) rolls off to eventually equal the feedback transimpedance expression. Beyond this point, at higher frequencies, this term increases in value rolling off the overall closed loop response.

The key thing to note is that the elements external to the amplifier that determine the loop gain, and hence the closed loop frequency response, do not exactly equal the desired signal gain expression in the transfer function numerator. **The desired signal gain expression has been de-coupled from the feedback expression in the loop gain.**

If the inverting input impedance were zero, the loop gain would depend externally only on the feedback resistor value. Even with small R_i, the feedback resistor dominantly sets the loop gain and every current feedback amplifier has a recommended R_f for which Z(s) has been optimized. As the desired signal gain becomes very high, the $R_i(1+R_f/R_g)$ term in the feedback transimpedance can come to dominate, pushing the amplifier back into a gain bandwidth type operation.

Understanding the Loop Gain

It is very useful, and commonly done for voltage feedback amplifiers, to look at the loop gain graphically. Figure 3 shows this for the CLC400, a low gain part offering DC to 200MHz performance. What has been graphed is 20*log(|Z(s)|), the forward transimpedance gain, along with its phase, and 20 log(Zt). **This Z_t is the feedback transimpedance, $R_f+R_i(1+R_f/R_g)$, and where it crosses the forward transimpedance curve is the frequency at which the loop gain has dropped to 1.** Note that the forward transimpedance phase starts out with a 180° phase shift, indicating a signal inversion through the part, and could have plotted as continuing to 360° or, as shown, going to zero. Using these axis allows a direct reading of the phase margin at unity gain crossover.

As with any negative feedback amplifier, the key determinant of the closed loop frequency response is the phase margin at unity gain crossover. If the phase has shifted completely around to 360°, or dropped to zero on the axis used above when the loop gain has decreased to 1, unity gain crossover - (where the 20 log(Z_t) line intersects the 20 log(/Z(s)/) curve), the denominator in the closed loop expression will become (1-1), or infinity (For the axis used above, the closed loop expression (Eq.2) would have a 1-1/LG in the denominator. The form developed as Equation 2 accounted for the inversion with the sign convention for i_{err} and V_o).

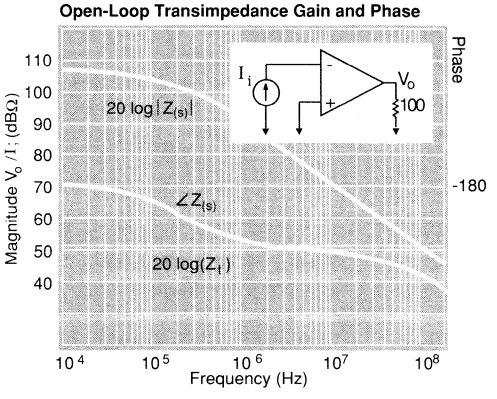


Figure 3

It is critical for stable amplifier operation to maintain adequate phase margin at the unity gain crossover frequency. The feedback transimpedance that is plotted in Figure 3 is $R_f+R_i(1+R_f/R_g)$ evaluated at the specifications setup point for the CLC400. This yields:

$R_f = 250\Omega$ then

$A_v \equiv 1 + \frac{R_f}{R_g} = 2$ $Z_t = 250\Omega + 50\Omega\ (2) = 350\Omega$

and

$Z_i \simeq 50\Omega$ 20 log (350Ω) = 50.9 dB

Looking at the unity gain crossover near 100MHz, we see somewhere in the neighborhood of a 60° phase margin. This is Comlinear's targeted phase margin at the gain and R_f used to specify any particular current feedback part. This phase margin, for simple 2 pole Z(s), yields a maximally flat Butterworth filter shape for the closed loop amplifier response (Q=.707). Note that the design targets reasonable flatness over a wide range of process tolerances and temperatures. This typically yields a nominal part that is somewhat overcompensated (phase margin > 60°) at room temperature.

Note that the closed loop bandwidth will only equal the open loop unity gain crossover frequency for 90° phase margins (single pole forward gain response). As the open loop phase margin decreases from 90°, with the impact of higher frequency poles in the forward transimpedance gain, the closed loop poles move off the negative real axis (in the s- plane) peaking the response up and extending the bandwidth. The actual bandwidth achieved by Comlinear's amplifiers is considerably beyond the unity gain crossover frequency due to these open loop phase effects.

Controlling the Loop Gain

One of the key insights provided by the loop gain plot is what happens when Z_t is changed. Decreasing Z_t (dropping the horizontal line of 20 log(Z_t)), will extend the unity gain crossover frequency but will sacrifice phase margin. This is commonly seen in current feedback amplifiers when an erroneously low R_f value is used yielding an extremely peaked frequency response. In fact a very reliable oscillator can be generated with any current feedback amplifier by using R_f=0 in a unity gain configuration. Conversely, increasing Z_t (raising the horizontal line of 20 log(Z_t)) will drop the unity gain crossover frequency and increase phase margin. Increasing R_f is in fact a very effective means of over-compensating a current feedback amplifier. Increasing R_f will decrease the closed loop bandwidth and/or decrease peaking in the frequency response.

Computing Z_t for the design point used in setting the specifications for any particular current feedback part indicates an optimum targeted feedback transimpedance under any condition.

In design, the internal Z(s) has been set up to yield a maximally flat closed loop response with the gain and Rf used to develop the performance specifications. If we then try to hold the same feedback transimpedance under different gain conditions, an option not possible with voltage feedback topologies, this optimum unity gain crossover for the open loop response can be maintained.

If we designate this optimum feedback transimpedance as Z_t*,

we would like to hold $R_f+R_i(1+R_f/R_g)=Z_t$*
(where R_f and $1+R_f/R_g$ are those values shown at the top of the parts performance specifications.)

Substituting $A_v=1+R_f/R_g$, we get, $R_f = Z_t^* - R_iA_v$ Eq. 4
(where R_f is a new value to be used at a gain other than the design point.)

This is a design equation for holding optimum unity gain crossover. Having computed R_f to hold $Z_t = Z_t$*
$R_g=R_f/(A_v - 1)$ Eq.5

The Benefits of Controlling Z_t

As an example of adjusting R_f to hold a constant Z_t as the desired signal gain is changed, consider a CLC404 at gains of +2, +6 and +11. Figure 4 shows test results over these gains for a fixed R_f - very similar to how the CLC404 data sheet plots were generated.

Using the CLC404 design and specifications points (see Appendix I)
A_v = +6
R_f = 500 Ω
R_i = 30 Ω
Z_t^* = 500 + 30*6 = 680 Ω

Figure 5 shows the same part operated with R_f adjusted as indicated by Equation 4. R_g in both cases is set using Equation 5.

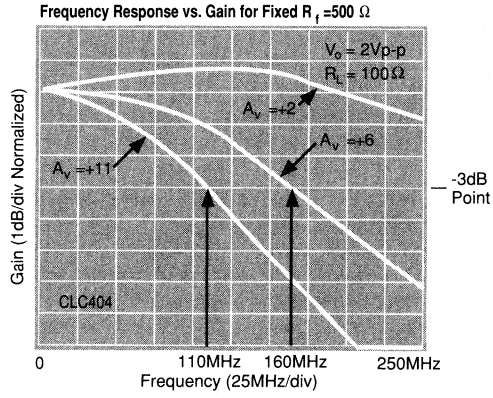


Figure 4

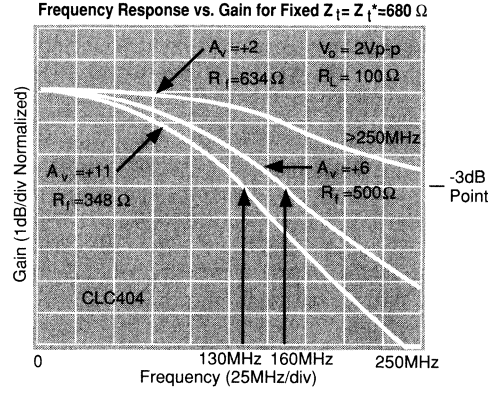


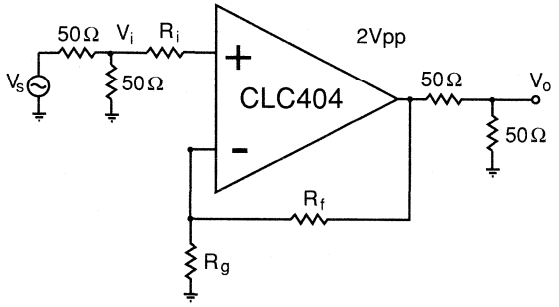
Figure 5

The results of Figure 5 vs. Figure 4 show that adjusting R_f does indeed hold a more constant frequency response over gain than a simple fixed R_f. The low gain response has flattened out while the high gain response has been extended.

The remaining variability in frequency response can be attributed to 2nd order effects that have not yet been considered. As described in Application Note OA-15, parasitic capacitance shunting the gain setting resistor, R_g, will introduce a response zero for non-inverting gain operation. This zero location can be easily located by substituting $R_g||C_g$ into the numerator part of the transfer function, Equation 2. This yields a zero at $1/(R_f||R_g)C_g$ in radians. This effect would not be observed in inverting mode operation yielding a much more consistent response over gains, especially with R_f adjusted as shown above.

If we assume equal parasitic capacitances on the two inputs, we can cancel this zero by introducing a series impedance into the non-inverting input that equals $R_f||R_g$. Figure 6 shows the test circuit and table of values used

to test this for the same CLC404 used above. Note that we must include the equivalent source impedance of the source matching and termination resistors in setting the series resistor into the non-inverting node, (25 Ω here). Note that the table shows actual standard values used, rather than the exact calculated values.



$R_f = 680 - A_v(30)$
$R_g = R_f/(A_v - 1)$
$R_i = (R_f || R_g) - 25\Omega$

A_v	R_f	R_g	R_i
+2	634	634	287
+6	500	100	56.2
+11	348	34	6

Figure 6

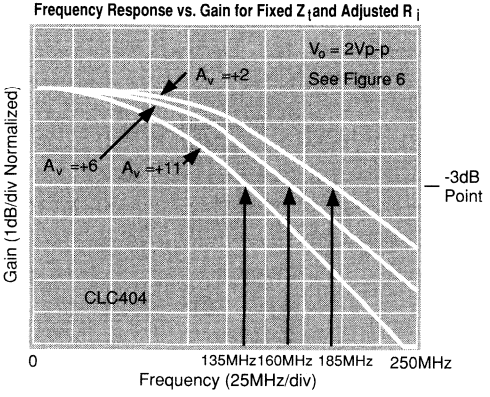


Figure 7

Figure 7 shows the measured frequency responses under the conditions tabulated in Figure 6.

Clearly, adding R_i has brought the low gain response to be much more consistent with the higher gains. Little effect was observed by adding R_i at gains of 6 and 11. Generally, adding R_i is particularly effective at flattening out the frequency response for higher gain parts, which are designed using high value of feedback resistors, when they are operated at lower gains.

An alternative to adding R_i is simply to continue to increase R_f until the loop gain is overcompensated enough to cancel the zero. This is increasingly ineffective as the resistor values get larger but was developed empirically for the CLC414 and CLC415 quad amplifiers (Refer to those data sheets for details). An alternative approach with those parts would be to adjust R_f using the data from Appendix I and then add an R_i as described above.

Note that Equation 3 will predict negative R_f values as the desired gain exceeds Z_t^*/R_i. From a loop gain standpoint, this is exactly correct. However, additional concerns (particularly distortion and output current limits) will come in to limit the applicable range of gains for Equation 3. Generally, the total loading on the amplifiers should not be allowed to drop below 65 ohms. This is the actual load in parallel with R_f+R_g for the non-inverting configuration. For a 100 ohm load, this limits the minimum R_f+R_g to about 200 Ω. Lower values can be used if R_L is greater. For inverting mode, which has exactly the same loop gain expression as non-inverting, R_f alone appears in parallel with R_L as an additional load. This would limit R_f to a minimum of 200 Ω in inverting mode operation. This does not, of course, limit the amplifier's maximum gain. When a minimum R_f has been reached, R_g can continue to decrease, yielding higher gains, with a gain bandwidth characteristic eventually developing as the R_i $(1+R_f/R_g)$ part of Z_t comes to dominate.

Special Considerations for Variable Supply Current

The inverting input impedance, R_i, is essentially the output impedance of parallel/series combinations of emitter followers for most Comlinear amplifiers. Thus, R_i is some fraction or integer multiple of V_t/I_c, where V_t=kT/q and I_c is the bias current in those transistors. For lower power parts, and parts with adjustable supply currents, R_i can get very large, as I_c decreases quickly putting the parts into a gain bandwidth type operation. Appendix I shows the nominal design point I_c, along with a room temperature R_i, and, for the adjustable supply current, I_{cc}. Anything that adjusts the total quiescent supply current from its nominal design point, changing power supply voltages, using the bias adjust pins on some parts, etc., will scale the I_c listed in Appendix I in direct proportion to I_{cc}.

Additional Loop Gain Control Applications

Recognizing that the inverting input impedance provides an opportunity to adjust the loop gain, without having any impact on the signal gain, we can add a resistor inside the loop that can act as an independent frequency response compensation element. This is very useful if a fine control over the frequency response shape is desired.

Using the same CLC404 used in the earlier tests (a part that is nominally overcompensated as shown by the rolloff at its gain of +6 condition in Figure 4), the circuit of Figure 8 shows an adjustment technique for the frequency response. Since we are intentionally adding R_i to the feedback transimpedance expression, Z_t, it is recommended to approximately set R_f to yield Z_t^* when the

adjustment to R_i is at midrange. This will yield a lower R_f as shown in Figure 8. Figure 9 shows the original gain of +6 response of Figure 4, along with the response achieved with the circuit of Figure 8 with R_p adjusted to yielded maximally flat frequency response. This circuit shows a ± .1dB gain flatness to beyond 100 MHz.

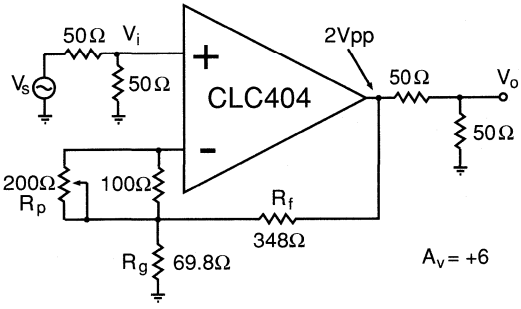


Figure 8: Adjustable Frequency Response

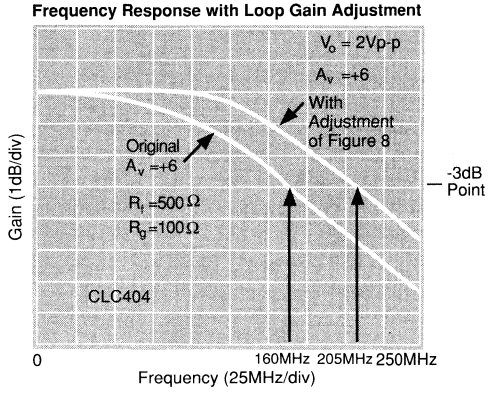


Figure 9

In inverting applications there is oftentimes a conflict between the required gain setting resistors from an input impedance and signal gain standpoint, and what the amplifier would like to see from a loop gain phase margin standpoint. In a similar fashion to voltage feedback, in this case, an additional resistor to ground on the inverting input can be used to tune the loop gain independently of the inverting signal gain requirements. The drawback of this, is that, like voltage feedback, this increases the noise gain for the non- inverting input voltage noise.

Figure 10 shows an example of a transimpedance application using a CLC401 with a 1kΩ feedback resistor. In this case, the value of the feedback resistor is set by the desired signal gain, while R_g is used to satisfy the loop gain phase margin by setting the feedback transimpedance to $Z_t^* = 2.5k$.

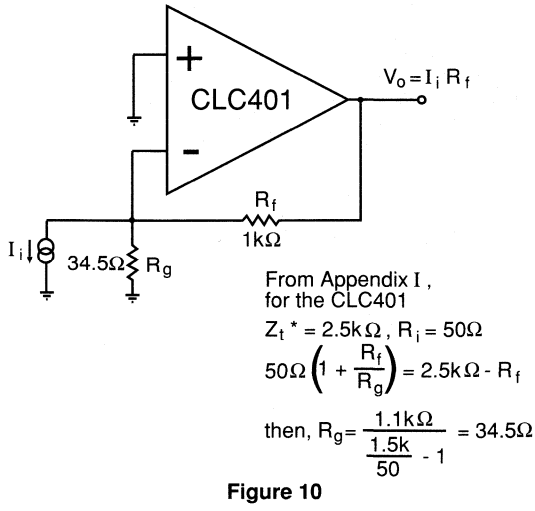


Figure 10

Similarly, in an inverting summing application, once the desired gain and input impedance conditions are set, the loop gain can be independently controlled through the use of an additional resistor to ground on the inverting input. Figure 11 shows an example of this using the CLC401 summing 5 channels, at a gain of -1 for each channel, using 1k Ω input resistors.

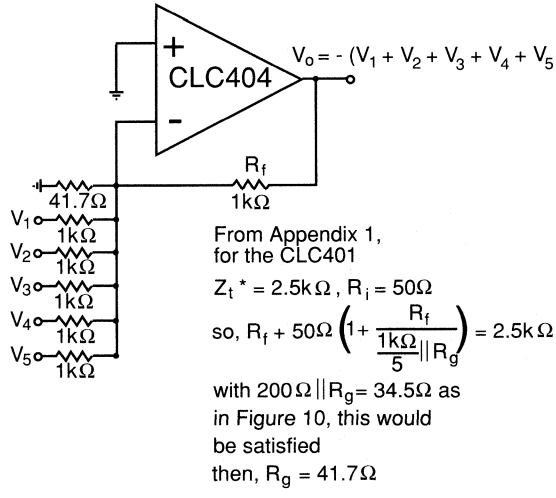


Figure 11: Loop Gain Adjusted in inverting Summing Application

Conclusions

The current feedback topology has allowed us to de-couple the signal gain from the loop gain expressions. This provides ample opportunity for independent control of both the signal gains and the frequency response by using only resistive elements. A thorough understanding of the loop gain mechanisms provides the designer with a flexibility unavailable to the voltage feedback op amp.

Appendix I

The data tabulated here provide the necessary information to hold a constant feedback transimpedance over a wide range of closed loop signals gains for the current feedback amplifiers available from Comlinear at the time of this application note's publication. The data is broken into a set for the monolithic amplifiers, which generally have a higher R_i due to their lower quiescent bias current, and a set of data for the hybrid amplifier products.

The table entries show

1. A_v -> Non-inverting voltage gain used to set device specs.
2. R_f -> Feedback resistor value used to set the device specs.
3. R_i -> Nominal inverting input impedance

These 3 items are used to compute the optimum feedback transimpedance for the particular part. This is given by

$$Z_t^* = R_f + R_iA_v$$

This information is used to compute a more optimum R_f as the desired closed loop gain moves away from the design point A_v.

It is important to note that, given any feedback R_f and any closed loop non-inverting signal gain, a feedback transimpedance can be computed using the equation for $Z_t = R_f + R_iA_v$. Z_t^* is the optimum value for open loop phase margin and closed loop response flatness found by evaluating the expression at the specific R_f and gain used in designing and specifying the part.

Ic -> Approximate collector current for the emmitter followers seen looking into the inverting input. The inverting inputs do not necessarily present an integer number of series/parallel emmitter followers. The approximate scale factors can be computed by solving for n in the following expression.

$R_i = n\ V_t/I_c$ with $V_t = kT/q$ (=26mV at room temperature)

I_c/I_{cc} -> ratio of inverting input stage bias current to the total device quiescent current. With n determined from above, the adjusted value for R_i may be determined for a part that is being operated at a different quiescent current than is normally specified.

The data presented here represent a good approximation to the device characteristics. Several second order effects have been neglected for the sake of simplicity.

The CLC505, an adjustable supply current op amp, was optimized at 9mA supply current. No attempt was made in this table, or in the data sheet, to reset the optimum R_f as the supply current is decreased. At very low supply currents, the CLC505's inverting input impedance dominates the feedback transimpedance expression. To compensate for this with a reduced R_f, as has been suggested in this document, would require such low values as to excessively load the limited output drive current available. The CLC505 at 1mA supply current shows a gain bandwidth product performance due to the dominance of R_i in the loop gain equation.

Table 1

Comlinear Monolithic, Current Feedback, Amplifier Optimum Feedback Transimpedance and Operating Point Information

Part #	Design Point Information				Operating Currents		Comments
	A_v	R_f (Ω)	R_i (Ω)	Z_t* (Ω)	I_c (mA)	I_c/I_{cc}	
CLC400	+ 2	250	40	330	.67	.045	
CLC401	+ 20	1500	50	2500	.52	.035	
CLC402	+ 2	250	16	282	.82	.055	
CLC404	+ 6	500	30	680	.87	.080	
CLC406	+ 6	500	60	860	.43	.09	
CLC409	+ 2	250	25	300	1.05	.08	
CLC410	+ 2	250	35	320	.74	.05	disable left open
CLC411	+ 2	301	50	400	.52	.05	disable left open
CLC414	+ 6	500	250	2000	.105	.05	each amplifier of quad
CLC415	+ 6	500	60	860	.43	.09	each amplifier of quad
CLC430	+ 2	750	60	870	.43	.04	disable left open
CLC500	+ 2	250	32	314	.82	.05	
CLC501	+ 20	1500	30	2100	.86	.05	see note 3
CLC502	+ 2	250	16	282	.82	.05	
CLC505	+ 6	1000	50	1300	.52	.06	I_{cc} = 9.0 mA R_p = 33 kΩ
CLC505	+ 6	1000	150	1900	.175	.06	I_{cc} = 3.3 mA R_p = 100 kΩ
CLC505	+ 6	1000	490	3950	.053	.06	I_{cc} = 1.0 mA R_p = 300 kΩ

Notes

1. Power supplies at ± 5V
2. 25°C temperature assumed; yields kT/q = .026V
3. CLC501 specification point at A_v = + 32, R_f = 1500Ω
   Design point, however is at A_v = + 20, R_f = 1500Ω

Table 2

Comlinear Hybrid, Current Feedback, Amplifier Optimum Feedback Transimpedance and Operating Point Information

Part #	Design Point Information				Operating Currents		Comments
	A_V	R_f (Ω)	R_i (Ω)	Z_t* (Ω)	I_c (mA)	I_c/I_{cc}	
CLC103	20	1500	8.5	1670	1.57	.054	fixed internal R_f. See note 3
CLC203	20	1500	11.8	1736	2.21	.072	fixed internal R_f. See note 3
CLC200	20	2000	8.5	2170	1.54	.053	see note 4
CLC201	20	2000	17	2340	1.54	.053	see note 4
CLC205	20	2000	23Ω	2460	.74	.037	see note 5
CLC206	20	2000	15Ω	2300	1.10	.038	see note 5
CLC207	20	2000	23Ω	2460	.74	.030	see note 5
CLC220	20	1500	8.5	1670	1.54	.053	see note 4
CLC221	20	1500	17	1840	1.54	.053	see note 4
CLC231	2	250	15	280	1.78	.093	
CLC232	2	250	15	280	1.78	.071	
CLC300A	20	1500	7.5	1650	1.73	.070	see note 4

11

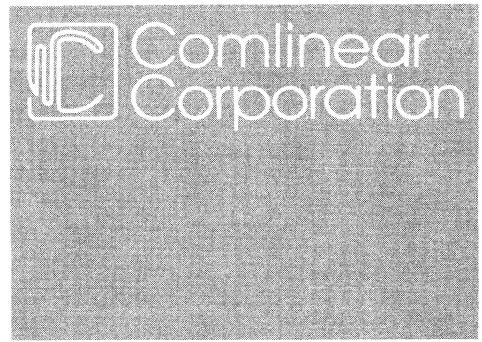
Notes

1. Power supplies at ±15V
2. 25°C temperature assumed; yields kT/q=.026V
3. CLC103 & CLC203 have fixed internal R_f. Cannot, therefore increase the R_f value or insert additional R_i for loop gain control.
4. These parts include an optional internal feedback resistor that may or may not be used in applying the part. Not using this internal R_f allows adjusting the R_f over gain and/or inserting additional R_i.
5. CLC205, CLC206, & CLC207 use a small shunting capacitance across the internal R_f to extend the bandwidth. Using a standard RN55D external R_f, with lower shunt capacitance, will require a larger nominal design point value for Z_t* to hold optimum loop gain. At A_V=+20, an external R_f=2.74 kΩ yields the desired Z_t.

Application Note OA-14

Improving Amplifier Noise Figure for High 3rd Order Intercept Amplifiers

Michael Steffes



Abstract: Wide spurious-free dynamic range is certainly the goal for any IF amplifier. This is particularly true for OTH radar as well as other systems using high resolution digitizers. Recently introduced current feedback amplifiers offer exceptional 3rd order intermodulation intercepts at very low quiescent power levels, but have been plagued by relatively poor noise figures. Teaming these op amps with a simple transformer input coupling yields noise figures less than 7dB with 3rd order intercepts greater than 40dBm (for frequencies < 10MHz).

Although not commonly considered for IF amplifiers, wideband, DC coupled operational amplifiers can offer considerable performance advantages at the lower IF (or HF) over standard AC coupled amplifiers. Particularly suitable from a distortion standpoint are a family of recently introduced monolithic current feedback operational amplifiers. Similar to the more common voltage feedback op amps, these parts offer very high non-inverting input impedance, very low output impedance, and a very high open loop gain that is controlled through the use of external resistors to set a well controlled closed loop gain. These amplifiers are unique in that the inverting node presents a low impedance through which the amplifier senses a feedback current as opposed to the more common feedback voltage. (Reference 1)

The current feedback topology, as implemented in Comlinear's CLC400 and CLC401 amplifiers, is also exceptionally symmetric. This yields intrinsically low distortion mechanisms internal to the amplifier which are then divided by the loop gain to yield the closed loop distortion. As described in Reference 1, the loop gain for a current feedback amplifier is principally set by the feedback resistor value. The loop gain will, of course, show a frequency dependence yielding a continued improvement in distortion down to the dominant open loop pole frequency (at approximately 350kHz for these parts). Conversely, the distortion will worsen moving to higher frequencies as the open loop gain rolls off. Measuring the 3rd order intermodulation intercept at 10MHz yields between 40 and 45dBm for these two parts. Although theory indicates a continued improvement below this frequency, accurate measurements are difficult to perform for intercepts above 45dBm for output power levels within the capability of these two devices.

Taking advantage of this exceptional intercept performance has, however, been impaired by noise figures ranging from 11 to 20dB depending on the device and the gain setting used. Reflecting all op amp noise sources to the non-inverting input typically yields an equivalent input spot noise voltage (at frequencies above the 1/f noise corner) that range from 2.4nV/$\sqrt{Hz}$ to well over 5nV/$\sqrt{Hz}$ (for the CLC401 operated at low gains.) Aside from the intrinsic noise voltage at the non-inverting input, the effect of the inverting noise current also contributes strongly to this result. (See the appendix and Application Note OA-12 for a discussion of calculating the equivalent input noise voltage.)

As suggested in the literature (Reference 2), transformer coupling can sometimes be used to reduce an amplifier's noise figure. This is possible when the equivalent input noise voltage is much greater than the noise voltage generated by the input noise current through the source impedance. Reference 2 suggests an optimum source impedance for noise figure given by the ratio of noise voltage to noise current. If this ideal impedance is much greater than the typical 50 ohm source impedance seen in IF strips (as it is for the two amplifiers considered here), a significant improvement in the noise figure can be achieved using transformer coupling. Conceptually, the transformer will provide a noiseless voltage gain at the expense of increasing the source impedance for the input noise current.

Using this technique with the current feedback op amps will sacrifice the DC coupling, with the transformer setting the low frequency limit of operation. Depending on the amplifier to set the high frequency limit will yield poor distortion performance near the amplifier's −3dB frequency. The amplifier's −3dB point is largely determined by the frequency at which the loop gain has dropped to unity. With negligible loop gain, the internal distortion mechanisms are no longer corrected yielding poor distortion performance. Hence, it is preferable to have the transformer also limit the high frequency performance. Both amplifiers considered here offer −3dB bandwidths exceeding 100MHz. A transformer offering good performance up through 50MHz maximum and down to as low a frequency as is desired would probably be a suitable choice.

Topology Description

Figure 1 shows the topology to be considered.

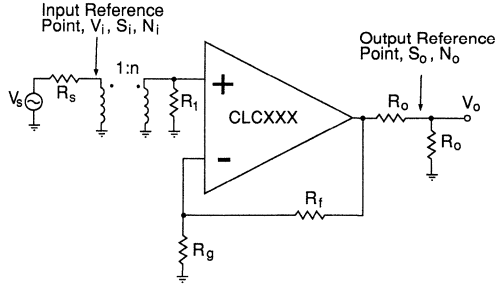


Figure 1

The transformer will provide a noiseless voltage gain from the voltage applied to its input to the non-inverting input of the amplifier. This is done at the expense of increasing the AC source impedance looking back out of the amplifier's non-inverting input. Increasing the turns ratio of the transformer (i.e. picking up voltage gain) will decrease the noise figure until the noise term due to the non-inverting input noise current times the source impedance equals the equivalent non-inverting input noise voltage.

Constraints and Assumptions

1. Input impedance matching to the source impedance (R_S) at the transformer input is desired. Therefore, $R_1 = n^2 R_S$

   With this assumption, going to the output side of the transformer, the source impedance for the non-inverting input noise current will equal $R_1/2$ or, in terms of R_S will be $n^2 R_S/2$.

   R_1 will also introduce a noise voltage term into the analysis.

2. Since the op amp offers a low output impedance, a separate matching resistor must be added to drive into a matched load as would be typical in an IF application (normally, $R_o = 50$ ohms). If we assume the resistor noise of the output matching network is negligible compared to the noise at the output, no change in the S/N ratio will be seen in going from the output pin of the amplifier to the load point. Therefore, the noise figure and gain will be calculated to the load point neglecting any noise added by the output matching resistor, R_o.

3. The various noise contributors for the amplifier are considered to be uncorrelated. This allows equivalent total noise powers to be developed as the sum of the separate noise powers. The noise voltage and currents are taken to be the spot noise values yielding a spot noise figure value. For transformer low frequency rolloff corners < 100kHz, some increase in spot noises at the low frequencies will be observed due to the 1/f noise corners for the amplifiers. (Refer to the individual op amp data sheets or Application Note OA-12 for detailed noise data).

Noise Figure Computation

To develop an expression of the noise figure for the circuit of Figure 1, the most elementary definition shown as Equation 1 will be used

$$NF = 10 \log \frac{S_i/N_i}{S_o/N_o} \qquad \textbf{Eq. 1}$$

This definition states that the noise figure is 10 times the log of the ratio of the signal/noise ratio at the input to the signal/noise ratio at the output. These ratios are for the signal and noise powers available at the input and output. The noise power available at the input is taken to be that delivered by R_s to a conjugant matched load where the noise of that load is separated out as being added by the system. Since some noise will always be added, the signal/noise ratio at the output will be degraded from that at the input yielding a noise figure always > 0.

To evaluate the noise figure expression, the circuit of Figure 1 is redrawn in a more idealized form in Figure 2.

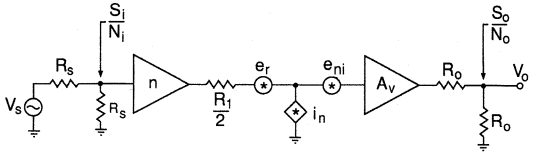


Figure 2

In this circuit, the transformer has been replaced by its equivalent elements; an input terminating impedance (R_s), a noiseless voltage gain given by the turns ratio (n), and an equivalent output impedance taken as the parallel combination of R_1 and R_s reflected through the transformer. ($R_1/2$). Note that R_1 has been reflected to the input side as a noiseless terminating resistor, R_s. R_1's noise contribution is retained as e_r on the output side of the transformer since this needs to be considered as part of the noise added by the system.

The amplifier has been replaced by an infinite input impedance gain block (A_v) with its two equivalent noise sources brought out as e_{ni} and i_n. Note that e_{ni} includes the noise contribution of the inverting input noise current and the feedback and gain setting resistor noises. (This analysis is described in the appendix.)

Although the gain and noise terms of Figure 2 have thus far been expressed as voltage gains with noise voltage and current terms, the noise figure development deals only with power gains and noise powers. Therefore, the gains and noises shown on Figure 2 will be modified to get the power gain from input to output and the noise powers delivered at the input and output.

Looking at the separate parts of the argument in Equation 1, we can separate them as:

$\frac{S_i}{S_o} \rightarrow$ inverse of the power gain through the path

$$= \frac{V_i^2/R_s}{\left(\frac{nA_vV_i}{2}\right)^2/R_o} = \frac{4}{(nA_v)^2}\,\frac{R_o}{R_s}$$

$\frac{N_o}{N_i} \rightarrow$ output noise power over input noise power

The output noise power can be developed by taking each contributing noise voltage term through to the output then developing the power of that voltage across R_o and adding all the terms. The separate noise voltage terms at the output are:

Source noise voltage $\rightarrow \sqrt{4KTR_s}\ \frac{1}{2}\ nA_v\ \frac{1}{2}$

Terminating resistor noise (e_r) $\rightarrow \sqrt{4KTR_1}\ \frac{1}{2}\ A_v\ \frac{1}{2}$

where K $\rightarrow$ Boltzman's constant
= 1.38E−23 Joules/°Kelvin
T $\rightarrow$ °Kelvin = 290° in this analysis
then 4kT = 16E−21J

Amplifier current noise $\rightarrow i_n\ \frac{R_1}{2}\ A_v\ \frac{1}{2}$

Amplifier current noise $\rightarrow e_{ni}\ A_v\ \frac{1}{2}$

Note that both noise voltages intrinsic to R_s and R_1 are attenuated by ½ due to the impedance matching present on both sides of the transformer (i.e. R_1 reflects to the source side as R_s to ground, and R_s reflects to the secondary side as the driving impedance for the non-inverting input terminating impedance, R_1).

Substituting with $R_1 = n^2 R_s$, and adding each noise voltage term squared divided by the output terminating impedance, R_o, will yield the total output noise power.

$$N_o = \left[KTR_s\left(\frac{nA_v}{2}\right)^2 + KTn^2R_s\left(\frac{A_v}{2}\right)^2 + i_n^2\left(\frac{n^2R_s}{2}\right)^2\left(\frac{A_v}{2}\right)^2 + e_{ni}^2\left(\frac{A_v}{2}\right)^2\right]/R_o$$

The input noise power may be derived as the power delivered to the source matching resistor from the source resistor noise voltage. This is:

$$N_i \rightarrow \left[\tfrac{1}{2}\sqrt{4KTR_s}\right]^2/R_s = KT$$

Pulling an $\left(\frac{nAv}{2}\right)^2 R_s$ out of the N_o expression, the ratio of input to output noise power may be rewritten as:

$$\frac{N_o}{N_i} = \frac{(nA_v)^2 R_s}{4R_o} \cdot \frac{KT + KT + i_n^2 n^2 \frac{R_s}{4} + \frac{e_{ni}^2}{n^2 R_s}}{KT}$$

Combining the expressions for noise power ratios and the inverse of the power gain through the channel, developed above, yields:

$$\frac{S_i}{S_o}\frac{N_o}{N_i} = \frac{4R_o}{(nA_v)^2 R_s} \cdot \frac{(nA_v)^2 R_s}{4R_o}\left(2 + \frac{i_n^2 n^2 \frac{R_s}{4} + \frac{e_{ni}^2}{n^2 R_s}}{KT}\right) =$$

$$\frac{S_i}{S_o}\frac{N_o}{N_i} = \left(2 + \frac{i_n^2 n^2 \frac{R_s}{4} + \frac{e_{ni}^2}{n^2 R_s}}{KT}\right)$$

Multiplying the fraction through, top and bottom, by R_s and going back to the log form for noise figure yields:

$$NF = 10 \log\left(2 + \frac{\left(i_n n \frac{R_s}{2}\right)^2 + \left(\frac{e_{ni}}{n}\right)^2}{KTR_s}\right) \qquad \textbf{Eq. 2}$$

Looking at the component parts of this expression, the "2" in the log argument arises from our terminating with a discrete (noisy) matching resistor, R_1. This increases the minimum achievable noise figure from 0dB to $10 \cdot \log(2) = 3$dB.

The $\frac{\left(i_n n \frac{R_s}{2}\right)^2 + \left(\frac{e_{ni}}{n}\right)^2}{R_s}$ part of the fraction

represents the 2 noise voltages (the total equivalent input noise voltage and the voltage generated by the noise current through the source impedance) at the input of the amplifier reflected to the transformer input and added as powers across R_s. The kT term in the denominator is simply the noise power available from the source at the input to the network. From this, as the turns ratio increases, the contribution of the noise current increases while that due to the noise voltage decreases. As reported in Reference 1, the minimum value will occur when these two terms are equal.

Solving for the optimum turns ratio to minimize the noise figure:

$$n_{opt} = \sqrt{\frac{e_{ni}}{i_n \frac{R_s}{2}}}$$

Substituting this in Equation 2 yields a minimum noise figure:

$$NF_{min} = 10 \log\left(2 + \frac{e_{ni} i_n}{KT}\right)$$

Recognizing that transformer turns ratios are actually only available in integer steps, the optimum turns ratio is somewhat academic. However, for a given n, it can be recognized that anything that will reduce i_n or e_n will improve the noise figure.

Little can be done to reduce the noise current at the amplifier's non-inverting input. The equivalent input noise voltage can, however, be reduced as the amplifier is operated at higher gains. The results in the appendix show that equivalent input noise terms due to the inverting noise current and resistor noises are reduced as the gain increases. However, once these noise terms have been reduced below the intrinsic non-inverting input noise voltage, further improvements through increased gain are minimal.

Design Procedure and Test Results

To illustrate the design procedure and the resulting performance using this input transformer coupling, two possible designs using the CLC400 and CLC401 will be developed. The designs will proceed with the assumption that the maximum gain consistent with broad bandwidth and good 3rd order intermod intercept is desired. Enough information is presented to allow a design to proceed from a targeted gain as well.

The CLC400 is a broadband DC coupled monolithic amplifier intended for relatively low gain operation. Typical specifications show a 200MHz bandwidth (−3dB) at a gain of +2. Both parts pull a nominal no load current of 15mA when operated from their recommended ±5 volt power supplies. For the current feedback topology, a low gain part corresponds to a part that has been optimized for a lower value of feedback resistor as opposed to a high gain part such as the CLC401. Hence, the nominal R_f at a gain of +2 for the CLC400 is shown on the data sheet as 250 ohms, while the CLC401 is optimized to use a 1.5k feedback at a gain of +20. Most of the requisite information for the design can be found in Comlinear Application Notes OA-12 (Noise Analysis) and OA-13 (Current Feedback Loop Gain Analysis).

Non-inverting input intrinsic noise voltage	$e_n = 2.5nV/\sqrt{Hz}$
Inverting input noise current	$i_i = 14pA/\sqrt{Hz}$

Non-inverting input noise current	$i_{ni} = 3.2pA/\sqrt{Hz}$
Inverting input impedance	$Z_i \simeq 50\Omega$
Nominal feedback transimpedance for maximally flat frequency response	$Z_t = 350\Omega$

Using these numbers, and Equation F in the appendix, a maximum amplifier gain for reduced equivalent input noise voltage may be derived as (this assumes an α of 1/9) $G = 4.3$

Rounding this off to a gain of +4 yields a feedback resistor value of:

$R_f = Z_t - GZ_i = 150\Omega$ **(Eq. D in Appendix)**

Note that taking the gain too high will eventually yield very low R_f values from this equation. For very low values of R_f, a significant degradation in both bandwidth and 3rd order intercept will be observed due to the added output stage loading presented by the feedback network. Generally, $R_f + R_g = 200\Omega$ should be taken as a lower limit to R_f.

Computing the equivalent input noise voltage for $G = 4$ using Eq. E of the appendix yields:

$$e_{ni} = \sqrt{(2.5nV)^2 + [(14pA)(37.5\Omega)]^2 + 16E\text{-}21(37.5\Omega)} = 2.67\frac{nV}{\sqrt{Hz}}$$

As hoped, this total equivalent input noise voltage is nearly equal to the intrinsic noise voltage listed above. From these results, and assuming a 50Ω source impedance, an optimum transformer turns ratio would be

$$n_{opt} = \sqrt{\frac{e_{ni}}{i_n \frac{R_s}{2}}} = \sqrt{\frac{2.67nV}{3.2pA(25\Omega)}} = 5.78$$

This yields a best case noise figure equal to

$$NF_{min} = 10 \log\left(2 + \frac{2.67nV\ (3.2pA)}{4E\text{-}21}\right) = 6.2dB$$

It is, however, difficult to maintain broadband performance through the transformer with a turns ratio this high. For test, a 1:4 turns ratio transformer from Mini-Circuits was selected as a reasonable compromise between best noise figure and broadband performance (part #T16-6T)

The resulting test circuit for the CLC400 is shown in Figure 3.

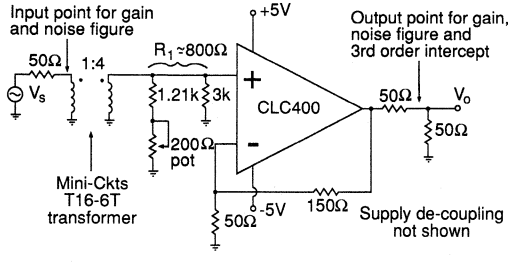


Figure 3

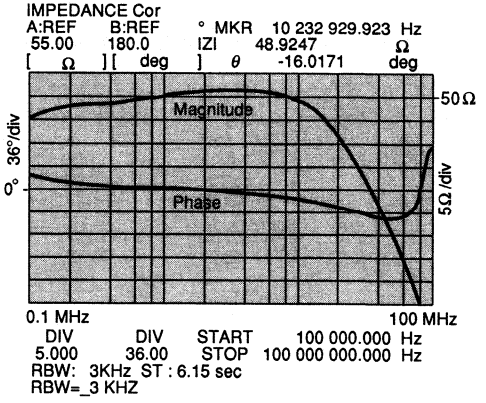
Using this test circuit, the anticipated performance can be calculated to be:

Overall Gain $A_v = 4 \cdot 4 \cdot \frac{1}{2} = +8$ (18dB)

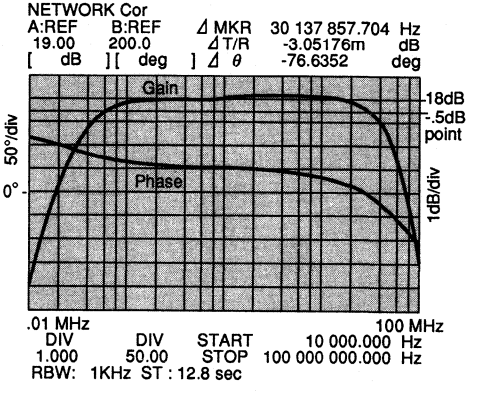
Noise Figure (from Eq. 2)

$$NF = 10 \log\left(2 + \frac{(4\ (3.2pA)\ 25\Omega)^2 + \left(\frac{2.67nV}{4}\right)^2}{(4E\text{-}21)\ (50\Omega)}\right) = 6.8dB$$

In test, the first step was to tune the input impedance matching to provide a good 50Ω match over the frequency range of interest, after which the transfer function (S_{21}) was measured. These results are shown in Figure 4.



Input Impedance
Figure 4a



Transfer Function
Figure 4b

These results show excellent input impedance matching over a broad frequency range with a very flat passband gain from about 60kHz to 30MHz.

The noise figure for this circuit was measured using an HP8970A with an HP346B noise source. Figure 5 tabulates those results along with the 3rd order intercept.

Frequency	Noise Figure	3rd Order Intercept
10MHz	6.8dB	44dBm
20MHz	6.8dB	38dBm
30MHz	7.1dB	33dBm
40MHz	7.4dB	30dBm

Figure 5

The measured noise figure shows excellent agreement with the predicted value, while the 3rd order intercept parallels the CLC400 data sheet plots. Note that the data sheets typically show intercept defined for a power level at the output pin as opposed to the 6dB lower value if defined at the matched load. Adding 6dB to the results shown above gets us back to the data sheet plots. This indicates that the intercept has not been degraded by the transformer input coupling.

Note that the noise figure for just the CLC400, configured as shown in Figure 3 without the transformer, may be derived by simply letting $n=1$ in the noise figure equation (Equation 2). Doing this yields a noise figure of 15.8dB for the CLC400 by itself (assuming only a 50 ohm non-inverting input impedance matching resistor). Hence, the transformer not only provides us with more gain but with greatly improved noise figure.

In summary, this circuit shows a 50 ohm in/50 ohm out, 18dB gain block with very flat frequency response from 60kHz to 30MHz offering an approximate 7dB noise figure with a 3rd order intercept greater than 33dBm over that frequency range, while dissipating only 150mW quiescent power!

Design and Test Results for the CLC401

The CLC401 is a monolithic, DC coupled, wideband current feedback amplifier optimized for higher closed loop gains. Typical specifications show a 150MHz −3dB bandwidth at a gain of +20 using a 1.5k feedback resistor while drawing only 15mA no load current from the specified ±5 volt supplies. Getting the requisite design information from Application Notes OA-12 and OA-13,

Non-inverting input intrinsic noise voltage	$e_n = 2.4nV/\sqrt{Hz}$
Inverting input noise current	$i_i = 17pA/\sqrt{Hz}$
Non-inverting input noise current	$i_{ni} = 2.8pA/\sqrt{Hz}$
Inverting input impedance	$Z_i \simeq 50\Omega$
Nominal feedback transimpedance for maximally flat frequency response	$Z_t = 2.5k\Omega$

Using these numbers, and Eq. F of the Appendix, yields a maximum amplifier gain for minimal equivalent input noise voltage of (assuming $\propto$ of 1/9) G=32.5

Building up the circuit at this gain and using the same transformer as for the CLC400 test circuit resulted in a 3dB response peaking at the higher frequency limits. This seemed to arise from a gain dependent non-inverting input impedance resonating with the transformer. Reducing the amplifier gain ameliorated this effect. Since the amplifier gain was being determined somewhat arbitrarily to reduce the noise figure, backing away from this gain to improve frequency response seemed reasonable. For test, an amplifier gain of G=+25 was selected. Using Eq. E of the appendix shows an equivalent input noise voltage with a gain of +25 given by:

$$e_{ni} = \sqrt{(2.4nV)^2 + [17pA(50\Omega)]^2 + 16E\text{-}21(50)} = 2.70\frac{nV}{\sqrt{Hz}}$$

With this result, an optimum turns ratio for the transformer and a theoretical best noise figure may be calculated to be:

$$n_{opt} = \sqrt{\frac{2.70nV}{(2.8pA)(25\Omega)}} = 6.2$$

and

$$NF_{min} = 10\log\left(2 + \frac{2.70nV\ (2.8pA)}{4E\text{-}21}\right) = 5.9dB$$

Again, the high transformer turns ratio required for optimum noise figure would result in an unnecessarily limited bandwidth. Backing off to a 1:4 turns ratio transformer yielded the test circuit shown in Figure 6.

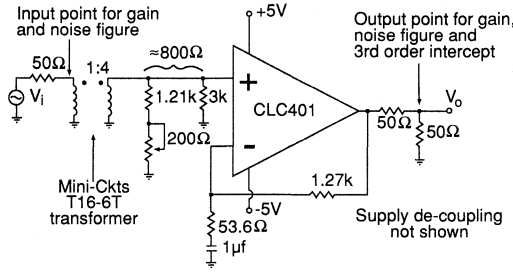


Figure 6

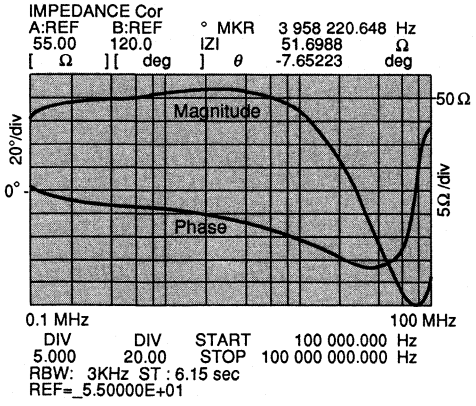
Note that for this test, the amplifier's gain setting resistor has been AC coupled with a 1μf capacitor. This is intended to reduce the DC gain for the amplifier's input offset voltage to 1, holding the output DC as close to 0 as possible. The capacitor value was chosen to yield a transfer function pole well below the transformer low frequency cutoff. The feedback resistor value is set using Equation D of the Appendix. The anticipated mid-band gain and noise figure performance can be calculated to be:

Overall Gain $A_v = 4 \cdot 25 \cdot \frac{1}{2} = +50$ (34dB)

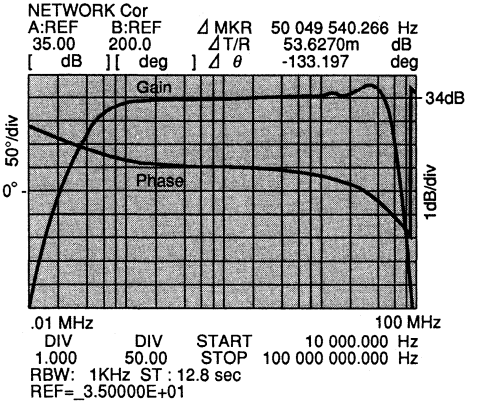
Noise Figure (from Eq. 2)

$$NF = 10\log\left(2 + \frac{(4(2.8pA)\ 25\Omega)^2 + \left(\frac{2.70nV}{4}\right)^2}{4E\text{-}21\ (50\Omega)}\right) = 6.7dB$$

As with the CLC400, the test sequence was to tune the input matching impedance network to yield a good 50 ohm match over as wide a frequency range as possible. After this, the input to output transfer function was measured (S_{21}). Figure 7 show these results:



Input Impedance
Figure 7a



Transfer Function
Figure 7b

This circuit doesn't do quite as well in holding up the input impedance to higher frequencies but it does provide a reasonably flat frequency response from 70kHz to 50MHz (passband with $<\pm.5$dB ripple).

A measure of the noise performance was obtained using an HP3585 spectrum analyzer along with a CLC100 low noise wideband amplifier as a preamp to the analyzer input. Although accurate noise figure measurements are difficult to achieve in this fashion, this approach indicated noise figures between 7 and 8dB. Figure 8 tabulates the measured 3rd order intercept results and this estimated noise figure.

Frequency	Estimated NF	3rd Order Intercept
10MHz	7-8dB	38dBm
20MHz	7-8dB	33dBm
30MHz	7-8dB	29dBm
40MHz	7-8dB	25dBm
50MHz	7-8dB	23dBm

Figure 8

Calculating the noise figure of just the CLC401 without the transformer coupling (by letting n=1 in the noise figure equation) yields 15.9dB for just the amplifier by itself with a 50 ohm non-inverting termination resistor. So, again, the transformer has added signal gain while greatly improving the noise figure.

The results of Figures 7 and 8 show a 50Ω in/50Ω out, 34dB gain block with reasonably flat frequency response from 70kHz to 50MHz offering an approximate 7dB noise figure with 3rd order intercepts greater than 25dBm for operation below 40MHz – dissipating only 150mW! The intercept performance improves rapidly at lower frequencies with continued improvement observed below 10MHz.

Comparisons and Conclusions

Clearly, the transformer coupling offers the potential for some real improvement in noise figures for the amplifiers considered here. Having given up the DC coupling in the process, however, we are now looking to compare these parts to the more classical AC coupled IF amplifiers.

Those parts generally use a Class A output stage as opposed to the Class AB structure used in most of Comlinear's amplifier products. This, along with the high loop gain at lower frequencies, allows exceptional distortion performance to be achieved at a fraction of the quiescent power dissipation vs. the more classical Class A output. This advantage narrows as we move to frequencies over 100MHz with the op amp's loop gain dropping below unity at these higher frequencies.

Generally, for the lower frequency applications, the circuits described here, or similar circuits using different Comlinear amplifiers can offer considerable advantages in the areas of power dissipation, size, and cost.

The transformer coupling offers additional flexibility through potential signal inversion, by reversing the dot convention, output DC shifting, by inserting a DC voltage in place of the ground on the secondary, and potential narrowband filtering. If higher output power levels are desired, this same approach could be used with one of Comlinear's hybrid op amps offering higher supply voltages and greater output power capability. The CLC232, for low gains, and the CLC207 for higher gains, are particularly low harmonic distortion parts that would also benefit, from a noise figure standpoint, from transformer coupling.

This approach to noise figure improvement is applicable to any op amp with an optimum source resistance greater than the actual source resistance. With the total equivalent input noise voltage at the non-inverting input decreasing as the closed loop gain is increased (as shown in the appendix), it is advantageous to operate the op amps at high gains. The current feedback topology, pioneered by Comlinear, is particularly suitable for wideband, high gain applications.

As described in Application Notes 300-1 and OA-13, the current feedback op amp topology largely eliminates the gain-bandwidth performance limitations plaguing earlier voltage feedback designs. Therefore, running the amplifiers to higher gains, in an effort to drive down the non-inverting input voltage noise, will not sacrifice broadband performance as it would using a voltage feedback part.

Acknowledgements
Ralph Carfi, General Electric, Syracuse, N.Y., for measuring the noise figure on the CLC400 test circuit and many useful discussions on this application.

Alan Baker, R&D, Comlinear Corp., for review and discussion of the noise figure equation development.

Steve Smith, R&D, Comlinear Corp., for automating the 3rd order intercept measurement procedure.

References

1. "Current-Feedback Amplifiers," Sergio Franco EDN, Jan. 5, 1989, page 161 (in CLC 1989/1991 Databook). Also, Comlinear Application Note 300-1 and Application Note 0A-14.

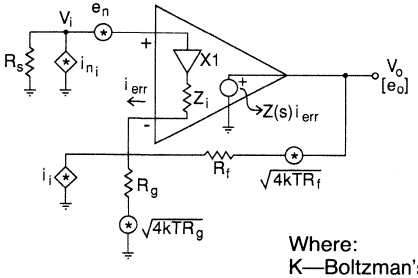
2. "Low-Noise Electronic Design," Motchenbacher and Fitchen; Wiley 1973, pp. 10, 34, and 127.

Appendix:

Computing the equivalent input noise voltage, the gain, and feedback resistor values for noise figure reduction with current feedback op amps.

The equations for determining the equivalent input noise voltage for use in the noise figure calculations will be developed. Since the external resistors around the amplifier, R_f and R_g, play a large role in setting that noise, the amplifiers transfer function, which is also determined by these resistors, will be given and used to set the gain.

Figure A shows the necessary information to develop both the transfer function from V_i to V_o and the equivalent input noise voltage expression. As described in Reference 1, a current feedback amplifier uses a unity gain buffer from the + input to the inverting node, X1, with the inverting node current (i_{err}) acting as the feedback signal sensed and passed on to the output through a transimpedance gain, Z_s.



Where:
K—Boltzman's constant
= 1.38 E−23 J/°K

T—degrees Kelvin
290°K used here

Figure A

The goal here is to develop an equivalent non-inverting input noise voltage source to place at the non-inverting input for noise figure calculations. Normally, a noise generator for the non-inverting termination resistor would be included in this analysis. In the context of using an input transformer coupling, however, this resistor will be set by impedance matching concerns removing it as a variable for equivalent input noise voltage reduction. The effect of this resistor's noise is included in the development for noise figure. The 3 noise sources on the inverting side of the circuit must be reflected to the non-inverting side and combined with the intrinsic noise voltage, e_{ni}, already present in the model. Neglecting i_{ni}, which is left separate for later use in the noise figure equations, each noise voltage or current will develop an output voltage noise. With the non-inverting signal gain defined to be $G = (1 + R_f/R_g)$, the separate output noise voltages are:

intrinsic non-inverting input noise voltage $\rightarrow e_n\ G$

inverting input noise current $\rightarrow i_i\ R_f$

combined resistor noise terms $\rightarrow \sqrt{4KTR_fG}$

Combining terms as the root sum of squared elements, and reflecting this to the non-inverting input yields

equivalent input noise voltage $\rightarrow \sqrt{(e_n)^2 + \left(\frac{i_i R_f}{G}\right)^2 + \frac{4KTR_f}{G}}$ **Eq. C**

As is apparent from this expression, both the gain and the resistor values can be used to reduce the input noise voltage. Increasing the gain and/or reducing the resistor values will both decrease the apparent input noise voltage. This effort is bounded by the intrinsic input noise voltage, e_{ni}.

Setting the gain and the resistor values needs to be done in the context of maintaining adequate phase margin for the closed loop amplifier response. Analyzing the circuit of Figure A for the V_o/V_i transfer function yields (see Application Note OA-13 for a more complete development);

$$\frac{V_o}{V_i} = \frac{1+R_f/R_G}{1+\frac{R_f + Z_i(1+R_f/R_G)}{Z_{(s)}}} = \frac{G}{1+\frac{R_f + GZ_i}{Z_{(s)}}}$$

where: $Z_{(s)} \rightarrow$ Forward transimpedance gain of the amplifier (frequency dependent)

$Z_i \rightarrow$ Inverting input impedance (Considered noiseless and real)

The inverting node current is the feedback signal with an output voltage to inverting input current transfer gain given by $Z_t \equiv R_f + Z_iG$

Every current feedback amplifier has an internal forward transimpedance gain function ($Z_{(s)}$) optimized for a certain value of Z_t. Typically, this optimization yields a 60° phase margin at the gain and feedback resistor value specified on the data sheet for guaranteed performance specs. To a first approximation, this Z_t can be held constant (maintaining maximum closed loop bandwidth with no peaking) as the desired closed loop signal gain is changed from the nominal design point. This is done by adjusting R_f vs gain. Solving for this from the above expression for Z_t yields:

$R_f = Z_t - Z_iG$ **Eq. D**

If this expression for R_f is placed into the equivalent input noise expression developed above, Eq. C, we get:

$$e_{ni} = \sqrt{(e_{n_i})^2 + i_i^2\left(\frac{Z_t}{G} - Z_i\right)^2 + 4KT\left(\frac{Z_t}{G} - Z_i\right)} \qquad \textbf{Eq. E}$$

The only variable left at this point is the desired closed loop gain. The absolute resistor values have been removed with the assumption that a maximally flat frequency response is desired as the closed loop gain is changed. Again we see that increasing the gain will decrease the equivalent input noise voltage. This approach is decreasingly effective as those terms involving G become less than the non-inverting input noise voltage e_{ni}. If we target a desired ratio of the two squared terms involving G to the intrinsic non-inverting input noise voltage squared, we can develop a targeted maximum gain beyond which minimal noise reduction is achieved through further gain increases. If we call that ratio of the noise powers $\propto$ we can solve for:

$$\left(\frac{Z_t}{G} - Z_i\right) = \frac{2KT}{i_i^2}\left[\sqrt{1 + \propto\left(\frac{e_n\, i_i}{2KT}\right)^2} - 1\right] \qquad \textbf{Eq. F}$$

From this expression, and a knowledge of Z_t and Z_i, a maximum desired gain may be derived. This yields a somewhat arbitrary upper limit on amplifer gain in that we are only trying to increase the gain until negligible improvements in the noise figure are seen. The amplifier can, of course, be operated at lower gains, with an increase in noise, or at higher gains, with little noise improvement but an eventual bandwidth limitation. If we set $\propto$ to be 1/9 (saying that the reflected equivalent noise power terms at the non-inverting input are 1/9 the intrinsic input noise power due to the non-inverting input noise voltage) those terms increase the equivalent input noise voltage by only 5%. This will be the initial targeted design criteria used in the example developments.

See Application Note OA-13 for a complete development of adjusting R_f to hold a constant loop gain, and hence bandwidth, as the desired signal gain is changed.

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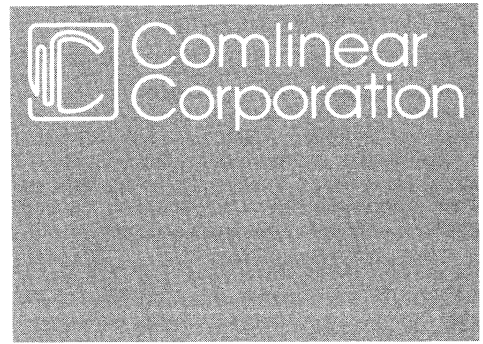
APPLICATION NOTE OA-15

Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers

Michael Steffes

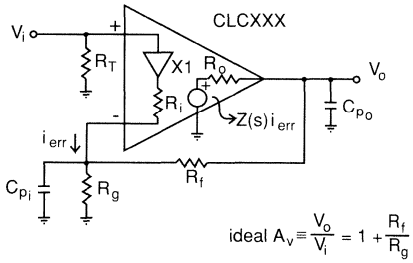


As op amp operating speeds have moved to ever higher frequencies, a whole new set of design concerns have come into play for linear op amp applications. With the development of the current feedback topology, design concerns unique to that topology must also be considered if optimal performance is to be achieved from devices offering over 200MHz −3dB bandwidths. This discussion will review some of the considerations common to all wideband linear op amp applications as well as topics unique to the current feedback topology pioneered by Comlinear Corporation. These design guidelines are intended to help the designer get the full potential out of Comlinear's high performance, current feedback, operational amplifiers.

Since there are quite disparate areas to consider here, the approximate order of discussion will follow a perceived frequency of occurrence ranking. Those considered first seem to impact every designer, with more particular concerns dealt with later.

1. **Parasitic capacitance effects and what to do about ground and power planes in a PC board layout.**

The sensitivity of the Comlinear amplifiers to parasitic capacitance arises solely from their wide bandwidth characteristics and not from the current feedback aspect of their design. With parts showing a loop gain that does not drop to unity until the 100MHz region, a few picofarad capacitance to ground in the loop can have a profound effect on the phase margin at the unity gain crossover frequency. Figure 1 shows a typical non-inverting gain op amp, including the internal structure for the current feedback topology (note 1), along with the two most critical external parasitic capacitances.



Most critical parasitic capacitances
C_{po} → output capacitance
C_{pi} → inverting input capacitance

Figure 1: Non-inverting gain with internal current feedback topology

Note 1: See application note AN, AN-300, or OA-13 for a development of the current feedback transfer function.

Parasitic, or loading, capacitance directly on the output is particularly effective at transforming amplifiers into oscillators. Closed loop stability for any negative feedback amplifier is determined by the open loop phase margin. In tracing the signal around the loop it is always desirable to have significantly less than 180 degrees phase shift around the loop at the unity gain crossover frequency. Adding a capacitor directly on the output will cause additional signal phase shift due to the additionally pole introduced by the open loop output impedance, R_o, driving the output pin capacitance, C_{po}. Even small capacitances and low R_o's can cause significant phase shifts with unity gain crossovers in the 100MHz region (a typical unity gain crossover frequency for Comlinear amplifiers).

Several design and test guidelines can be suggested to keep this sensitivity to C_{po} under control.

a. Always clear ground and power planes away from the output pin net. This includes opening up a little wider than standard clearance to ground and power inner planes to any through hole or trace carrying the output signal.
b. Never probe directly with a high impedance probe or a DVM on the output pin (passive divider probes are okay). If probing, always probe through a series resistor >= 100Ω since this will decouple the effect of the probe capacitance from the output pin. This also holds for adding PC board test points. If needed, connect the test points through a series resistor located as close as possible to the device pin being brought out.
c. If a capacitive load must be driven, such as flash ADC's, most of the Comlinear amplifier data sheets include a plot of a recommended series resistor to put at the output prior to the load capacitance. Adding a resistor prior to the load (or parasitic) capacitance, changes the load's effect from a pole to a pole-zero pair. This causes a phase dip in the loop phase response that has recovered prior to unity gain crossover.
d. Driving into another amplifier stage, or actually almost any other high input impedance active device, can also present enough capacitance to cause problems. Again, a small series resistor right at the output prior to going off to this device will defuse the situation.

Figure 2 shows the effect of an output capacitance on the small signal frequency response of the CLC205, a hybrid current feedback op amp intended for higher gains. The plot shows the SPICE simulated gain, in dB, vs. linear frequency under several loading conditions. Similar plots may be generated using the small signal macromodels of Application Note OA-09. Initially, a 200Ω load is driven, then just a 20pF load, and finally, the 20pF load with a series 30Ω resistor (R_s in Figure 2a). Clearly, getting into a series resistor prior to the capacitive load can dramatically improve the frequency response flatness, and hence pulse response capabilities for the amplifier simulated here. Recall that this approach is applicable for both current and voltage feedback amplifiers.

Generally, it is suggested to get the output voltage through a resistor as soon as possible before running it over any significant length of trace or cable. If a matched impedance load is to be driven, source match right at the output pin with a discrete resistor equal to the transmission line's characteristic impedance, and terminate the line similarly. Although short trace runs do not need to be impedance matched, using just the series resistor will isolate the trace capacitance when

no terminating resistor is used.

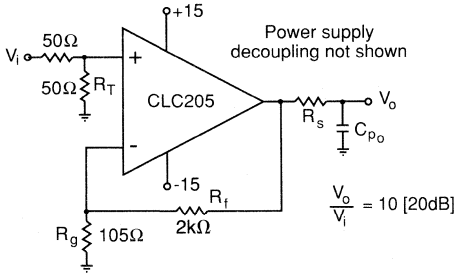


Figure 2a: Simulation circuit for capacitive loading test

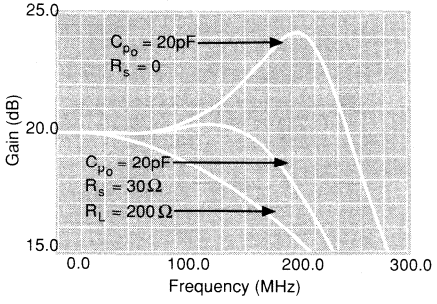


Figure 2b: Frequency response for various loadings

Parasitic capacitance on the inverting node is a considerably more complex, but not nearly as troublesome, phenomena. Capacitance on this input affects both the non-inverting signal gain, by appearing in shunt with the gain setting resistor, and the loop gain phase margin in a 2nd order sense. Two types of pulse response characteristics can be observed due to this parasitic. If the dominant effect is simply shunting R_g in the ideal gain expression, neglecting loop gain effects for now, a single overshoot with a decay will be observed. If this capacitance is large enough to effect the phase margin, considerable ringing in the pulse response will also be observed.

Again, minimize ground and power planes around the inverting node net. The single overshoot and decay will most often be observed when a current feedback part intended for higher gains, and hence designed to use a relatively high feedback resistor value, is used at low non-inverting gains. The relatively high R_g required to get a low non-inverting gain will bring the impact of whatever parasitic is present down in frequency into the passband of the amplifier. The solution here, beyond simply limiting C_{pi}, is to run inverting mode if possible, or switch to a part intended for lower gain operation, and hence designed to use lower resistor values. Given a fixed C_{pi}, operating with lower R_f and R_g will move the zero frequency out beyond the amplifier passband. Application Note OA-14 discusses in more detail the gain range considerations for current feedback amplifiers.

Figure 3 shows a test circuit and simulation results demonstrating the effect of inverting node capacitance for the CLC205 operated at relatively low non-inverting gain.

The effect of increasing C_{pi} from .5pF to 5pF in the circuit of Figure 3a can be seen as a considerable peaking in the frequency response of Figure 3b. This is not, in this case, a loss of phase margin peaking, but simply a zero coming into the non-inverting transfer function due to C_{pi} shunting R_g. This zero frequency is at $(C_{pi} \bullet (R_g || R_f) / (2 \bullet pi))$ Hz. Note in the pulse response of Figure 3c that C_{pi} causes a single overshoot with negligible ringing.

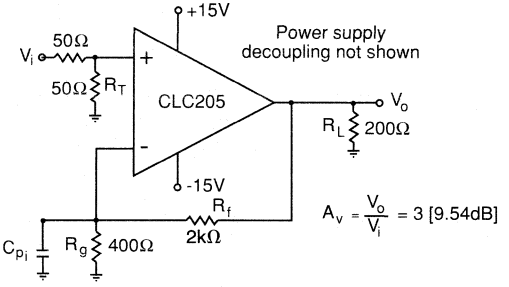


Figure 3a: Simulation circuit for inverting input capacitive test

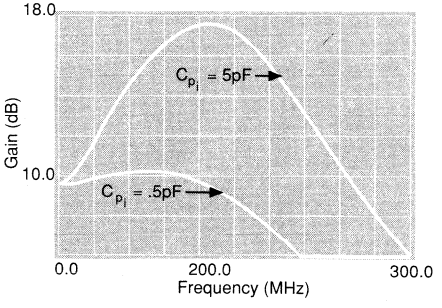


Figure 3b: Frequency response vs. C_{pi}

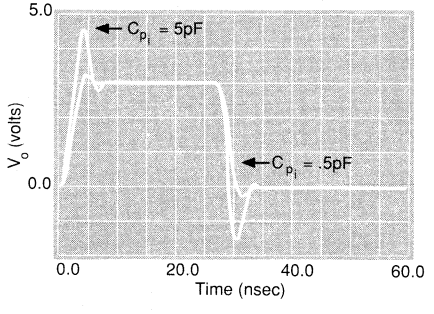


Figure 3c: Pulse response vs. C_{pi}

If ringing is observed in the pulse response, this is more likely due to capacitance on the output pin. However, larger parasitic capacitances on the inverting node (>10pF) can also cause loop gain phase margin problems, particularly for parts intended for high gains. Again, the discussion about avoiding parasitic capacitances on the output pin applies equally well here. Figure 4 shows the difference in pulse response behavior between C_{po} and C_{pi} effects. The upper trace, which was plotted with a 1V offset for clarity, shows the ringing pulse response for the most peaked response of Figure 2b. This is typical of output pin capacitance effects. The lower trace is a repeat of the $C_{pi}=5pF$ pulse response of Figure 3c.

Parasitic capacitance to an AC ground on the non-inverting input, including the capacitance of the high impedance non-inverting input itself, will generally only introduce an additional response pole, depending on the source impedance driving the input capacitance. For low source impedances, this pole comes in well beyond the passband of the amplifier. However, when the parasitic capacitance on the non-inverting and inverting nodes are approximately equal, intentionally adding non-inverting source impedance equal to $R_g||R_f$ can be very effective at cancelling the response zero coming in through C_{pi} shunting R_g.

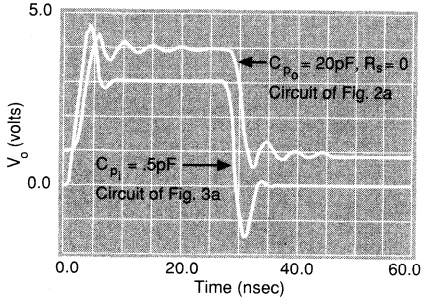


Figure 4: Contrasting pulse responses for C_{po} and C_{pi}

Figure 5 shows this approach with the $C_{pi}=5pf$ case considered earlier in Figure 3. Note that we have intentionally matched the capacitance at the non-inverting input and added $R_{ni}=300$ to bring the frequency response back to flatness. The signal gain is not changed by the addition of R_p. This . approach simply cancels the zero apparent in the upper trace of Figure 5b, significantly decreasing the pulse overshoot as shown in Figure 5c.

Although it is critical to remove ground plane from the signal input and output nodes, a good, low inductance, ground return path must be provided for the AC load current. This is typically provided by putting small-valued ceramic capacitors directly on the power supplies, connected to a good adjacent ground plane. These conflicting goals of good power supply grounding with no parasitic capacitance on the I/O pins can be achieved by opening a window around the part for the

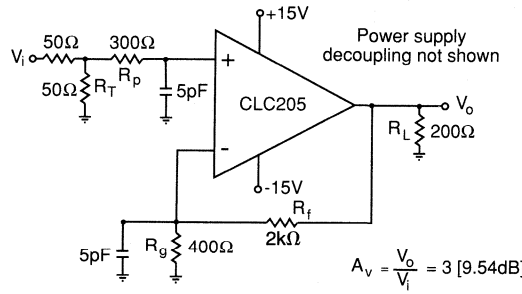


Figure 5a: Simulation circuit of C_{pi} peaking cancellation

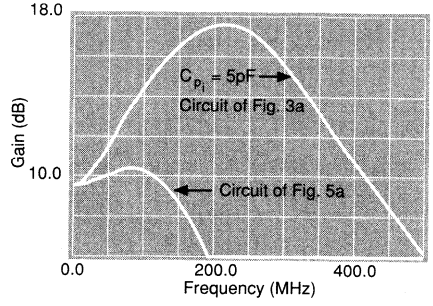


Figure 5b: Frequency response demonstrating zero cancellation

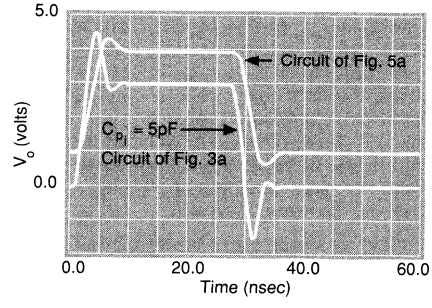


Figure 5c: Pulse response with zero cancellation

ground and power planes with the high frequency decoupling capacitors connecting into this ground plane. The layout drawing of the 730013 evaluation board (in the product accessories section of the catalog), shows a good high frequency layout for the 8-pin DIP monolithic amplifier products offered by Comlinear.

Figure 6 shows the same amplifier as Figure 1 with the suggestions for handling parasitic capacitances incorporated.

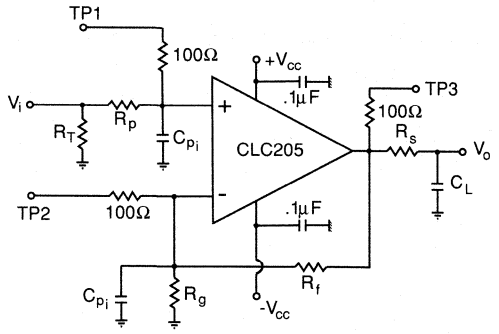


Figure 6: Non-inverting amplifier featuring several suggested protections from parasitic capacitance effects

The circuit of Figure 6 includes every fix for the possible problems arising from parasitic capacitance discussed thus far. Very rarely would all of these be required for the same application. If test points are to be brought out, always come out through at least 100Ω resistors with the body of those resistors as close as possible to the amplifier pins. Probing at these test points can still radically alter the signal path frequency response. The amplifier should, however, remain stable with at least 100Ω isolating resistors. If inverting node parasitic capacitance seems to be a problem, R_p can be very effective at cancelling it out (except when C_{pi} is so large as to cause phase margin problems). If a parasitic or load capacitance must be driven, R_s may be used very effectively to improve the frequency response flatness. And, always get the high frequency capacitors on the power supplies as close to the part as possible into a good ground plane.

2. **The importance of the feedback resistor**
The feedback resistor value becomes of paramount importance in the current feedback topology used by most of the Comlinear amplifiers. As discussed in detail in Application Note OA-14, the feedback resistor is the single most important element in setting the overall frequency response for the current feedback amplifier topology. Briefly, since we are looking for a feedback current from the output voltage to the inverting input, the feedback impedance plays the dominant role in determining what this will be. This, in turn, will determine the amplifier's loop gain and phase margin. Achieving adequate phase margin is critical to the success of any operational amplifier application.

Every current feedback amplifier is optimized for a particular value of feedback resistor. This value is typically noted at the heading of the specifications listing. Always select a value near this as the starting point for any design. Lower values may be used at the risk of lower phase margin and greater frequency response peaking. Higher values may be used at the expense of lower amplifier bandwidth. In fact, increasing the feedback resistor value is a very effective means of overcompensating the amplifier. Unlike voltage feedback amplifiers, a unity gain follower application requires the recommended feedback resistor to be in place from the output to the inverting input. Although having no influence on the low frequency signal gain in the unity follower application, the feedback element is still needed to determine the loop gain for the current feedback topology.

Using reactive elements in the feedback path, either intentionally or unintentionally, can play havoc with the loop gain phase margin. Generally, this should be avoided unless done with extreme care. The small signal macromodels in Application Note OA-9 are very useful for predicting what will happen with different feedback configurations. Using direct capacitive feedback, to implement an integrator, will generally cause oscillations with a current feedback amplifier. Integrators can be implemented, however, using the alternative topologies shown in Application Note OA-7. Also, the CLC420, a wideband voltage feedback op amp, can be used to implement classical integrator topologies.

Returning to the feedback resistor itself, never use a wirewound type for this, or any other, resistor in a broadband application. Also, trying to compensate the amplifier by using shunt capacitance across R_f will typically yield oscillations with the current feedback topology. It is much more fruitful to compensate by increasing the value of the feedback resistor, although a pot in the feedback path is not recommended.

3. **Non-inverting source impedance considerations**
The impedance seen looking out of the non-inverting input can play a strong role in determining an amplifier's overall performance. For very broadband applications, significant resistive source impedance, in conjunction with the part's input capacitance, can become the bandlimiting point in the system. This is normally not a problem for 50Ω terminations driven from a 50Ω source.

When running the amplifier in inverting mode, the non-inverting input would typically be grounded, either directly, or through an approximately 25Ω resistor. No attempt at source impedance matching on the two inputs for bias current cancellation should be made since the two bias currents for a current feedback amplifier are totally unrelated in both magnitude and polarity. Hence, unlike a voltage feedback op amp, there is no meaning to an offset current specification.

Generally, taking the non-inverting input to ground through a 25Ω resistor (for inverting amplifier applications) will eliminate any oscillations that might be seen due to negative input impedance effects at very high frequencies for the non-inverting input. It is oftentimes sufficient to simply ground the non-inverting input. But a careful check for low level oscillations above 500MHz should be made, particularly for the faster amplifiers, if direct grounding is desired. If oscillations are observed, going to a 25Ω, or higher, resistor to ground will kill this self oscillation in the non-inverting input transistors.

When it is desired to AC couple the non-inverting input signal, as shown in Figure 7, particular attention must be paid to the effect the terminating resistor has on the DC operating point of the amplifier. Oftentimes, in an effort to achieve very low pole frequencies for the AC coupling (without an inordinately large coupling capacitor, C_t), R_t is made very large or, in some cases, not included.

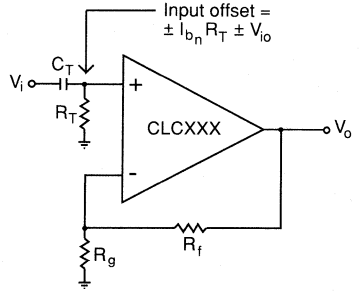


Figure 7: Effect of R_t on DC input offset voltage

R_t, however, provides the DC current path for the non-inverting input bias current. Wideband amplifiers with a purely bipolar construction, as Comlinear's amplifiers typically are, have an input bias current ranging into the 10's of μA's. It is critical, therefore, to consider the effect a large R_t has on the input offset voltage (as shown in Figure 7). It is very easy, with large R_t, for this bias current requirement to have driven the input and output into saturation precluding proper high frequency operation. The effect of high R_t on the non-inverting noise current gain should also be considered. This noise current will add as an input noise voltage term dependent on the frequency dependent source impedance looking back out the non-inverting input.

4. **Input and output voltage range considerations**
The common mode input voltage range specification (CMIR) shown in the Comlinear data sheets indicates how near the specified supply voltages the non-inverting input voltage may be for proper operation. When operating properly, the inverting node voltage simply follows the non-inverting even for differential amp applications. For current feedback, this is due to the unity gain buffer from V+ to V−, while for voltage feedback, this is due the feedback loop.

Since all of the amplifiers are specified with balanced bipolar supply voltages, the CMIR and output voltage ranges are given as an allowed bipolar swing around ground. Both specifications are, however, indicating the required voltage headroom to the supplies on the non-inverting input and output pins respectively. Recasting these specifications as a required voltage headroom would allow input and output voltage ranges to be set for non-standard supply voltages.

In almost all cases, the maximum output voltage swing will be the limiting factor. Only at very low non-inverting gains, or for single amplifier differential operation, will the CMIR limit operation. The crossover non-inverting gain where the limiting point will change from input to output can be found by dividing the output voltage range by the input voltage range.

Operation that can cause the amplifier to exceed its output voltage range should be handled with special caution. Except for devices including an output limiting or clamping function (CLC500, CLC501, CLC502), exceeding the output voltage range will result in saturation internal to the amplifier. In all cases, this will result in very slow recovery time from overdrive. Since the error signal, for current feedback, is a current back to the inverting input, saturating the output voltage so that it no longer fully supplies the current being set up in the gain setting resistor will cause a current to build up in the inverting input. This is analogous to a voltage developing across the inputs of a voltage feedback amplifier when overdriven. This inverting input current can also limit recovery time from saturation effects internal to the amplifier.

All of the monolithic amplifiers from Comlinear can handle this saturation without damage. Extreme overdrives at the inputs can, however, exceed the current handling capability of the inverting node at which point a voltage will start to build across the inputs. This can, if large enough, break down some internal junctions leading to an increase in noise and possibly a shift in the DC characteristics of the amplifier.

Unless specifically indicated as overdrive protected (CLC205, CLC206, CLC207, CLC560, CLC561), special care should be taken not to drive any of the hybrid amplifiers into output saturation. Intended for the widest band, high power operation, these parts have enough internal drive capability to potentially damage themselves under a saturated output condition. Although not noted in the data sheets, the CLC231 and CLC232 low gain hybrid amplifiers can also be output stage saturated without damage. Even with an output saturable capability, all of the hybrid amplifiers need a careful analysis of junction temperatures to ensure that they do not exceed the rated maximum of 175°C.

From these considerations, it is not recommended that these unprotected hybrid amps be used as comparators – with the output intentionally forced from supply rail to supply rail. (The fast recovery clamping of the CLC501 does, however, offer an excellent opportunity for a very flexible high speed comparator function.) It is also not recommended to increase the value of the output stage collector resistors, for those parts bringing the output transistor collectors out separately, to act as a current limit since this will only saturate the output stage sooner. Generally, these resistors are intended only to de-couple high speed load current transients from the rest of the amplifier to enhance high speed settling times. It is possible, however, to use these resistors as an output short ckt current limit for those parts indicated as being overdrive protected. And finally, when using adjustable gain circuits, particularly with switching FETs, take care to keep the amplifiers out of an open loop situation during gain adjust.

For situations requiring a robust output overdrive capability, the clamping amplifiers are by far the best choice.

5. **Cascaded amplifier considerations**
High gain, cascaded amplifier applications require particular attention to a number of parasitic and operational effects. Figure 8 shows an example circuit of 3-CLC401's configured for an overall gain of 1000 (60dB) that will be used to demonstrate the suggestions developed here.

Several opportunities exist to develop an oscillator with very high gain, wideband circuits. The most common

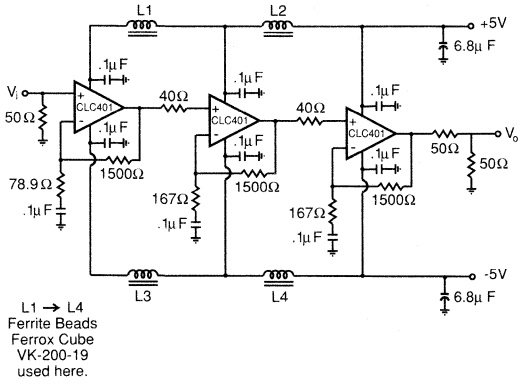


Figure 8: Wideband, high gain, cascaded amplifiers

is direct output to input parasitic coupling. The output signal path should be physically isolated and, if necessary, shielded from the input signal path. When the final output is driving a relatively heavy AC load, either capacitive or, in this case, resistive (100Ω), high frequency load currents through the supplies can couple back into early stages completing an oscillatory feedback loop. High frequency de-coupling directly on the supply pins of each stage are required at a minimum.

Interstage ferrite beads on the supply rails, as shown in Figure 8, can also be used to attenuate this feedback path. The power supply connections of Figure 8 bring in the supplies at the final gain stage with LC PI filter stages used as it connects into earlier amplifier stages.

This provides increasing high frequency attenuation as we go to amplifier stages earlier on in the gain path. This is very desirable from both a PSRR standpoint and in breaking any feedback path through the power supplies from the output to input.

For close physically coupled amplifier stages, interstage matched impedances are probably not necessary. The two interstage 40Ω resistors of Figure 8 are intended to isolate the input capacitance of the next stage from the output of the previous stage as suggested earlier in the discussion of parasitic load capacitance effects.

One key concern in a very high gain path is the build-up of DC errors. The circuit of Figure 8 AC couples the gain setting resistors which reduces the DC gain to 1 for each amplifier stage. With only 1mV input offset voltage at the first stage, the final amplifier output, (prior to the 6dB matching loss), would be at 2V for this gain of 2000 if the 1µF capacitors had not been used in the gain setting networks. If DC coupling at high gains is desired, some sort of composite correction loop (as described in Application Note OA-07) should be considered.

As a general rule, the highest gain stage should be used as the first stage to limit the impact on the overall input noise of the noise contribution of succeeding stages. Here, the equivalent input noise of the 2nd two stages would be divided by the gain of +20 in the first stage in adding to overall equivalent input noise. The total equivalent input noise for the circuit of Figure 8 is $3nV/\sqrt{Hz}$. See Application Notes OA-12 for a noise calculation discussion and OA-14 for reducing the input noise for AC coupled applications.

Figure 9 shows the measured broadband gain and phase response for the circuit of Figure 8. Note that the measured −3dB bandwidth, extending from 3KHz to 200MHz, achieves an equivalent 200GHz Gain-Bandwidth product.

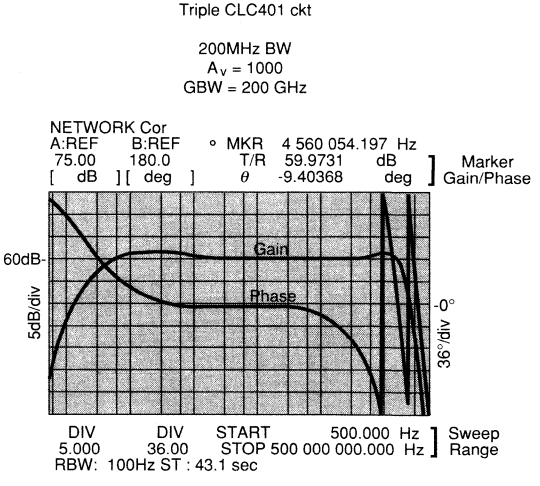


Figure 9: Measured Gain & Phase for high gain cascaded circuit

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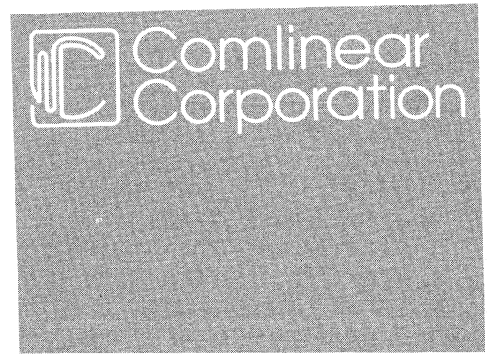
Application Note OA-16

Wideband AGC Amplifier Doubles as a Differential Amplifier

Michael Steffes



The CLC520 is a very flexible DC-coupled Automatic Gain Control amplifier (AGC). Unique features include two closely-matched differential inputs, a wideband gain-control channel (100 MHz), and a ground-referenced DC-coupled output signal driven from a low output impedance amplifier. Figure 1 illustrates the internal block diagram and pin assignments of the CLC520.

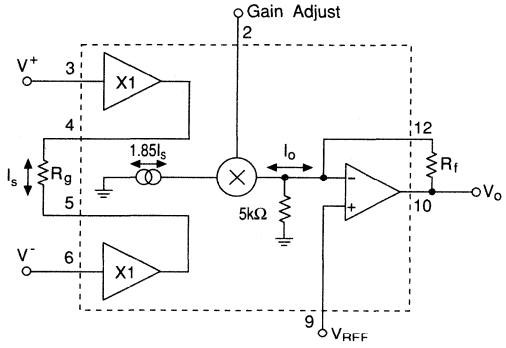


Figure 1: CLC520 Internal block diagram

As shown in figure 1, two unity-gain closed-loop input buffers on pins 3 and 6 are used to force the two input voltages to appear across the external resistor, R_g. The differential voltage across R_g generates a signal current which is amplified by a factor of 1.85 and fed into a two-quadrant multiplier stage. The gain-adjustment voltage on pin 2 determines how much of this signal current makes it through the multiplier stage, with the remainder of the signal current being shunted to ground. The multiplier's output current then flows through the transimpedance amplifier formed by the external feedback resistor, R_f, and the internal amplifier. If the non-inverting input of this output amplifier, V_{ref}, is tied to ground then a ground-referenced DC-coupled replica of the differential voltage across R_g appears at the output of the op amp. The values of R_f and R_g, along with the gain-adjust voltage, determine the gain. Refer to the CLC520 data sheet for a more complete operational and performance discussion.

In order to implement a fixed-gain differential amplifier, the CLC520 will rely on it's very well-matched input buffers and it's differential-to-single-ended voltage conversion. For the purposes of this discussion, the gain-control input will be held at a fixed level to yield the maximum gain given by $1.85 \cdot R_f/R_g$. Thus, the differential signal gain depends only on the ratio of two external resistors and the internal current-mirror gain. Both R_f and R_g can be adjusted to yield a wide range of differential gains. As an example, the circuit of figure 2 is used to demonstrate the performance of the CLC520 in a fixed-gain differential amplifier configuration.
To demonstrate this application, the CLC520 is set up for a gain of 4.08V/V. The 50Ω impedance-matching

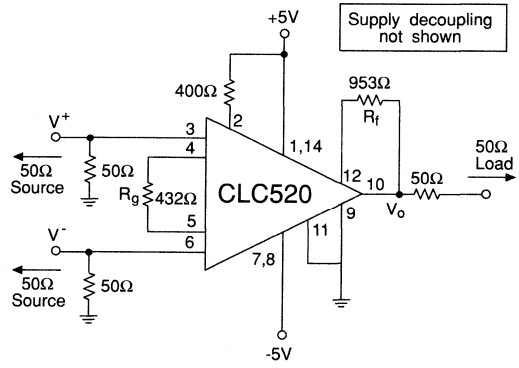


Figure 2: CLC520 Fixed-gain differential amplifier configuration

resistor at the output effectively halves the differential gain to 2.04V/V (6.2dB) at the 50Ω load. Figure 3 shows the single-ended gain and phase response for both inputs on a linear frequency scale through 200MHz. Note the 180° phase offset for the inverting-signal gain, indicating signal inversion. The slightly quicker roll-off of the inverting-gain response is consistent from part to part. This broadband performance is maintained as the part is operated at higher gain settings. It is the close, broadband, gain match of the inputs that allows the CLC520 to provide this wideband differential amplifier with very good common-mode signal rejection.

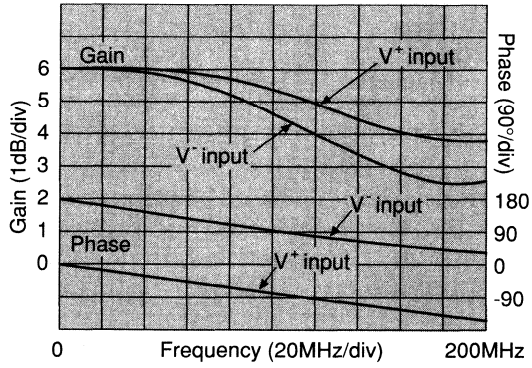


Figure 3: Single-ended gain and phase

One measure of a good differential amplifier is its ability to reject common-mode signals. The common approach in describing this rejection is as a Common Mode Rejection Ratio (CMRR). The definition of CMRR is structured to allow the common-mode input signal to be placed in series with one of the differential inputs, (divided by CMRR), as an equivalent error term. With the following definition of CMRR, an equivalent input error term is placed at one of the inputs as shown in figure 4.

Ad: Differential gain
Ac: Common-mode gain

$$CMRR \equiv \frac{Ad}{Ac}$$

$$CMRR = 20\log(Ad) - 20\log(Ac) \qquad \textbf{Eq. 1}$$

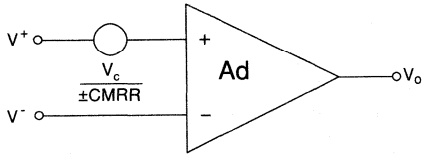


Figure 4: Input-referred common mode error model

V^+, V^-: pure differential signals
Vc: common mode signal element

$$V_O = Ad(V^+ - V^-) \pm \frac{V_C}{CMRR} Ad$$

$$= Ad(V^+ - V^-) \pm \frac{V_C}{Ad / Ac} Ad$$

$$= Ad(V^+ - V^-) \pm VcAc$$

This definition of CMRR essentially input refers an output signal due to a common-mode input signal which effectively holds the common-mode gain constant as the differential gain is changed. In computing the actual input-to-output signal gain due to a common-mode input voltage, simply use Ac. Note, with Ac<<1, the logarithmic form of CMRR yields a large positive value. However, in computing the output common-mode signal, as shown in figure 4, a linear (Volts/Volts) gain must be used and the error must be considered bipolar.

To measure the CMRR as defined in figure 4, a measure of the pure differential gain must first be made. This measurement can be accomplished with the circuit of figure 5. This circuit uses a transformer with a center-tapped secondary to generate a pure differential input signal. The center tap also provides a DC path to ground supplying a DC-bias current to each of the inputs. It is necessary, in all cases, to carefully consider the source of these DC-bias currents. The transformer's frequency response was normalized prior to the gain and phase response measurement. Although using this transformer effectively AC couples the differential gain, it is important to recognize that the CLC520 is a truly DC-coupled device.

The measured gain and phase for the circuit of figure 5 are shown in figure 6. In order to maintain compatibility with the common-mode gain measurement, this figure is represented with a logarithmic frequency sweep from 100kHz to 100MHz. This circuit offers an exceptional gain-flatness with only 0.5dB rolloff to 100MHz.

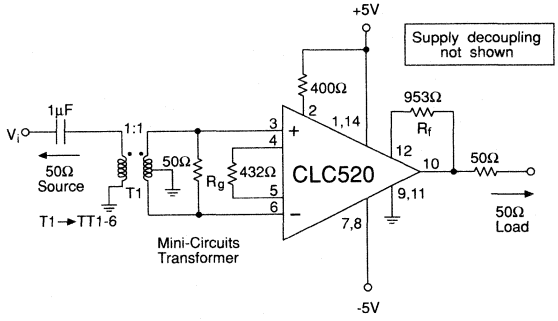


Figure 5: Differential gain test circuit

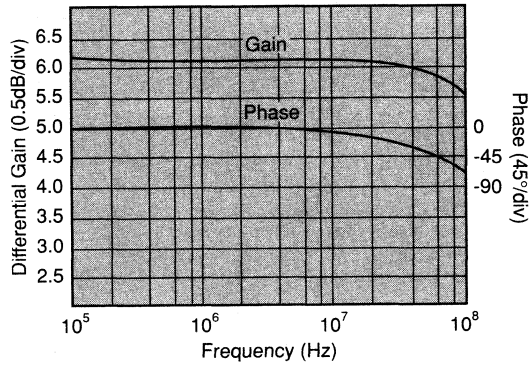


Figure 6: Differential gain and phase

The common-mode gain is measured by replacing each of the 50Ω input resistors of figure 2 with 100Ω while connecting the two inputs together. Tying the inputs together forces the input signals to be exactly the same while the resistor replacement retains the 50Ω input-impedance match. In an actual application, connecting the two inputs together is impractical. In most cases the common-mode gain is not set by the amplifier, but by the mismatch of signal attenuations arising from each signal-source's impedance into the single-ended input impedance of each of the differential amplifier's inputs. A careful attention to the signal-source impedance match is necessary in order for the CMRR performance to be dominated by the amplifier and not by the deleterious effects of signal-source impedance mismatches. The common-mode gain measurement made here sidesteps those issues by simply tying the two inputs together. Figure 7 shows the CMRR using the measured differential gain, the measured common-mode gain and the logarithmic form of CMRR (Eq.1).

The upper limit of CMRR at low-frequencies (below 100kHz) is approximately 70dB. This limit is set by the differential-to-single-ended conversion that takes place internal to the CLC520 . At higher frequencies, the

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divergence in single-ended gains results in a 40dB rolloff of CMRR at 10MHz (shown in figure 3). The CLC520's two high-impedance inputs with its internal wideband differential-to-single ended conversion combine to form a very wideband, high CMRR, differential amplifier.

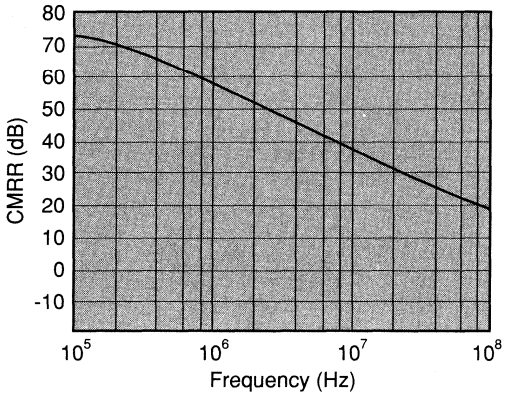


Figure 7: Common-mode rejection ratio of the circuit in figure 2

Application Hints:

I. Improving CMRR

Several elements combine to set the frequency response of the CLC520. On the input side, parasitic capacitance to ground on either of the buffer outputs (pins 4 & 5) can cause high-frequency peaking. It is essential to keep the PC trace capacitance small and balanced when connecting R_g. For the tests shown here, R_g was soldered directly across the pins of the DIP while those pins were lifted from the board. On the output side, R_f will determine the frequency response of the output amplifier. Since this amplifier uses the current-feedback topology, R_f is the dominant element determining its frequency response. Increasing the value of R_f can be used to roll-off any peaking caused by parasitic capacitance on the output of the input buffers. However, it is preferable (from a noise standpoint) to minimize this parasitic on pins 4 & 5 and use lower values of R_f (and therefore lower values of R_g for any particular gain). The CLC520 is designed for use with a 1kΩ feedback resistor. Decreasing this value will cause the frequency response to peak, while increasing it will roll the response off. Most designs should start by first selecting a value for R_f and then determine the required R_g using the design equations found in the CLC520 data sheet. An additional constraint on lower values of R_g for good linear operation is that the maximum current supplied by the buffers through R_g should be kept within ±1.35mA. This will set a maximum differential input voltage based on this current limit and the value of R_g.

Once the parasitic capacitance to ground on pins 4 & 5 has been minimized, a frequency response similar to that shown in figure 3 can be achieved for each of the two inputs separately. It is possible to take advantage of a parasitic gain imbalance in order to bring the inverting gain, at higher frequencies, into a closer match with the non-inverting gain. A closer gain match over a wider frequency range will improve the CMRR at high frequencies.

Although the equivalent circuit of figure 1 shows an output that depends only on the current through R_g, any additional current driven in to or out of the buffers will also generate an output signal. Therefore, by adding an AC coupled path to ground on the output of the inverting buffer, its response can be matched to that of the non-inverting buffer. The circuit of figure 8 shows the original test circuit with the addition of this frequency-response-matching network (R_T and C_T).

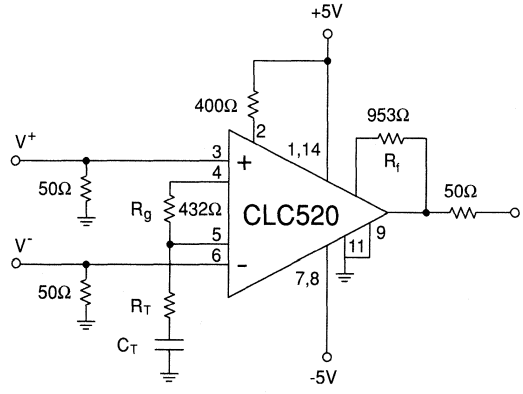


Figure 8: Differential amplifier with inverting response compensation

The single-ended frequency responses shown in figure 3 show a lower bandwidth for the inverting gain path vs. the non-inverting. This bandwidth mis-match is consistent from part to part and is set by the internal gain path. The buffer bandwidths are considerably higher and do not play a role determining this response. The following analysis will show how to select the appropriate values for R_T and C_T such that the frequency response of the inverting gain path can be matched to that of the non-inverting gain path.

ω^+: Non-inverting response pole
ω^-: Inverting response pole

Non-inverting frequency response:

$$A^+ = Ad\left(\frac{\omega^+}{s+\omega^+}\right)$$

Inverting frequency response:

$$A^- = Ad\left(\frac{\omega^-}{s+\omega^-}\right)$$

Assuming $\omega^- < \omega^+$

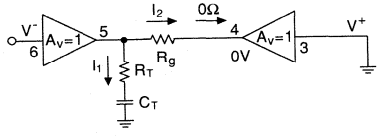
Compensate A^- to achieve the following

$$A^+ = Ad\left(\frac{\omega+}{s+\omega+}\right)$$

$$= Ad\left(\frac{\omega^-}{s+\omega^-}\right)\left(\frac{s+\omega^-}{s+\omega+}\right)\left(\frac{\omega+}{\omega^-}\right)$$

$$= Ad\left(\frac{\omega+}{s+\omega+}\right)$$

The single-ended gain response of either input may be analyzed by grounding one input in order to determine the current generated at the output of the active buffer channel. Adding the R_T-C_T series combination will then provide a means of canceling the internal inverting-path pole with a zero, and replacing it with a pole that matches that seen by the single-ended non-inverting gain path. Note, adding this network will not impact the non-inverting response as long as it is assumed the buffers have zero output-impedance. The following analysis provides a method for computing the required values of R_T and C_T given R_g and the initial single-ended frequency response of each input as shown in figure 3. Note: the input-to-output gain from the current produced in the compensation path is ½ that of the gain of the current produced through R_g.



The output voltage due to an inverting input voltage is:

$$V_o = -\left[\left(1.85(I_2)R_f + \frac{1}{2}(1.85)I_1R_f\right)\right]\left(\frac{\omega^-}{s+\omega^-}\right)$$

$$I_1 = \left(\frac{V^-}{R_T + \frac{1}{sC_T}}\right) \text{ and } I_2 = \frac{V^-}{R_g};\quad \omega^- \equiv \text{single-pole response}$$

Solving this for the gain to the output:

$$\frac{V_o}{V^-} = -1.85\frac{R_f}{R_g}\left(1+\frac{\frac{1}{2}R_g}{R_T}\right)\left(\frac{s+\frac{1}{\left(R_T+\frac{R_g}{2}\right)C_T}}{s+\frac{1}{R_TC_T}}\right)\left(\frac{\omega^-}{s+\omega^-}\right)$$

The non-inverting path has a gain of:

$$\frac{V_o}{V^+} = 1.85\frac{R_f}{R_g}\left(\frac{\omega^+}{s+\omega^+}\right),\ \omega^+ \equiv \text{single-pole response}$$

Equating these two gains requires a cancelling of the ω^- pole with the zero developed by the R_TC_T network while placing the R_TC_T pole at ω^+.

Solving for R_T and C_T

$$R_T = \left(\frac{\frac{1}{2}R_g}{\frac{\omega^+}{\omega^-}-1}\right),\quad C_T = \left(\frac{1}{R_T\omega^+}\right)$$

Estimating ω^+ and ω^- from the -1dB roll-off frequencies of figure 3 and using

$$\omega_{-3dB} = 1.97\ \omega_{-1dB} \text{ for a 1-pole response roll-off}$$

$$\omega^- = 2\pi(176\text{MHz})$$

$$\omega^+ = 2\pi(240\text{MHz})$$

R_T and C_T therefore,

$$R_T = \left(\frac{216}{\frac{240}{176}-1}\right) = 595\,\Omega$$

$$C_T = \frac{1}{(595\Omega)2\pi(240\text{MHz})} = 1.12\text{pF}$$

Figures 9 & 10 show the resulting single-ended frequency responses and the CMRR achieved through this compensation. Comparing figure 9 to figure 3 shows a much closer match over frequency. A significant improvement in the high-frequency CMRR has been achieved with this simple approach. C_T should be tuned for best CMRR at these higher frequencies. Note: when using different values of R_f and R_g, a remeasurement of the single-ended gains is required in order to provide the single-ended gain poles necessary for this compensation analysis.

II. Setting the Differential Gain

To use the CLC520 at a fixed gain, it is best (from a temperature stability standpoint) to operate at its maximum gain, determined by R_f and R_g. The adjustable portion of the CLC520's gain is set by a two-transistor internal differential stage which compares the voltage seen on pin 2 to an internal reference voltage developed as a resistor divider from the positive supply to ground. With approximately 750Ω internally to ground on pin 2, the 400Ω external resistor shown on the circuits above will develop approximately 3.3 volts at pin 2, insuring the internal gain stage is fully switched to maximum gain.

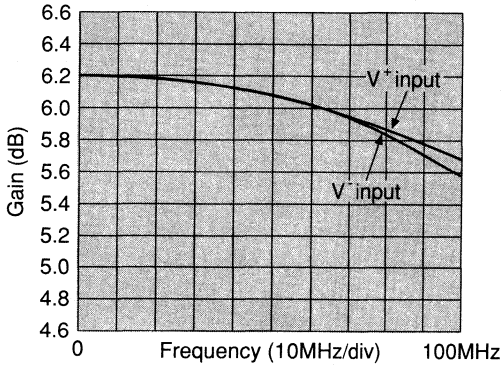


Figure 9: Single-wnded gains with inverting-path compensation

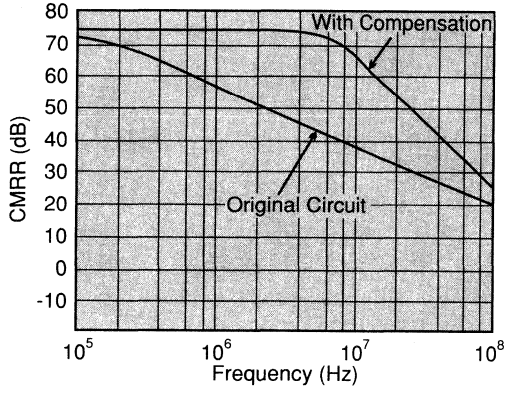


Figure 10: Improved CMRR with better response-match over frequency

Note that the signal gain is also dependent on an internal current-mirror gain from the current developed in R_g to the multiplier stage. This nominal 1.85 factor will show some part-to-part tolerance and a slight temperature dependence. A ± 3% part-to-part tolerance in this current gain along with a +80ppm/°C temperature drift over 0°-70°C may by used in the design of the CLC520 circuits.

III. Using the Gain Adjust Pin

The fixed-gain differential amplifiers shown above can also be disabled with an open-collector pull-down device on pin 2. Once pin 2 is pulled below 0.4 volts, the gain will be attenuated by greater than 60dB. Again, refer to the CLC520 data sheet for a full discussion of signal attenuation vs. gain-adjust voltage. Although the forward path can be shut down in this fashion, the output pin remains a low-impedance driver: it will not be tri-stated. However, when driving several of these differential stages into an n:1 MUX, shutting down the CLC520's gain will significantly improve the overall signal isolation at the MUX output.

An adjustable-gain differential amplifier can also be implemented with the CLC520. As discussed in the data sheet, the CLC520's gain adjustment is intended for operation inside an AGC loop. The gain-adjust accuracy and temperature stability of the CLC520 does not support open loop operation. A companion part, the CLC522, should be used if absolute gain accuracy and gain temperature stability is desired in an open loop (no feedback to the gain adjust pin), adjustable-gain differential-amplifier application.

IV. Input Noise

The equivalent input noise of the CLC520 is set largely by the value of R_g. As shown in the data sheet, a model for the input noise voltage due to R_g is simply R_g*18pA/$\sqrt{Hz}$. For any given gain setting, scaling down the values of R_f and R_g will reduce this input noise. Since R_f controls the output-amplifier stability, it cannot be made too small. For a fixed R_f, decreasing R_g will increase the signal gain. Since the input noise decreases at the same rate as the gain increases, the output noise remains nearly constant as R_g is decreased.

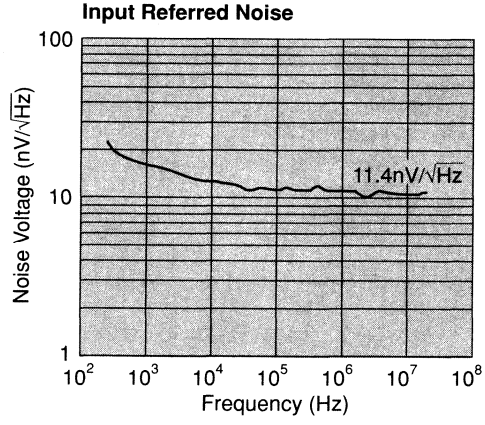


Figure 11: Input noise voltage

Figure 11 shows the measured input-referred spot-noise voltage for the differential amplifier circuit of figure 5.

Application Suggestion: Wideband Differential Coax Line Receiver

It is often necessary to transfer high-speed signals from point to point via a matched-impedance coaxial line. Figure 12 illustrates one receiver implementation using the CLC520 at a fixed gain. Since both buffers have high-impedance inputs, a simple termination across the

center conductor and shield will properly terminate the cable allowing the differential signal to be picked-off and amplified by the CLC520. This circuit ties the coax shield into the local ground through a high-frequency blocking ferrite bead. This will help prevent coupling of high-frequency common-mode noise from the coaxial line onto the local ground, while at the same time setting the DC voltage and current operating point for the CLC520 inputs. This will also act to break high-frequency ground loops between different pieces of equipment.

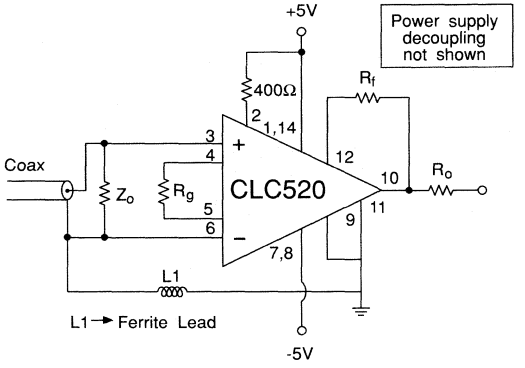


Figure 12: Differential coax line receiver

considering common-mode rejection and offset-current drift, to keep these input termination resistors as large as possible. Ideally, the termination resistors should be eliminated if the bias current can be supplied by the cable. Remember, any mis-match in the single-ended attenuations from the center conductor's and shield's source impedances into the CLC520's input impedances will degrade the CMRR.

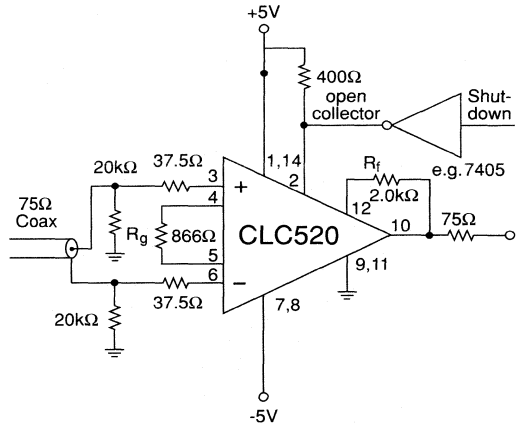


Figure 13: Video loop-through connection using a wideband differential amplifier

Application Suggestion: Video Loop-Through Amplifier

The loop-through connection is one alternative to the impedance-matching approach of high-speed signals. For this approach, a high-input-impedance differential amplifier is simply placed across the center conductor and shield with minimal loading and no characteristic impedance-matching. Good high-frequency common-mode rejection and good wideband differential amplification are essential for this application. The final destination of this daisy-chained connection terminates the cable in it's characteristic impedance.

An implementation of this loop-through connection using the CLC520 is shown in figure 13. This circuit is a replication the circuit of figure 2 with some additional input resistors and a shutdown control gate.

The 20kΩ resistors to ground will insure a DC-bias path for the input-stage bias currents. If it is absolutely certain that a DC path through both the center conductor and the shield will be maintained, the 20kΩ resistors can be eliminated with an overall improvement of VSWR. With only the 20kΩ termination, the CLC520's input offset-current drift will generate a nominal input offset-voltage drift of 100μV/°C. It is desirable, The two series 37.5Ω resistors into pins 3 and 6 act to isolate the inputs from the cable reactance helping to maintain high-frequency input stability. These resistors, included with the parasitic input-capacitance to ground, will also form a matched-impedance termination for the cable at very high frequencies (>500MHz): well beyond the signal frequencies of interest. The full signal level would be available to downstream stages using this wideband differential amplifier as a loop-through connection.

Application Suggestion: A Very Wideband Pulse-Differencing Amplifier

With the addition of several frequency-response trims, the basic circuit figure 2 can be used to implement a very wideband pulse-differencing amplifier. Targeting a gain of +1V/V into a matched 50Ω load, bandwidths in excess of 300MHz are achievable. Figure 9 shows a typical single-sided pulse response. The input rise time for this test is approximately 800ps. With a 1.15ns output rise time and a 0.8ns input rise time, the amplifier's actual rise time is approximately 0.8ns for this 0.9V step at the load. Very similar and well-matched results can be achieved for both the inverting and non-inverting inputs. Contact Comlinear for more information on implementing this circuit.

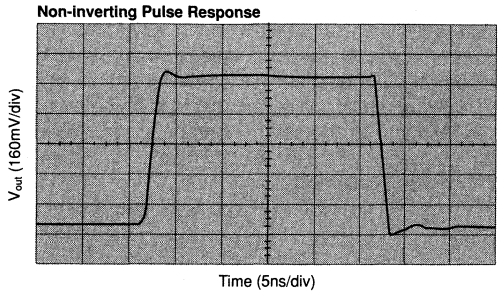


Figure 14. Very wideband single input pulse response

Application Suggestion: Alternative Wideband Differential Amplifiers

Although the classical single op amp differential amplifier has found wide usage, several intrinsic problems limit it's performance. Both signal inputs are looking into relatively low and not necessarily well-matched impedances causing unbalanced signal-source attenuation, having the effect of degraded CMRR. Most simplified analyses assume a 0Ω source impedance in order to circumvent this problem. Furthermore, resistor inaccuracies, instead of the amplifier itself, will typically dominate the CMRR. These resistors and the amplifier's open-loop gain will determine the differential-to-single-ended conversion carried out so well by the CLC520.

However, a classical single-amp differential amplifier combined with a pair of wideband, low-output-impedance buffers can be made to approach the performance of the CLC520. This approach may be preferred if lower input noise, lower power dissipation and improved DC-drift characteristics are worth a higher number of parts, lower differential bandwidth and the necessary precise resistor-matching. Figure 15 provides an example of a single-amp differential amplifier using two buffers from a CLC114 quad buffer and a low-gain op amp with a differential gain of +1V/V.

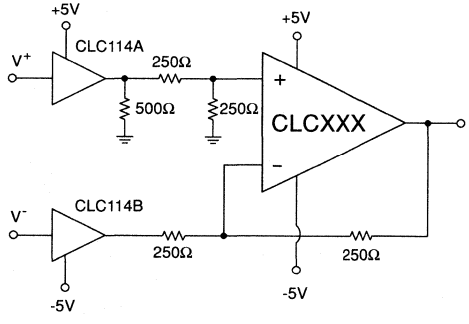


Figure 15. Single amplifier differential amplifier with input buffering

The two input-buffers provide many of the same advantages found with the CLC520 inputs. Any of the input terminations described for the CLC520 may be used here as well. The optional 500Ω resistor to ground on the output of the non-inverting buffer provides a means of matching the loads seen by both buffer outputs. This load matching will improve the high-frequency response-match. The four 250Ω resistors should be matched as closely as possible since any mis-match will degrade the CMRR. The recommended low-gain differencing amplifier may be chosen from the following selection of Comlinear's wideband low-gain amplifiers.

CLC420 - Unity-gain stable voltage-feedback amplifier
This part will provide the best CMRR and DC accuracy

CLC402 - Low-gain high-accuracy current-feed back amplifier
Lower CMRR than the CLC420 with wider bandwidth and better fine-scale, pulse-settling accuracy.

CLC502 - Similar to the CLC402 but with an output-clipping feature

CLC410 - Intermediate performance, low-gain, current-feedback amplifier. This part also includes a shutdown feature and provides the best dG/dϕ for composite video applications.

CLC409 - Very wideband, low-gain, current-feed back amplifier.

All of these parts are optimized for the 250Ω feedback resistor shown in the circuit of figure 15.

Conclusion

As operating speeds have increased, the need for a wide-bandwidth high-CMRR differential amplifiers has increased. Comlinear's CLC520 & CLC522 provide all of the required building blocks integrated into one part. Although intended for adjustable gain requirements, operating the CLC520 at a fixed gain is perfectly acceptable and preferable in a differential receiver application. Signal bandwidths in excess of 150MHz over a wide range of gains, along with CMRR exceeding 60dB through 10MHz, and two matched high-impedance inputs provide all the essential requirements for wideband differential amplification. In some applications using wideband, low power buffers and a standard single op amp differential amplifier topology offers certain advantages over the CLC520 approach.

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Application Note OA-19

Wideband Op Amp Capable of μPower Operation

Michael Steffes

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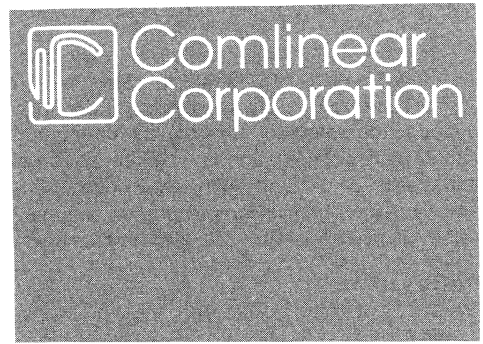

The CLC505 is a current-feedback operational amplifier with an externally-adjustable supply current whose AC performance can be tuned to meet the precise requirements of many high-speed applications. The CLC505 provides a small-signal bandwidth of 150MHz (Av=+6) while drawing 9mA supply current from ±5V power supplies. Reducing the supply current to 1mA decreases the bandwidth by only a third; 50MHz (Av=+6). Please refer to the CLC505 data sheet for a full performance description over the 1mA to 9mA supply current range. The following application note is intended to supplement the CLC505 data sheet describing its operation with quiescent supply currents at or below 1mA.

Frequency Response Dependence on Supply Current

Application note OA-13 describes the internal topology of a current-feedback amplifier and the dependence of its loop gain (and hence bandwidth) on the inverting-input impedance. For an ideal current-feedback amplifier, this impedance is zero and the amplifier's frequency response is completely independent of the signal gain. As the supply current of the CLC505 is reduced below the 1mA region, the inverting-input impedance increases to such a degree that its effect on the loop-gain begins to dominate. To understand the impact of this impedance, as well as a similar increase in the output impedance (R_o) at low supply currents, the amplifier's internal block diagram, figure 1, and resulting transfer function are shown. This analysis considers only the non-inverting op amp configuration but a similar result is obtained for the inverting configuration.

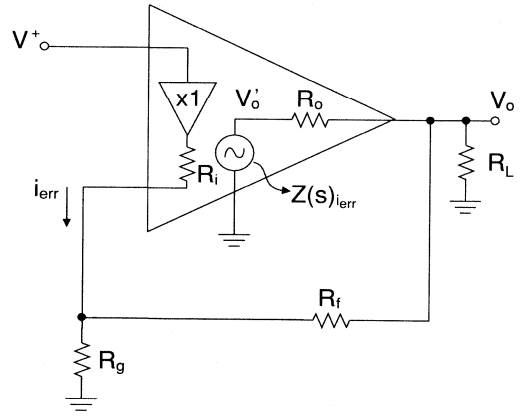

Figure 1: Low Current CLC505 analysis topology

An understanding of the transfer function given in equation 1 is the central point of this discussion. The supply current's dependence enters into this equation through the three internal terms, R_i, R_o, and Z(s). R_i represents the output impedance of the unity-gain buffer found between the amplifier's inputs, while R_o represents the output impedance of the output voltage buffer. Z(s) is the frequency-dependent transimpedance gain which converts the error current (i_{err}), flowing through the inverting input, to a voltage which is buffered to the output.

$$\frac{V_o}{V^+} = \left(1+\frac{R_f}{R_g}\right)\left(\frac{1+\dfrac{R_o}{\left(1+\frac{R_f}{R_g}\right)z(s)}}{1+\dfrac{\left(R_f+R_i\left(1\,|\,\frac{R_f}{R_g}\right)\right)\left(1+\frac{R_o}{R_L}\right)+R_o\left(1+\frac{R_i}{R_g}\right)}{z(s)}}\right) \quad \textbf{Eq. 1}$$

where:

$1+\dfrac{R_f}{R_g} \rightarrow$ desired noninverting signal gain

$\dfrac{R_o}{\left(1+\frac{R_f}{R_g}\right)z(s)} \rightarrow$ will set a limit to the high frequency attenuation as the forward transimpedance gain, Z(s), become very small.

$$\frac{\left(R_f+R_i\left(1+\frac{R_f}{R_g}\right)\right)\left(1+\frac{R_o}{R_L}\right)+R_o\left(1+\frac{R_i}{R_g}\right)}{z(s)} = \frac{1}{\text{Loop Gain}}$$

Both the inverting input and the output pins are voltage-output structures consisting of symmetric (PNP and NPN) emitter followers (ref. 1), very similar to a Class AB power buffer (ref. 2, p 293). Emitter-follower outputs show an output impedance that is directly proportional to the operating temperature (K) and inversely proportional to the transistor's quiescent current ($R_e = V_t/I_c$, $V_t=kT/q$, ref. 2, p 398). As the supply current decreases, the portion of the supply current allocated to these stages also decreases causing an increase in both the inverting input impedance, R_i, and the output impedance, R_o. Decreasing the supply current will also increase the DC open-loop gain, Z_{OL}, while decreasing the dominant pole frequency, w_o. However, the product of $Z_{OL}\cdot w_o$ remains relatively constant over supply current and temperature.

From the transfer function shown in equation 1

Let $1+\dfrac{R_f}{R_g} = A_V^+$ desired signal gain

$z(s) = \dfrac{z_{OL}\,\omega_o}{s+\omega_o}$ single pole, forward transimpedance gain

$$z_t = \left(R_f+R_i\left(1+\frac{R_f}{Rg}\right)\right)\left(1+\frac{R_o}{R_L}\right)+R_o\left(1+\frac{R_i}{Rg}\right) \quad \textbf{Eq. 2}$$

feedback transimpedance; this is the inverting error current, i_{err} resulting from V_o'

$$\text{Loop gain} \equiv \frac{z(s)}{z_t}$$

Rewriting Equation 1 in these terms

$$\frac{V_o}{V^+} = A_V^+ \left(\frac{1 + \frac{R_o}{A_V^+}\left(\frac{s+\omega_o}{z_{OL}\,\omega_o}\right)}{1 + \frac{z_t(s+\omega_o)}{z_{OL}\,\omega_o}} \right)$$

Manipulating this into standard form

$$\frac{V_o}{V^+} = \frac{R_o}{z_t}\left(\frac{s+\omega_o\left(\frac{A_V^+ z_{OL}}{R_o}+1\right)}{s+\omega_o\left(\frac{z_{OL}}{z_t}+1\right)} \right) \quad \text{Let} \quad \frac{A_V^+ z_{OL}}{R_o} >> 1, \quad \frac{z_{OL}}{z_t} >> 1$$

then

$$\frac{V_o}{V^+} = \frac{R_o}{z_t}\left(\frac{s+\left(\frac{A_V^+}{R_o}\right) z_{OL}\omega_o}{s+\frac{z_{OL}\omega_o}{z_t}} \right) \qquad \textbf{Eq. 3}$$

as $s \rightarrow 0$, DC gain, $\frac{V_o}{V^+} = A_V^+$

as $s \rightarrow \infty$, high frequency gain, $\frac{V_o}{V^+} = \frac{R_o}{z_t} \equiv A_{min}$

Note that the zero frequency shown in equation 3 is at a significantly higher frequency than the pole frequency. Once the operating frequency approaches this zero frequency, equation 3 predicts a minimum gain, A_{min}. This is generally not observed in practice, since the zero frequency of equation 3 is typically much higher than the frequencies at which R_i and R_o start to show a normal emitter-follower inductive characteristic. To simplify this analysis, the inductive characteristics of R_i and R_o have been neglected. It should be noted that the inductive characteristics will continue to roll off the closed-loop response with attenuations much greater than that predicted by A_{min} at high frequencies. The zero shown in the transfer function of equation 3 will be neglected with the rest of this discussion focused on the closed-loop pole frequency.

Looking at equation 3 again, the closed-loop response pole will be set by $(Z_{OL} \cdot w_o)/Z_t$. As the supply current is changed, the $Z_{OL} \cdot w_o$ product remains relatively constant. Figure 2 shows the typical open-loop forward transimpedance gain, $(20 \cdot \log(|Z(s)|))$, plotted over frequency as the supply current is varied. Figure 3 shows this same forward open-loop gain at 1mA supply current plotted over the full military temperature range. As long as these forward gain responses fall on the same line in the 20dB/decade roll-off region, the $Z_{OL} \cdot w_o$ product remains constant.

With a constant $Z_{OL} \cdot w_o$ term, the only element setting the bandwidth in the transfer function of equation 3 is the Z_t expression, equation 2. In general, it is advantageous to make Z_t as small as possible which will increase the loop gain and as a result improve harmonic distortion and extend the bandwidth. The limit to the reduction of Z_t comes when higher order poles of Z(s) degrade the phase margin at the unity-gain crossover of the loop gain. For a given supply current and desired gain, decreasing R_f and increasing R_L will decrease Z_t. An important limitation on decreasing R_f is the available output current drive. For the non-inverting configuration, R_f+R_g appears as an additional load in parallel with R_L, while for the inverting configuration, only R_f appears as an additional load in parallel with R_L.

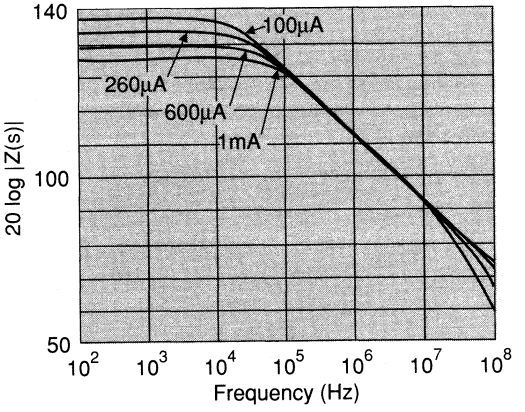

Figure 2: 20log|Z(s)| at different supply currents

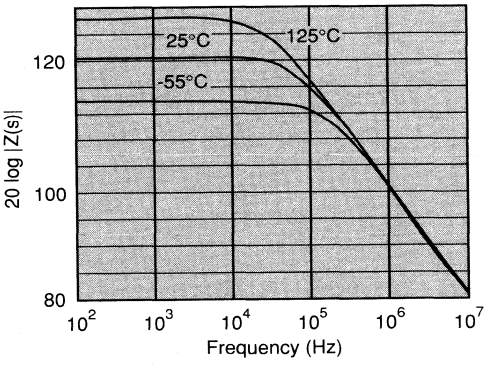

Figure 3: 20log|Z(s)| at 1mA = I_{cc} over temperature

Letting $1 + \frac{R_f}{R_g} = A_V^+$, and $R_g = \frac{R_f}{A_V^+ - 1}$

Z_t can be rewritten as

$$z_t = A_V^+ R_i \left(1 + \frac{R_o}{R_L \| R_f}\right) + R_f + R_o\left(1 + \frac{R_f}{R_L} - \frac{R_i}{R_f}\right) \qquad \textbf{Eq. 4}$$

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Equation 4 emphasizes the gain dependence of Z_t. At low supply currents, R_i becomes so large (500Ω at 1mA) as to cause the first term of equation 4 to dominate. This part of the feedback transimpedance expression is directly related to the desired signal gain, A_v. As the gain is increased, Z_t increases, decreasing the bandwidth. This bandwidth dependence on gain is analogous to that observed with voltage-feedback amplifiers. As such, for configurations which set the first term of equation 4 to be the dominant contributor to Z_t, a gain-bandwidth (GBW) product characteristic will be observed. Figure 4 shows a test circuit used to measure the GBW as the supply current is decreased from 1mA to 100μA over gains of +5, +10, and +20. At very low supply currents, slight DC-output currents due to offsets can change the AC performance. For this reason, the output DC-blocking capacitor was used to limit output DC currents.

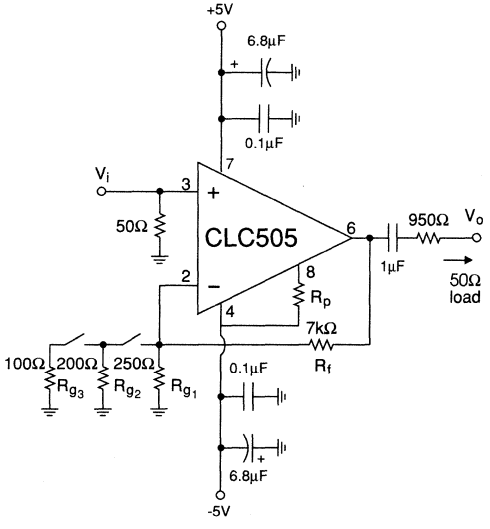

Figure 4: Test circuit for Gain Bandwidth product measurement

For the 1mA case, equations 2 and 3 were used to predict the small-signal -3dB bandwidth at the three gains of +5,+10, & +20.

> With R_p=300kΩ, I_{cc}≈ 1mA, R_i≈ 500Ω, R_o≈ 50Ω and approximate Z_{OL}·w_o product = 2π120E9
> Compute Z_t from equation 2 and expected -3dB bandwidth from equation 3.

The computed and measured results are shown in Table 1.

Table 1.

Gain	Computed Z_t	Expected -3dB BW	Measured -3dB BW	Measured GBW
A_v=5	3.78kΩ	32MHz	57MHz	285MHz
A_v=10	6.50kΩ	18.5MHz	26MHz	260MHz
A_v=20	11.9kΩ	10MHz	11.5MHz	230MHz

Figure 5 shows the small-signal frequency responses for each of these gains normalized to enter the graph at the same point on the y-axis.

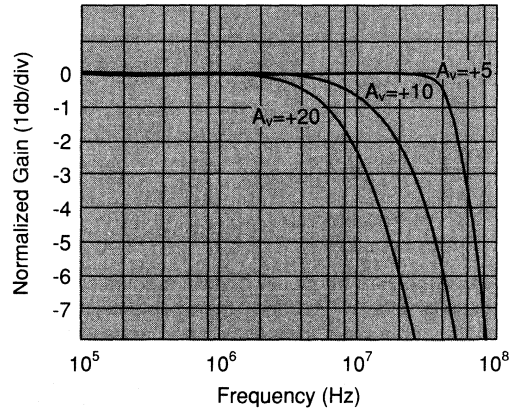

Figure 5: Small signal frequency response vs. gain (I_{cc} = 1mA)

The test results are in good agreement with the simplified analysis of figure 1 at the highest gain tested, A_v=+20. At lower gains, several effects combine to extend the bandwidth beyond that predicted by this simplified analysis. Specifically, all of the additional higher frequency poles of the open loop response can come into play at lower gains. These include both the inductive characteristics of the two output impedances and higher order poles for Z(s). This has the effect of decreasing the phase margin from the theoretical 90° assumed by the single pole analysis. Phase margins less than 90° but greater than 60° will extend the closed-loop bandwidth without peaking.

An additional effect serves to increase the measured bandwidth as the desired signal level is increased. As the frequency of operation increases (or as fast rise time signals are applied), an increase in the steady-state inverting-stage current is observed due to the increased I_{err} required when operating at these higher frequencies with reduced loop gain. This increasing error current, as the input is swept over higher frequencies, decreases the inverting input impedance. This frequency and signal level

dependence of R_i will decrease the value for Z_t, increasing the loop gain and extending the bandwidth. This effect is particularly pronounced when the $R_i \cdot A_v$ term becomes a large part of the total Z_t expression, at relatively high non-inverting or inverting gains. Under these conditions, the bandwidth actually increases as the signal level is increased. Figure 6 shows this effect for the A_v=+20 case of Fig. 4 with I_{cc} = 1mA.

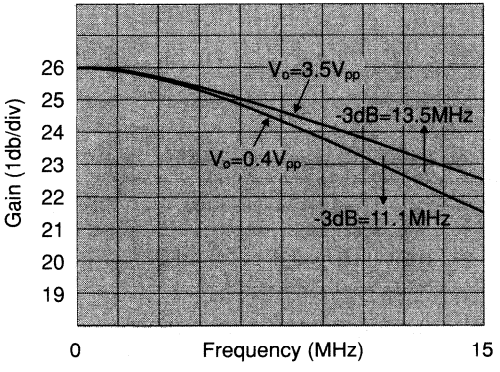

Figure 6: Frequency response vs. signal level

For a given desired supply current, load impedance and signal gain, a close inspection of the feedback transimpedance expression of equation 4 shows that an optimum R_f can be found that will minimize Z_t, maximizing the bandwidth and loop gain. This is a relatively shallow minimum with the resulting -3dB bandwidth not significantly different than for a fixed 1kΩ = R_f. Nevertheless, solving for this optimum R_f yields the following.

$$\text{Optimum } R_f = \sqrt{\frac{R_i R_o\left(A_V^+ - 1\right)}{1 + \frac{R_o}{R_L}}} \qquad \textbf{Eq. 5}$$

Table 2 shows the required information to predict a gain-bandwidth product vs. supply current. At each supply current, the internal parameters (R_i, R_o, and $Z_{OL} \cdot w_o$) are shown. From this, an optimum R_f can be calculated using equation 5. The measured small-signal bandwidth and GBW are then recorded. The measured -3dB bandwidths shown in table 2 agree very closely with those predicted from $Z_{OL} \cdot w_o / Z_t$ (evaluating this expression from the data given in this table and equation 2 for Z_t).

This estimate of GBW vs. supply current represents a very conservative estimate. As the signal gain is decreased from A_v=+20V/V, the GBW will increase as shown in table 1. In addition, the measured bandwidth would increase as signal level is increased, as discussed earlier, up to the point that output-stage drive current and slew limits come into consideration. The supply current and resulting GBW of table 2 are plotted in figure 7. This GBW should be taken as a minimum achievable value and a good starting point for estimating the bandwidth capability of the CLC505 at very low supply currents. A PSPICE simulation macromodel available from Comlinear can be used to test the performance under different operating conditions. This macromodel reasonably simulates most of the effects discussed earlier. Transient simulation will even show the improved rise times at higher gains as the signal swing is increased.

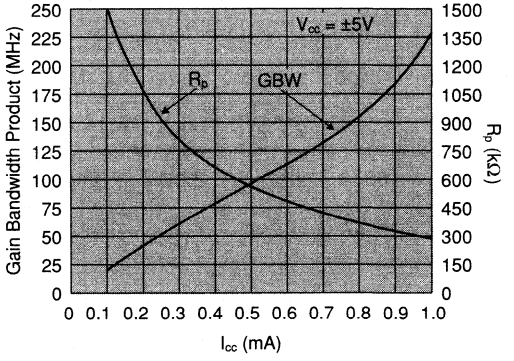

Figure 7: Gain bandwidth product and current set resistor vs. I_{cc}

A common way to illustrate the wideband capability of low-power amplifiers is through a MHz-per-mA figure of merit. Figure 8 shows the same data as figure 7 with boundary regions for decades of MHz/mA shown. Two low-power Maxim op amps are also shown that claim superior MHz/mA performance. Although certainly capable parts, the Maxim amplifiers are about a decade lower in performance than the CLC505. The CLC505, along with several other Comlinear wideband current-feedback amplifiers (such as the CLC406), push strongly above the 100MHz/mA barrier. The discussion thus far has assumed ±5 volt supplies. As will be discussed later, single supply operation is also possible.

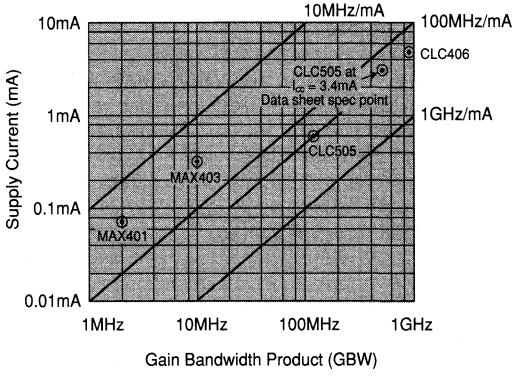

Figure 8: GBW vs. supply current

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Table 2: Performance vs. Supply Current (V_{CC}=±5V, T_A=25°C, R_L=1kΩ)

R_p	I_{cc}	R_i	R_o	Z_{OL}	W_o	$Z_{OL}W_o$	A_v=+20 Optimum R_f	A_v=+20 -3dB BW	GBW
300kΩ	1mA	500Ω	47Ω	1.93MΩ	2π62kHz	2π120E9	653Ω	11.4MHz	228MHz
400kΩ	800µA	620Ω	64Ω	2.46MΩ	2π49kHz	2π121E9	842Ω	7.9MHz	158MHz
500kΩ	600µA	920Ω	81Ω	2.92MΩ	2π42kHz	2π123E9	1.14kΩ	6.0MHz	120MHz
600kΩ	480µA	1.16kΩ	100Ω	3.35MΩ	2π38kHz	2π127E9	1.42kΩ	4.6MHz	92MHz
900kΩ	260µA	1.97kΩ	139Ω	4.73MΩ	2π26kHz	2π123E9	2.14kΩ	2.7MHz	54MHz
1MΩ	230µA	2.27kΩ	185Ω	5.13MΩ	2π25kHz	2π128E9	2.60kΩ	2.3MHz	46MHz
1.3MΩ	160µA	3.27kΩ	258Ω	6.80MΩ	2π20kHz	2π136E9	3.57kΩ	1.6MHz	32MHz
1.6MΩ	100µA	4.30kΩ	333Ω	7.50MΩ	2π17.5kHz	2π131E9	4.52kΩ	1.1MHz	22MHz

Secondary Effects of Low Supply Current Operation

Besides having a profound effect on the small signal AC performance, low supply current operation of the CLC505 will also modify most other performance characteristics. The most drastic effect is on the available output current. At 1mA supply current, the CLC505 data sheet guarantees ±5mA at 25°C. This specification should be scaled down proportionately for operation below 1mA. The non-inverting slew rate is retained with very low power levels due to a slew enhancement circuitry in the input buffer stage (e.g. at 1mA supply current, SR = 500V/µs for the particularly demanding condition of A_v=+2). Both of the input bias currents will decrease with supply current but the input offset voltage and temperature drift will become more pronounced. Recall that, for a current-feedback topology, the two input bias current terms are unrelated in both magnitude and polarity. Bias current cancellation to an offset-current specification is therefore ineffective. Please refer to the CLC505 data sheet for more information on these DC error terms at 1mA.

The most subtle effect is perhaps found with the noise performance. As I_{cc} is reduced, all of the amplifier's input referred noise terms show an increase in their 1/f noise corner frequencies. Also, an additional gain term for the inverting noise current becomes appreciable. Specifically, the inverting input impedance acts as an additional impedance gain for the inverting bias current noise. The noise model discussed in application note OA-12 (Noise Analysis for Comlinear's Current-Feedback Amplifier's) does not consider this effect and would therefore understate the total output noise. The simulation macromodel will, however, show the correct output noise including this effect.

Taking Advantage of the Voltage Feedback Characteristic

Most of the design techniques developed for voltage-feedback amplifiers are applicable to the CLC505 operating at or below 1mA supply current. One of the standard applications for a voltage-feedback amplifier, that is not directly possible with a current-feedback part, is a simple integrator with direct capacitive feedback. Changing the feedback resistor to a capacitor and moving to the inverting integrator configuration will result in the following circuit, figure 9, and transfer function.

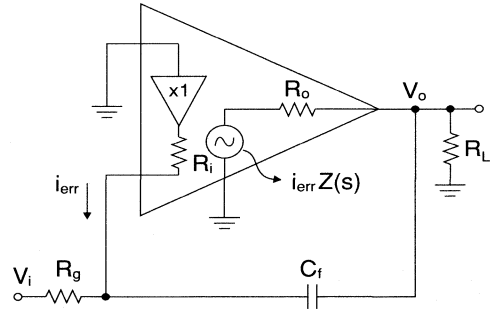

Figure 9: Analysis circuit for inverting integrator

Neglecting the high frequency zero due to R_o

$$\frac{V_o}{V_i} = \frac{-1}{sR_gC_f} \left(\frac{1}{1+\frac{1}{z(s)}\left(R_i\left(\frac{R_o}{R_L \| R_g}+1\right)+R_o\right)\left(\frac{s+\frac{1}{C_f\left(R_i \| R_g + R_o \| R_L\right)}}{s}\right)} \right)$$

Should set feedback transimpedance zero < higher order poles of Z(s)

$$\frac{1}{C_f\left(R_i \| R_g + R_o \| R_L\right)} < 2\pi(10 \rightarrow 20\text{MHz}) \text{ for } I_{cc} \leq 1\text{mA}$$

Also, high frequency feedback impedance should be > 1kΩ

$$R_i\left(\frac{R_o}{R_L \| R_g}+1\right)+R_o > 1\text{k}\Omega$$

Figure 10 shows a test circuit to demonstrate this integrator operation, while figure 11 shows the resulting integration of a square wave (100kHz) input to an output triangle wave. Again the simulation macromodel for the CLC505 is very effective for analyzing the performance of these types of circuits.

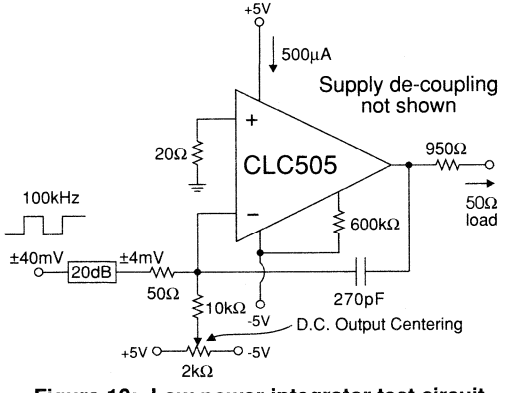

Figure 10: Low power integrator test circuit

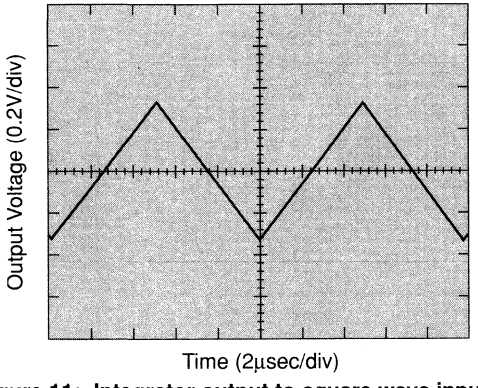

Figure 11: Integrator output to square wave input

Figure 12 shows the simulated gain and phase for the integrator shown in figure 10. Note that the DC gain of 66dB is comparable to other high-speed voltage-feedback amplifiers (such as the CLC420) while the supply current for this integrator is a very low 500µA.

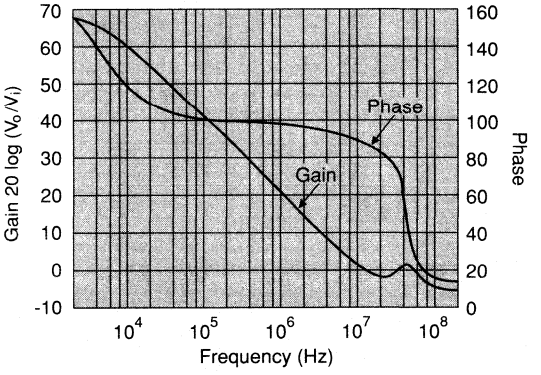

Figure 12: Integrator frequency response

µPower Active Filters

To implement the Sallen-Key type of active filters, it is generally desirable to have an amplifier bandwidth at least twenty times the desired cutoff frequency. It is also desirable to operate the amplifier at relatively low gains. Figure 13 shows a test circuit used to demonstrate the CLC505's capability of implementing very low-power single-supply high-frequency active filters.

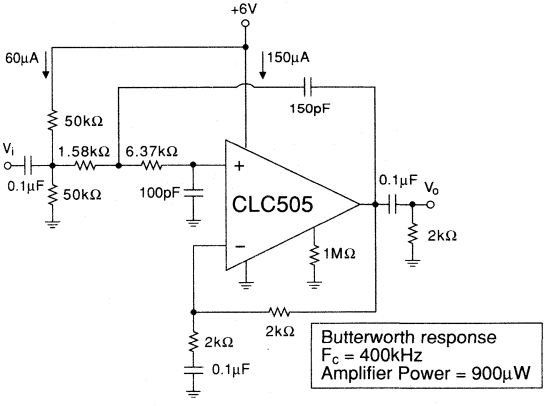

Figure 13: Single supply µpower active filter

For low-power single-supply operation, all of the signal nodes need to be AC coupled. The three 0.1µF capacitors provide this function. This allows the non-inverting input pin to be biased at a midpoint between the supply pins, +3V in this case. The capacitors also prevent any DC currents from flowing in the output pin and reduce the DC amplifier gain to 1, which will hold the output pin DC operating point equal to the non-inverting input (centered between the supply pins.) At least 6 volts across the part's supply pins is required to give some signal swing capability at the input

stage from common-mode input range considerations. The amplifier's AC gain has been set for +2 and the filter components have been adjusted to allow for the amplifier's bandwidth (ref. 3).

Figure 14 shows the frequency response for just the amplifier. At this very low power and gain some peaking due to a loss of phase margin is observed. This will not effect the filter performance however. The 9MHz bandwidth is more than adequate to implement the desired 400kHz Butterworth low-pass filter. Figure 15 shows the measured filter frequency response. The desired cutoff was achieved precisely. The loss in rolloff at higher frequencies arises from a direct signal coupling to the output through the filter components after the amplifier has stopped controlling the output voltage.

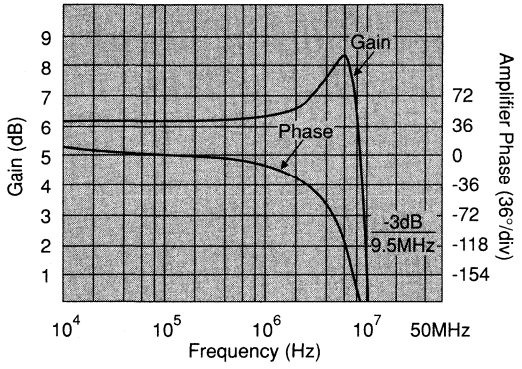

Figure 14: Very low power, single supply, amplifier frequency response

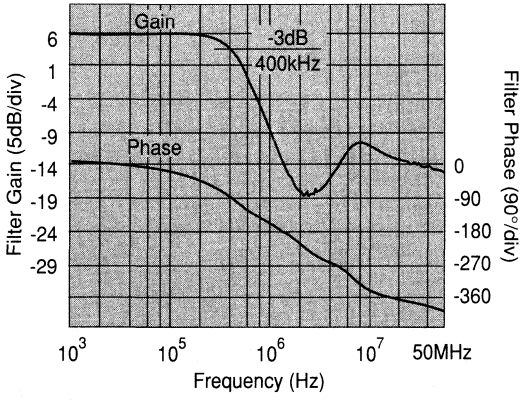

Figure 15: Very low power, single supply, active filter frequency response

Conclusions and Caveats

The CLC505 adjustable supply current op amp offers one of the highest MHz-per-mA performance levels available in a monolithic amplifier. A simplified analysis can do a good job of predicting the gain-bandwidth product under a variety of supply current, gain, feedback resistor, and loading conditions. A PSPICE simulation model available from Comlinear does an even better job of predicting performance over a wide variety of conditions. Although the internal topology of the CLC505 uses a current-feedback approach, at very low supply currents this part may be treated more like a voltage-feedback amplifier having a gain-bandwidth product. Very high-speed integrators and active filters may be implemented at exceptionally low supply currents.

Due to leakage effects, the part-to-part tolerance on supply current for a fixed R_p becomes greater as the desired nominal supply current is decreased. At R_p=300kΩ, Comlinear guarantees a maximum 1.3mA supply current at 25°C from a nominal 1mA value. If a closer tolerance at this, or lower, supply currents is required, please contact Comlinear for further information.

References:

Ref. 1 "Current Feedback Amplifiers", Comlinear Application Note AN

Ref. 2 "Analysis and Design of Analog Integrated Circuits", Gray & Meyer, Wiley 1977.

Ref. 3 "Simplified Component Value Pre-Distortion for High Speed Active Filters", Comlinear Application Note OA-21

Application Note OA-20

Current Feedback Myths Debunked

Arne Buck

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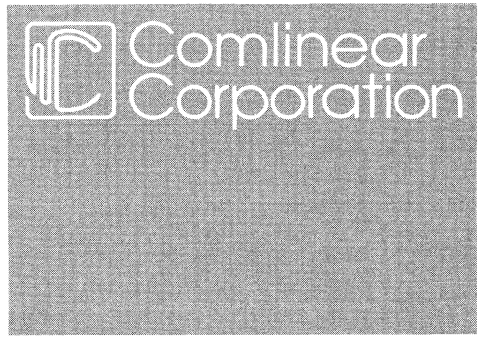

Mystery needlessly surrounds the operation and use of current feedback operational amplifiers. Many engineers refuse to design with these op-amps due to misunderstandings which are easily rectified.

Much has been written to date on the internal circuitry of current feedback op-amps. These open-loop "tutorials" obfuscate how current feedback works in a closed-loop circuit. Practical op-amp circuits are closed-loop feedback systems which yield to classical control theory analysis. Analog circuit designers are comfortable with voltage feedback op-amps in a closed-loop circuit and with the familiar ideal op-amp approximations feedback affords. It will be shown that current feedback op-amps can be analyzed in an analogous fashion. Once this closed-loop similarity is appreciated, it is easy to see that most circuits commonly built with voltage feedback op-amps can be realized with a current feedback op-amp, and with better results at high frequencies.

Refer to figure 1 to review the open-loop terminal characteristics of a voltage feedback amplifier. Ideally the non-inverting input impedance is infinite, as is the inverting input impedance. The output is a voltage source, the output impedance of which is zero. This voltage source is controlled by the potential difference between the two op-amp input terminals. This is the error voltage, hence the term voltage feedback. Feedback will drive the error voltage to zero. The open-loop dynamics are contained in A(s). This A(s) is a dimensionless gain, often represented in units of volts per volt or decibels.

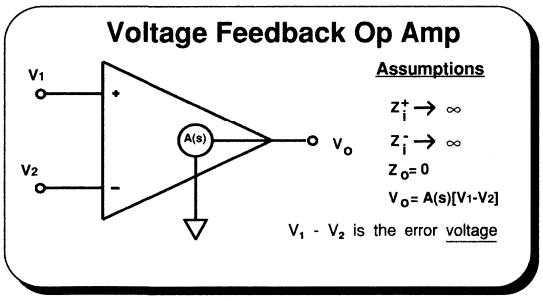

Figure 1

A typical voltage feedback circuit is shown in figure 2, the inverting amplifier. The transfer function is developed from the following equations:
$V_1 = 0$, $V_o = -A(s)V_2$, $(V_i - V_2) / R_1 = (V_2 - V_o) / R_2$.

As A(s) approaches infinity, the closed-loop gain is $-(R_2 / R_1)$. The frequency response of the closed-loop circuit is determined by the denominator of the transfer function. Both the noise gain $(1 + R_2 / R_1)$ of the circuit and the frequency-dependent source (A(s)) appear in the denominator, linking the closed-loop gain and bandwidth.

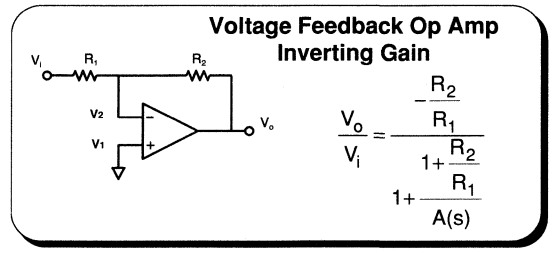

Figure 2

The familiar Bode plot of this circuit is shown in figure 3. The amplifier is typically compensated with a dominant low-frequency pole to ensure stability down to a specified minimum gain, often unity. In the region where the one-pole approximation of the open-loop response is valid, the phase is around -90 degrees. This is the gain-bandwidth product region. The intersection of the zero-slope noise gain line and the open-loop gain curve determines the closed-loop system –3dB bandwidth. A high gain circuit will have less bandwidth than a lower gain circuit. As the circuit moves to lower gains, bandwidth increases, phase margin is lost and stability suffers.

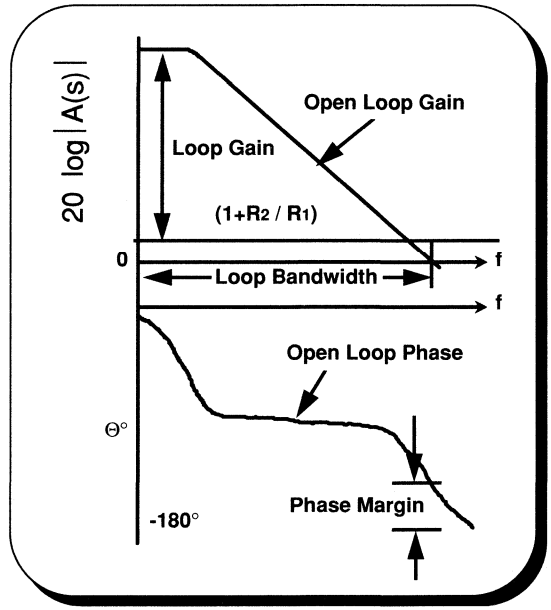

Figure 3

The open-loop terminal characteristics of a current feedback amplifier are depicted in figure 4. There is a unity-gain buffer between the two op-amp inputs. This buffer ideally has infinite input impedance and zero output impedance.

Thus the non-inverting input impedance of the current feedback op-amp is infinite, and the inverting input impedance is zero. The output is a voltage source, so the output impedance is zero. This voltage source is controlled by the current out of the inverting input. This is the error current, hence current feedback. Feedback forces the error current to zero. The open-loop dynamics are determined by Z(s). This Z(s) is a current controlled voltage source which has units of transimpedance, ohms.

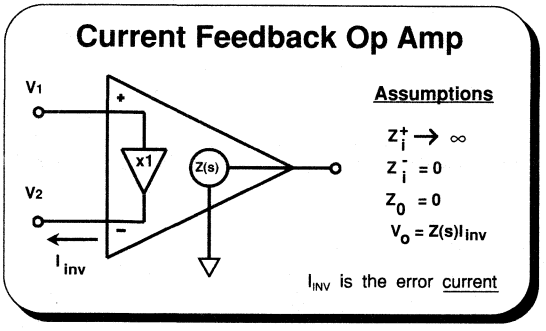

Figure 4

The inverting amplifier employing a current feedback op-amp is shown in figure 5. The transfer function is derived from the following equations:
$V_1=0$, $V_o = Z(s)I_{inv}$, $(V_i / R_1) + I_{inv} = -(V_o / R_2)$

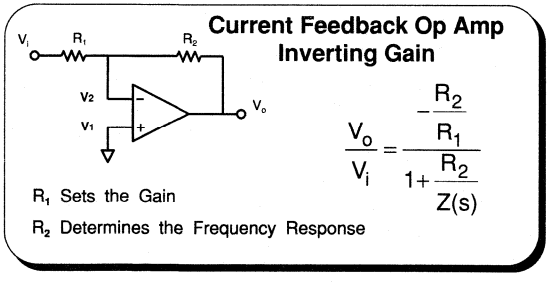

Figure 5

As Z(s) approaches infinity, the closed-loop gain is $-(R_2 / R_1)$. Notice that only the feedback resistor appears in the characteristic equation, in the term with Z(s). The closed-loop gain has been decoupled from the frequency response determining term of the transfer function. Only the feedback resistor affects the closed-loop frequency response.

A Bode plot for the circuit is shown in figure 6. A current feedback amplifier is also compensated with a dominant low-frequency pole. This pole is usually at a higher frequency than that of a voltage feedback op-amp. A current feedback op-amp is commonly compensated for maximally flat response at a specified closed-loop gain and with a specified feedback resistor. The phase is approximately -90 degrees where this one-pole approximation is valid. The ideal current feedback op-amp does not have a gain-bandwidth product. The closed-loop bandwidth is determined by the feedback resistor, not the closed-loop gain. One could entertain the idea of a "feedback-resistor-bandwidth" product. The intersection of the zero-slope feedback resistor line and the open-loop transimpedance curve yields the closed-loop -3dB bandwidth. A circuit with a higher feedback resistor will have reduced bandwidth. This is a good way to overcompensate the current feedback op-amp. A feedback resistor of twice the manufacturer's recommended value will cut the circuit bandwidth in half. As the feedback resistance, or impedance, is reduced to a lower value, there is a loss of phase margin. As can be seen from the transfer function in figure 5, if the negative of the loop transmission, $(R_2 / (Z)s)$, equals -1 the loop is unstable.

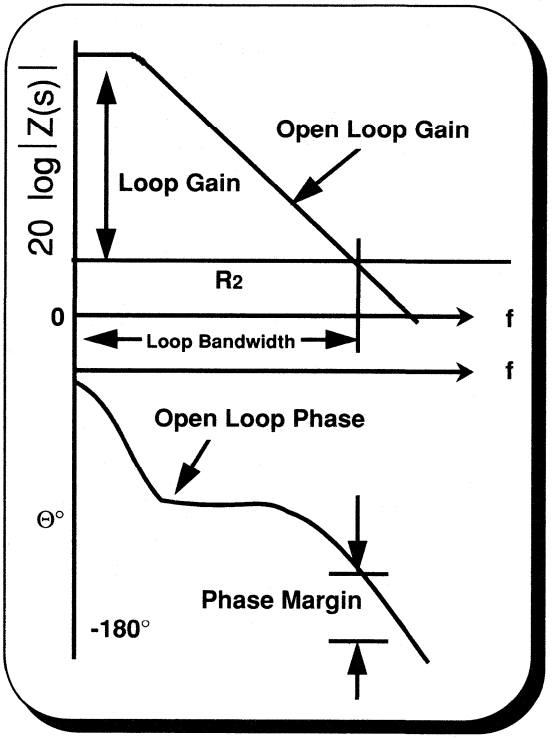

Figure 6

The design trade-offs between current feedback and voltage feedback differ. Voltage feedback allows freedom of choice of the feedback resistor (or impedance) at the expense of sacrificing bandwidth for gain. Current feedback maintains high bandwidth over a wide range of gains at the cost of limiting the feedback impedance.

For example, a common error in using a current feedback op-amp is to short the inverting input to the output in an attempt to build a voltage follower. This circuit will oscillate. The circuit is perfectly stable if the recommended feedback resistor is used in place of the short. Similarly, an integrator is commonly accomplished by placing a capacitor between the inverting input and output. At high frequencies a capacitor has a low impedance and can easily have an impedance less than that required for stability. The proper feedback resistor in series with the feedback capacitor will stabilize the amplifier, and introduce a high frequency zero into the integrator transfer function.

Another aspect of current feedback op-amps which causes much consternation is the low open-loop inverting input impedance. This feature, which causes the decoupling of closed-loop gain and bandwidth, is often viewed as making current feedback op-amps unsuitable for use as differential amplifiers. In fact, the low inverting input impedance can result in a better high-frequency differential amplifier than a similar circuit built with a voltage feedback op-amp.

First, consider the closed-loop driving-point impedance of an op-amp, regardless of the nature of the error signal. The circuit and equations to find this closed-loop impedance are shown in figure 7. The resistor, R, is the open-loop inverting input impedance. Note that R is simply a resistance. A voltage feedback amplifier will have an R approaching infinity; in a current feedback op-amp R approaches zero. A test current, I_T, is applied to the inverting input and the inverting node currents are summed. To find the closed-loop inverting input impedance of either amplifier type simply substitute the proper form of the output voltage, V_o.

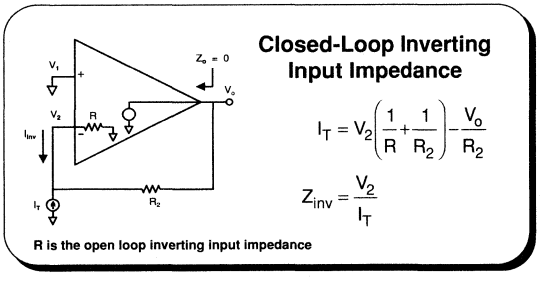

Figure 7

In the case of the voltage feedback op-amp, $V_o = -V_2 A(s)$ for this circuit. The result, $Z_{INV}(s)$, is in figure 8. The familiar result is that when A(s) approaches infinity, the incremental inverting impedance approaches zero. This is the incremental or virtual ground on which much first-order op-amp analysis is based.

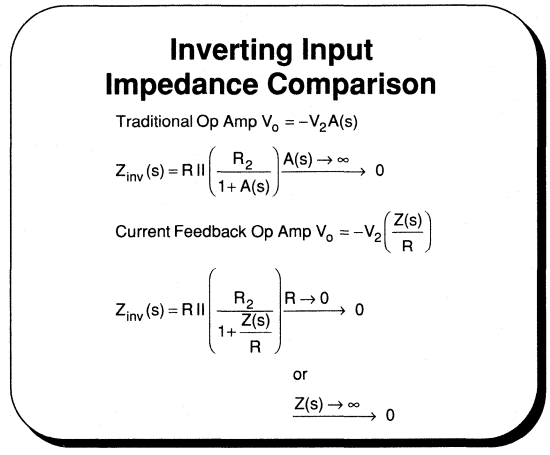

Figure 8

The output voltage is derived differently in the current feedback op-amp. When $V_o = -V_2(Z(s) / R)$ is substituted, the result is in figure 8 also. It can be seen that two mechanisms force the inverting input impedance to a low value, ideally zero. When Z(s) is very large, $Z_{INV}(s)$ goes to zero. In addition, as R goes to zero so does the closed-loop inverting input impedance. The topology of the input buffer keeps R small to very high frequencies. Thus a current feedback op-amp can have a better virtual ground at the inverting input than a voltage feedback amp, especially at high frequencies.

A summary of the above discussion is tabulated in figure 9. The voltage difference between the input terminals is zero. Voltage feedback drives this difference to zero. The current feedback amplifier input buffer forces the two input terminals to equal voltages. Both amplifier types have a high non-inverting input impedance, so the non-inverting current is small. A voltage feedback op-amp has a high open-loop inverting input impedance, thus the inverting current approaches zero. Current feedback forces the inverting current to zero. Both op-amps display similar input voltage and current characteristics. Only the mechanism forcing these to zero differs.

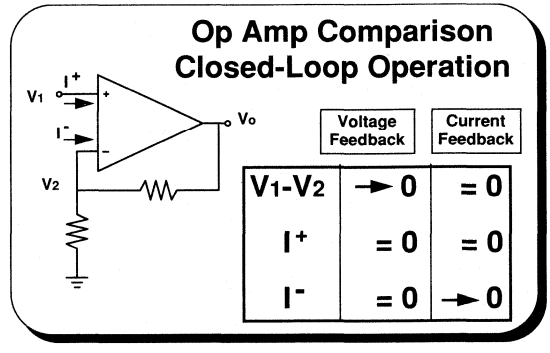

Figure 9

It can now be seen that from a closed-loop standpoint both current and voltage feedback op-amps allow the same ideal op-amp assumptions to be made. Voltage feedback has a gain-bandwidth product which limits the lowest stable gain. Current feedback displays a "feedback-resistor-bandwidth" product which limits the lowest stable feedback impedance.

The inverting input impedance of an ideal voltage feedback op-amp in a closed-loop circuit is zero. Feedback accomplishes this by dividing a high open-loop impedance by a high loop gain. The open-loop inverting input impedance of an ideal current feedback op-amp is zero. A practical current feedback op-amp has a finite inverting input impedance, less than 100Ω. Feedback reduces this further by dividing the initially low open-loop inverting input impedance by the loop transmission. The result is a better incremental ground at the inverting input to very high frequencies.

As both amplifier types are used in closed-loop topologies, the same methods of analysis are equally applicable. Now that this is seen, current feedback op-amps can easily be designed into amplifiers of any arbitrary gain (inverting and non-inverting), integrators, differential amplifiers (figure 10), and current-to-voltage converters, commonly known as transimpedance amplifiers (figure 11).

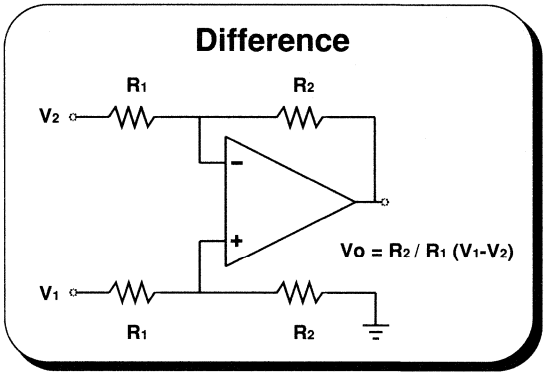

Figure 10

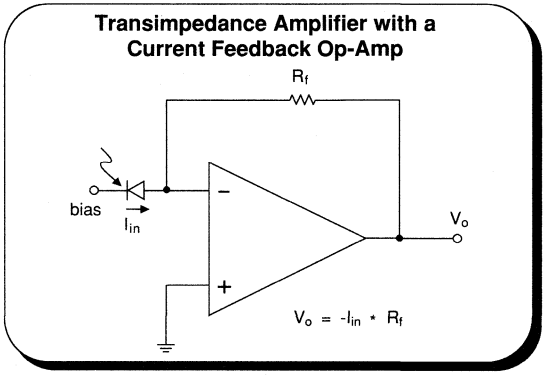

Figure 11

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Application Note TH-05

Selecting and Using High-Speed Track and Hold Amplifiers

David Potson
Scott Evans

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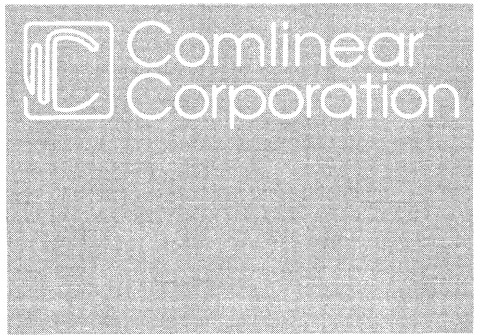

INTRODUCTION

High-speed track and hold (T/H) amplifiers are essential elements of high-performance flash A/D systems. In order to realize the performance improvements that a T/H can achieve, a knowledge of how to select the proper device and how to properly apply it is necessary. This requires a clear understanding of how the various device specifications impact system performance. This application note will discuss these issues in relation to the high-speed architecture of figure 1. The latter part of the ap note should be referenced for a detailed definition of each specification.

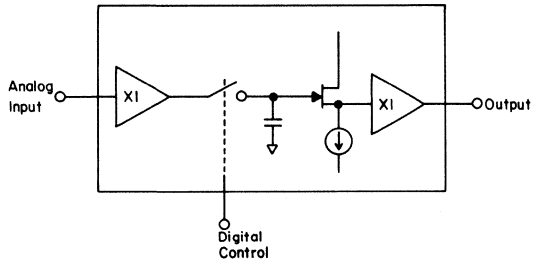

Figure 1: Block diagram of a high-speed T/H amplifier.

TIMING CONSIDERATIONS

The first consideration in selecting a T/H is to find one that will be fast enough for the intended A/D conversion system. There are two common flash conversion systems where T/Hs are frequently found. The simplest is the single-stage flash converter of figure 2. It is instructive to analyze the timing relationships of this system. A more complicated system, the sub-ranging A/D, is used where higher resolution is required at high sample rates. The timing relationships of this latter system are more complex and will not be discussed in this application note, although the concepts presented are valid in these systems as well.

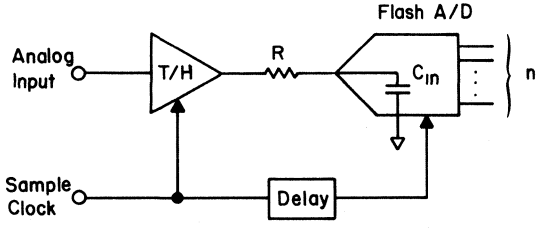

Figure 2: Block diagram of a single-stage flash A/D converter system incorporating a T/H amplifier.

In a timing analysis, there are two points of interest. The first is the T/H clock rate and duty cycle, and the other is the timing relationship of the A/D clock with respect to the T/H clock. The A/D clock duty cycle is also important, but is independent of the T/H and so will not be discussed.

The T/H worst-case clock rate and duty cycle are obtained by independently determining the minimum required "track" and "hold" times. Since sufficient time must be provided for all events to take place within their respective periods, the timing equations can be determined from the waveforms of figure 3. These are:

$$t_{TRACK} = t_{ACQ} + t_{DHT} - t_{EAD} - t_{DA} \quad (1)$$

$$t_{HOLD} = t_S + t_{A/D} - t_{DHT} + t_{EAD} + t_{DA} \quad (2)$$

where $t_{A/D}$ is the aperture time of the A/D and t_{ACQ} is the acquisition time of the T/H while driving the capacitive input of the A/D—not the value which is specified into a purely resistive load. Remember that t_{EAD} can be either positive or negative, depending upon the specific T/H. The minimum T/H cycle time is simply the sum of the above equations:

$$t_{CYCLE,\ MIN} = t_{ACQ} + t_S + t_{A/D} \quad \text{[Ideal case]} \quad (3)$$

Note that the three delay terms are "pipelined" out of the system.

Operation of the T/H at this minimum cycle time presents a problem, though, which is caused by manufacturing variations of the T/H and A/D. Again, since sufficient time must be allowed for all events, the worst-case t_{TRACK} and t_{HOLD} times should be used in the system set-up if the system must work without timing adjustments. Minimum t_{TRACK} is found by setting all positive terms in equation 1 to their maximums and all negative terms to their minimums. Likewise for equation 2. Now, however, the sum of equations 1 and 2 no longer equals equation 3. A more accurate expression for the minimum cycle time is,

$$t_{CYCLE,\ MIN} = [t_{ACQ} + t_S + t_{A/D}] + [\Delta t_{DHT} + \Delta t_{EAD} + \Delta t_{DA}] \quad (4)$$

The terms within the second set of brackets all cause the minimum cycle time to increase from the ideal value given by the first set. To set the system for maximum speed, the minimum cycle time is first computed from equation 4 and then equations 1 and 2 are used to set clock duty cycle while keeping in mind worst-case conditions.

Although they serve as useful analytical tools, equations 1, 2, 3, and 4 cannot in practice be used by themselves to arrive at a timing setup. This is because T/H manufacturers do not guarantee some of the delay terms and, when delay terms are guaranteed, just a maximum or a minimum is given. In addition, some A/D manufacturers do not guarantee $t_{A/D}$. This all points to the necessity of designing sufficient margin into the system timing. The best that can be done is to obtain typicals where no data is given and then to assume "reasonable" variations for those delays where only one extreme is guaranteed. Finally, the system can be tested to determine sensitivity to timing errors by varying T/H clock duty cycle and monitoring the change in performance. If an extreme sensitivity is found, system timing can be altered.

A similar analysis to that above shows that the conversion edge of the A/D clock should be positioned in relation to the hold edge of the T/H clock according to the following equation:

$$t_{EDGE\ SKEW} = t_{EAD} + t_{DA} + t_S + t_{GR} - t_{EAD,\ A/D} \quad (5)$$

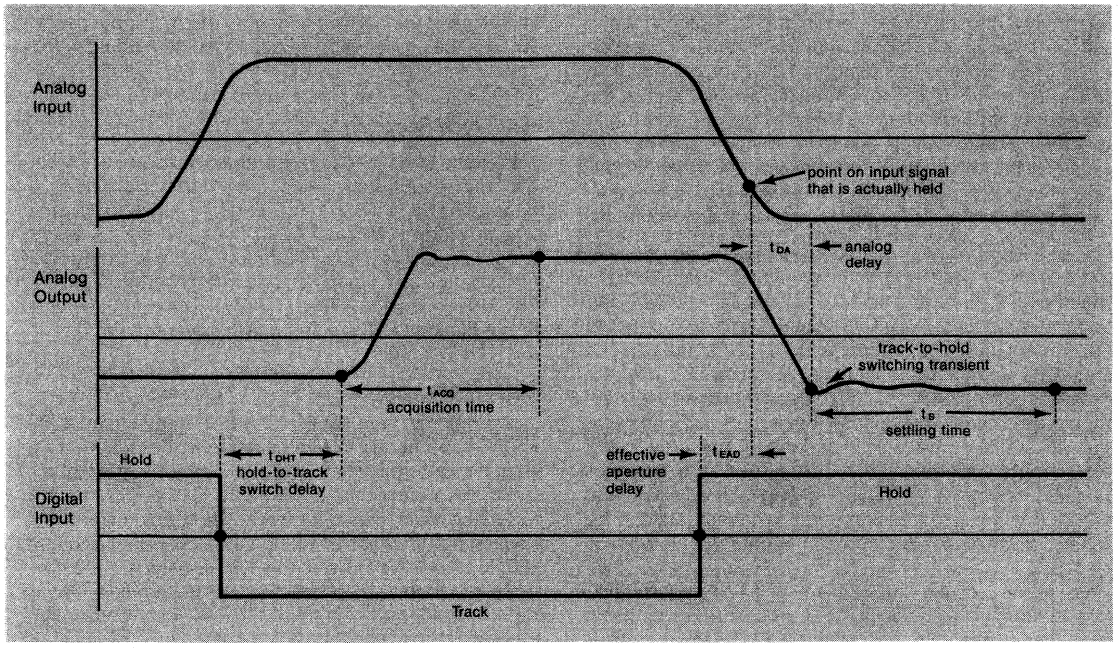

Figure 3: T/H amplifier waveforms for timing analysis.

where t_{GR} is the group delay of the RC filter formed by the A/D input capacitance and the series damping resistor, and $t_{EAD, A/D}$ is the effective aperture delay of the A/D. The same definition of effective aperture delay as applies to T/Hs is assumed for the A/D. A positive value for $t_{EDGE\ SKEW}$ indicates that the T/H clock edge should precede the A/D clock edge.

The same problems noted above exist also with the application of equation 5. Only typical values are usually given for t_{DA} and most A/D manufacturers specify a maximum for $t_{EAD, A/D}$ when a minimum is what is needed.

A versatile circuit for generating both the T/H and A/D clocks is shown in figure 4. Although somewhat complex, this circuit has the advantage of being able to independently set the duty cycles of both clocks and the skew between them. This may be of benefit in those situations where only one design iteration of the PCB will be performed, but it is still desired to make last-minute changes in the timing for optimum performance. Of course, if this is unnecessary, or if the A/D duty cycle is not critical, the circuit can be greatly simplified.

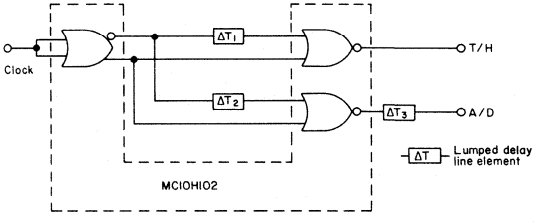

Figure 4: This clock circuit provides control over the delay between the T/H and A/D control signals and the duty cycles of these signals. Timing changes are made by selecting different delay line taps with wire jumpers.

LINEARITY AND DYNAMIC ACCURACY

Linearity and dynamic accuracy form another set of specifications usually evaluated in conjunction with the timing specifications. DC linearity is of some interest since a device cannot be relied upon to deliver better dynamic accuracy than it can at DC. More importantly, designers of high-speed systems focus on the harmonic distortion specification, which is an indication of the linearity of the amplifiers within the T/H at high analog frequencies. Both of these linearity specifications describe operation in the track mode. In addition, there are specifications that apply to the hold mode which can also impact accuracy. Finally, aperture jitter is a specification describing an error source that occurs during the transition from track to hold.

Harmonic Distortion

Because harmonic distortion is measured with the device in the track mode, it gives only an estimate of true performance in a sampled data system. The specification includes none of the switching dynamics which occur in the dynamic sample-mode where the T/H toggles repeatedly between the track and hold modes. Actual dynamic performance, being a function of these switching dynamics, will depend on the clock signals supplied to both the T/H and A/D. When operating with con-

servatively-chosen clock signals, the T/H performance can be expected to closely approach these distortion levels given by the manufacturer. However, as the cycle time approaches the minimum as determined above, the distortion levels will worsen. Manufacturers prefer not to specify dynamic sample-mode harmonic distortion because of the difficulty of the measurement and its dependence upon more application-specific variables compared to the simple track-mode harmonic distortion test.

Part of the difficulty encountered in measuring dynamic sample-mode harmonic distortion is in finding a high-speed quantizer having an accuracy that will not limit the performance of the T/H. This problem is especially acute since T/Hs are used to improve quantizer accuracy. Not only does this quantizer require resolution and linearity exceeding that of the T/H under test, aperture time should also be insignificant so that it does not limit cycle time. In addition, the load impedance it presents to the T/H should be benign in order to allow the designer flexibility in simulating various loading on the T/H output. A quantizer system meeting these requirements can be constructed using a latching comparator with integrator feedback as described in reference 1. This system allows the designer the freedom of determining T/H performance independent of any realistic A/D it would drive. Using this quantizer can be a time-consuming effort if the quantizer must first be designed and constructed, but it is a valuable device for evaluating T/Hs. Because of the time involved, most designers make a T/H selection based upon available data sheet information and then evaluate the chosen device as part of the overall system. The trade-offs between the two approaches are obvious.

Output Loading

T/H output loading is one of the variables affecting harmonic distortion and DC nonlinearity. For the sake of maximum speed, most high-speed T/H designs utilize open-loop buffer amplifiers and, therefore, function best with as high a load impedance as possible. Because of this, it is best to avoid transmission lines and long traces between the T/H output and A/D input. A properly-terminated transmission line will degrade linearity because of the additional loading; an unterminated line will increase acquisition and settling time because of reflections. If a transmission line is necessary, it should be located before the T/H and the distance between the T/H and A/D kept as short as possible. If this is not possible, a closed-loop amplifier can be used to drive the line. This, of course, will increase cycle time because of the amplifier settling time. Heavy loading also increases thermal tail although this is not a problem with most A/D applications.

Also related to loading is the fact that high-speed amplifiers do not yield their best settling times when operating into the highly capacitive inputs of flash A/D converters without some assistance. Typically, this assistance is simply a series damping resistor placed between the T/H and A/D as in figure 2. The value of this resistor is, of course, important in minimizing acquisition time. Too small a value will cause excessive ringing and too large a value will excessively overdamp the output. The acquisition time of the T/H while driving the A/D input capacitance is the proper value to use when computing worst-case timing.

Hold-Mode Specifications

Hold-mode specifications that impact accuracy are droop rate and feedthrough rejection. Poor performance in these areas becomes apparent when evaluating dynamic sample mode performance. This again points to the usefulness of the above technique for evaluating T/H performance since many error sources contribute to the overall performance. These tests by themselves, however, do not pinpoint the specific cause of a problem.

Droop Rate

Droop rate can be a source of nonlinearity because the actual droop added to each sample is a function of the sampled voltage level. In the T/H block diagram of figure 1, this behavior is attributable to the FET used to buffer the hold capacitor node. Its gate current is a function of V_{GD}, which is nonlinearly dependent upon the sampled level. As a target, the T/H chosen should have droop less than 1/2 lsb from the time the amplifier enters the hold mode to when the A/D completes conversion. This assessment should be done at maximum operating temperature because FET gate current increases exponentially with temperature. Furthermore, the gate current will be greatest for the most negative input level since this is where V_{GD} is greatest.

Feedthrough Rejection

Feedthrough rejection, another hold-mode specification, has the potential for degrading accuracy by causing the held voltage level to change as the analog input to the T/H continues to change. As a rule of thumb, feedthrough rejection should be (6dB)(n + 1) or better at the maximum analog input frequency. In this equation, n represents the system accuracy in number of bits. Feedthrough rejection can degrade if power supply bypassing is not properly done. Sometimes the power supply pins for the input and output sections of the T/H are brought out separately. These devices offer superior performance since they allow the user to filter the supply line between the various sections and eliminate the power supply as an input-to-output coupling path during the hold period.

Aperture Jitter

Aperture jitter, the last specification within this group, has its dominant effect on the output noise floor of the A/D system. This random variation in effective aperture delay causes a random error in the held level of the T/H. The conversion factor from time error to voltage error is the slew rate of the analog input signal. Larger slew rates cause larger errors. As a result, the noise floor is a function of the analog input signal frequency, f. Specifically, for a sine wave input, the slew rate is simply a cosine wave and its rms slope is (reference 2):

$$\left.\frac{dv}{dt}\right|_{rms} = \frac{2\pi f V_p}{\sqrt{2}} \qquad (6)$$

where V_p is the peak value of the sine wave. A given aperture jitter, dt, in rms, will give rise to an rms noise level of:

$$e_n|_{rms} = \left.\frac{dv}{dt}\right|_{rms} (dt) \quad (7)$$

Since an ideal n-bit A/D converter is expected to give an rms-signal-to-rms-noise ratio of:

$$SNR = [1.8 + 6.02n]dB \quad (8)$$

for n-bit performance, T/H aperture jitter should be low enough so that the following equation is obeyed:

$$20Log_{10}\left[\frac{\frac{V_p}{\sqrt{2}}}{e_n|_{rms}}\right] \geq [1.8 + 6.02n]dB \quad (9)$$

Solving for dt,

$$dt \leq \frac{1}{1.2\,\pi f 2^{(n+1)}} \quad (10)$$

As an example, for 12-bit SNR with f = 10MHz, the aperture jitter should be less than 3.2ps rms. Intermediate frequency (IF) sampling applications place even more severe restrictions on aperture jitter. Because of its randomness, aperture jitter does not affect the dynamic sample mode harmonic distortion of the A/D system. Overall SNR will decrease beyond that determined using equation 9 because of amplifier noise, quantization noise, and distortion (Reference 3).

OTHER PERFORMANCE ISSUES

In choosing a T/H amplifier, the specifications covered above usually determine the selection since little can be done elsewhere in the circuit to correct problems resulting from these. Once the selection is made, a survey of the miscellaneous specifications indicates how convenient it will be to design the device into the system. This, of course, is not entirely true if the system has some unusual sensitivity to a particular miscellaneous specification, such as power dissipation in space-based systems, for example.

Offset voltage and temperature drift combine with pedestal offset and temperature drift to establish the DC offsets of the T/H. Typically, because other system components such as amplifiers and the A/D have offsets and drifts of their own, the system will incorporate an adjustment somewhere to null the initial offsets, and the drifts if it is of the self-calibrating type. Because the pedestal offset occurs only in the hold mode, it is important that the null be performed after the device enters the hold mode and before significant error caused by droop is incurred.

For some T/Hs, the pedestal offset can be dependent upon input voltage level; when this is the case, linearity can be affected. Unfortunately, this is a hidden danger since some manufacturers do not specify this effect when it is present. Poor performance here will show up during dynamic sample distortion measurements.

The effects of low bandwidth will show up in the acquisition time specification. Beyond this, frequency response will be of interest when the application is IF sampling or when the system includes precise filter functions that should be designed independent of the T/H amplifier response.

Similarly, insufficient slew rate can show up as a poor acquisition time specification and should be scrutinized when the application calls for IF sampling.

The input voltage range of the T/H should be consistent with the A/D being used since T/H amplifier performance is optimized for a given input range. Operation in conjunction with an A/D having a different range will add complexity by requiring the insertion of active components between the the T/H and A/D. Most high-speed A/D converters have a 2 volt input range either centered about 0 or −1 volt.

Protection Circuitry

Protection is another issue usually addressed during the design process. Although protection circuit design is specific to the devices that are to be protected, some general guidelines can be stated. Quite often the maximum input range of the A/D will either be close to that of the T/H or, more often, more restricting. Because of this, a clamp located before the T/H can be used to protect both the T/H and A/D from excessive input levels. Maximum safe input levels are usually far enough removed from the region of linear operation to allow simple diode clamping to be effective without impacting linearity.

A clamp just before the T/H cannot protect the A/D from failure of the T/H or from large T/H output voltages that might occur upon loss of the clock if the T/H is allowed to remain in the hold mode. The former problem can be simply solved by locating an additional diode clamp after the T/H. Current limit circuitry, notorious for limiting high-speed performance, can be omitted and the T/H allowed to operate directly into the clamp since activation of this second clamp implies damage has already occurred to the T/H. The latter problem, a result of droop, is avoided by forcing the T/H into the track mode on loss of the clock.

Finally, compatibility of the digital control input with a particular logic family is a matter of convenience. Some T/Hs are compatible with only one logic family while others can be configured for several.

SYSTEM TESTING

Once a T/H amplifier selection has been made, the device is either tested by itself in the dynamic sample mode as discussed above, or as part of the entire A/D system. Chances for success improve as the margin between specification and requirement increases. The most common tests to be used are beat frequency testing, which is useful in finding spurious and missing codes, and SNR testing, which evaluates overall dynamic system performance against that of the ideal converter SNR (References 4 and 5). Other tests exist as well for isolating particular faults.

Read Comlinear Application Note TH-06, "Track and Hold Amplifiers Improve Flash A/D Accuracy" for a discussion of the A/D system dynamic performance benefits that a T/H amplifier provides.

TRACK AND HOLD TERMINOLOGY

Acquisition Time (hold to track) is the time required for the track and hold to *acquire* the input signal to a specific settling precision when it switches from hold mode to track mode. It is the time from the point when the *output* starts changing to the point when the *output* has settled.

Analog Delay (input to output) is the time required for a signal to travel from the analog input to the analog output.

Aperture Jitter or aperture uncertainty is the sample-to-sample variability in Effective Aperture Delay which is caused by a small amount of noise in the switch control circuitry. Aperture Jitter changes the time at which the device goes into hold mode. Coupled with the rate of change (slew rate) of the signal at the storage capacitor, Aperture Jitter causes an error in the held output voltage. (Output voltage error = $\Delta V/\Delta t * \Delta t$, where $\Delta V/\Delta t$ is the slew rate and Δt is the Aperture Jitter.)

Droop Rate is a drift in the held output voltage. It is caused by leakage currents flowing into (or out of) the storage capacitor from the switching circuit and the input stage of the output amplifier.

Effective Aperture Delay tells when the input signal is actually being sampled. It takes into account two delays: 1) the input signal transit time through the input amplifier and 2) the time needed for the switch to open after the part is given the hold command. (Conceivably, Effective Aperture Delay could be negative if the transit time through the input amplifier were longer than the delay in the switch.)

Feedthrough Rejection or analog input isolation describes how well the switch keeps the input signals from "feeding through" to the output when the device is in hold mode. It is the ratio of the signal that passes through the open switch to the signal at the analog input. Since signal feedthrough is, in part, caused by the capacitance of the switch, Feedthrough Rejection is better for low-frequency input signals. There are, of course, switching transients which feed through from the digital inputs; however, these settle out quickly and are accounted for in the Acquisition Time and Track-to-Hold Settling Time specifications.

Hold-to-Track Switch Delay is the time delay from the track command to the point when the output voltage begins to change as it starts to acquire the new signal.

Pedestal Offset or track-to-hold offset is an output offset voltage found in hold mode. It is caused by a small amount of charge injected into (or out of) the storage capacitor when the (diode bridge) switch opens. In practice, this offset is treated just as an output offset voltage.

Track-to-Hold Switching Transient is the switch-induced transient voltage which appears at the output immediately after the device switches from track to hold.

Track-to-Hold Settling Time is the time required for the Track-to-Hold Switching Transient to settle out to the point where the output is within 1mV of its final value.

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Application Note TH-06

Track and Hold Amplifiers Improve Flash A/D Accuracy

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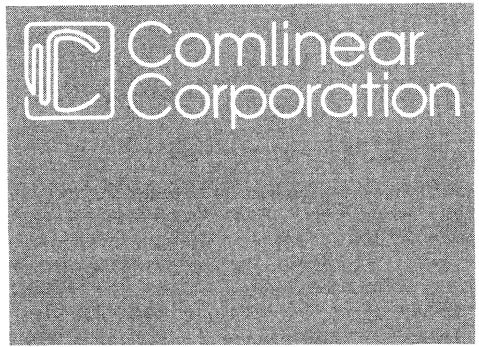


INTRODUCTION

The growing usage of flash A/D converters is testimony to the ever-higher sampling rates and bandwidths of high-speed systems. While this trend will, no doubt, continue, designers are now also demanding *accuracy* from their flash A/D systems. While this is possible at low speeds, it becomes increasingly difficult at high speeds. Specifically, at high signal bandwidths, flash A/D converters retain only a fraction of their low-speed accuracy. The solution to this dilemma is the use of a track and hold (T/H) amplifier to reduce or eliminate flash A/D errors.

FLASH A/D ERROR MECHANISMS

Flash A/D converters are so named because of their seemingly instantaneous conversion process. The architecture of the flash A/D shows this (see figure 1). Relative to other A/D architectures (such as dual slope integration or successive approximation), the flash A/D is indeed instantaneous. However, relative to the speed of high-speed analog input signals, this simplification of instantaneous conversion is not correct. Timing delays and variations which can be ignored at low frequencies become major sources of inaccuracy at high signal bandwidths.

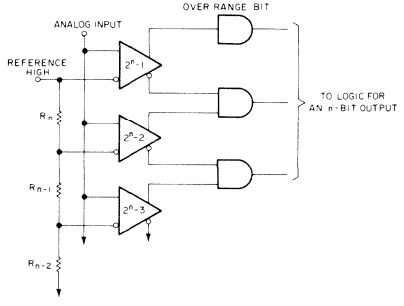


Figure 1: Simplified schematic of the flash A/D.

When the flash A/D architecture (figure 1) is reexamined in the context of wideband analog input signals, several potential error mechanisms are apparent. For example, the input comparators must receive the signal simultaneously and they all must be gated or latched simultaneously. The sheer complexity imposed by the 255 input comparators of an 8-bit device suggests that this will be difficult, if not impossible, for high-bandwidth analog signals. Circumventing the problems of this complicated input structure is exactly how a high-speed T/H improves accuracy.

THE TRACK AND HOLD CONTRIBUTION

Using a T/H transfers the burden of *acquiring* the signal from the complicated A/D input structure to the simple, single-element switch of the T/H (see figure 2). The task of *digitizing* the signal remains with the A/D, but now the comparators can operate on a signal level that remains constant during conversion. Most systems can benefit from this synergistic combination; fortunately, the performance improvement can be assessed quantitatively with the right test system. In the flash A/D system illustrated in this application note, for example, the signal to noise ratio was shown to improve by 17dB with the addition of the track and hold.

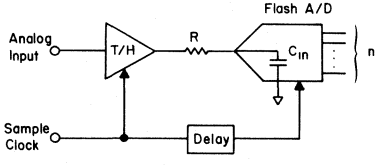


Figure 2: The use of a T/H transfers the burden of acquiring the signal from the complicated A/D input structure to the simple, single-element switch of the T/H.

MEASURING T/H ACCURACY CONTRIBUTION

There are many ways to test the performance of a high-speed A/D system (see reference). The method presented here was chosen with several objectives in mind: 1) the test system must be relevant to real A/D systems as they are used in real systems, 2) it should be easy to duplicate by others, and most importantly, 3) it must be experimentally correct. The test system is shown in figure 3.

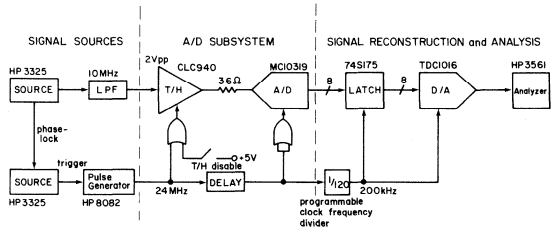


Figure 3: The T/H test system schematic shows the three blocks: signal sources, A/D subsystem, and signal reconstruction and analysis.

How the Test System Works

Conceptually, the system is quite simple. Central to the system is an 8-bit flash A/D system which includes a T/H that can be either active or inactive (see figure 3). Preceding the T/H are the signal sources which provide well characterized and controlled analog and switching signals. Following the A/D is a high-speed, high-resolution digital to analog (D/A) converter which reconstructs the analog input signal. Test equipment following the D/A then analyzes the signal in both the frequency and time domains. The difference in performance between the active and inactive states of the T/H shows the contribution of the T/H to system accuracy.

To understand the actual implementation, it is instructive to examine each of the three subsystems (signal sources, A/D, and reconstruction/analysis) in detail.

Signal Sources

Because of the analysis technique used (see "Interpreting the Frequency-Domain Graphs"), phase-locked signal sources are critical to the system (see figure 3). The analog signal source provides a 10MHz sine wave to the A/D subsystem; this is the signal which is digitized. The filter in the signal path is used to attenuate any harmonics which may be present in the 10MHz sine wave.

The sampling strobe (clock) is a 24MHz signal phase-locked to the analog signal source. A pulse generator is used to generate the logic levels compatible with the T/H and A/D.

A/D Subsystem

The A/D subsystem consists of a CLC940 track and hold and an MC10319 8-bit 25MSPS flash converter. This A/D was chosen for its low cost and low power consumption.

The A/D and T/H are each driven by a 24MHz clock signal. The OR gate before the T/H provides the ability to force the T/H into continual track mode; this permits a straightforward comparison of active and inactive T/H operation. (There is also an OR gate in the A/D clock signal, but this is included to compensate for the time delay caused by the other OR gate.) The time delay shown in the A/D clock signal compensates for the analog signal delay through the T/H.

The 36 ohm resistor between the T/H and A/D is used to maintain the critical damping of the T/H output stage while driving the 36pF input capacitance of the A/D input stage. This allows the acquisition time to be optimized. (The T/H data sheet shows the values of resistance required for other input capacitances.)

Signal Reconstruction and Analysis

Broadly speaking, there are two strategies in analyzing digitized signals: 1) reconstruction of the digital data to analog form followed by conventional analysis and 2) acquisition of the digital data

followed by manipulation and analysis. Each approach has its advantages and disadvantages. The first method, reconstruction and conventional analysis, is used here because it is easily duplicated with common test equipment and avoids the complexity involved in acquiring and then manipulating the digital data.

Reconstruction of the digitized analog signal is straightforward: the 8-bit A/D data is converted to analog by a 10-bit D/A. The D/A's output voltage is sent to a dynamic signal analyzer to show both the frequency-domain and time-domain performance. The only complexity is in the clocking scheme of the D/A converter which allows the use of readily-available test equipment.

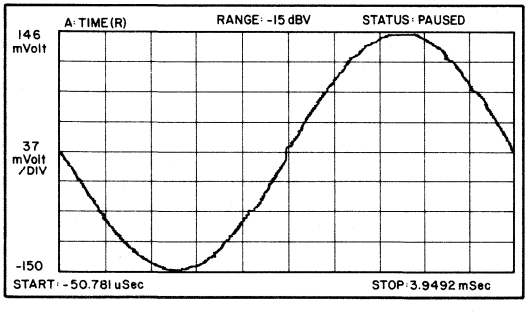
A divide-by-120 counter is used to generate the 200kHz D/A clock signal from the 24MHz A/D clock. Consequently, every 120th A/D sample is reconverted and analyzed by the test system. This produces a beat frequency which is a function of the analog input frequency and the 200kHz D/A clock; in effect, the beat frequency "walks through" the input signal. The benefit of this technique is that it provides full D/A accuracy while exercising the A/D under realistic conditions. Also, the relatively low reconstruction clock rate permits the beat frequency and the harmonics to appear in identical locations for every 200kHz increment in the analog test frequency. Consequently, the D/A operating conditions never change so that even small variations in D/A performance can be ruled out. See the section titled "Interpreting the Frequency-Domain Graphs" for a technical explanation of this analysis technique.

THE RESULTS

Time Domain

Figure 4 shows the time-domain performance of the A/D without and with the assistance of the T/H. The missing and spurious codes are obvious and especially so on the enlarged scale (figure 5). These problems typically amount to a reduction in accuracy of about 1-2 bits; the inaccuracy in some regions (zero-crossing region in particular) is much greater—effectively reducing the A/D's accuracy to only 4 bits or so.

4(a)



4(b)

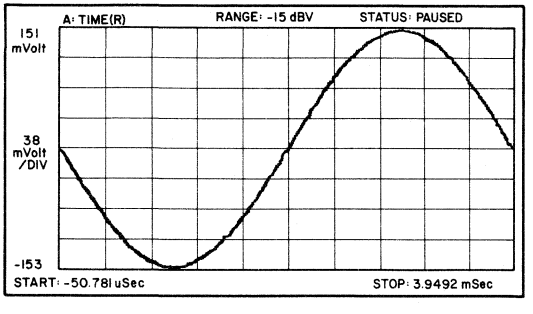


Figure 4: The MC10319 is operating at a sample rate of 24MSPS and an analog input of $2V_{pp}$, 10.000250MHz. Serious non-linearities are present in (a) with the CLC940 inactive. In (b), the CLC940 is activated and the non-linearities disappear.

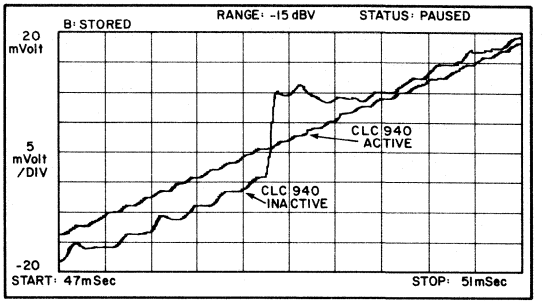


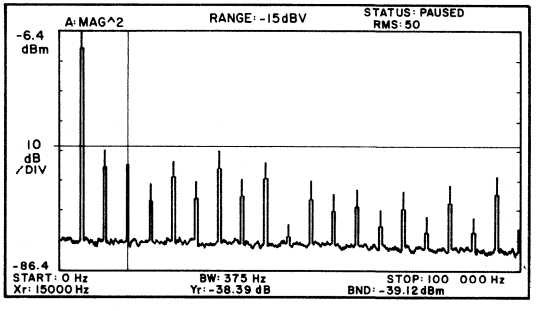
Figure 5: The zero-crossing region of figure 2 is expanded by reducing the analog input frequency to 10.0000625MHz. When the CLC940 is activated, a 12-LSB amplitude glitch is smoothed out. Lack of monotonicity in other areas is likewise eliminated. Time-record averaging is employed in both traces to eliminate noise.

Frequency Domain

As important, and often more useful, is the frequency-domain response of the system. Figure 6a shows the A/D performance with the T/H inactivated. The signal to noise ratio is 31.3dB and the total harmonic distortion is 32.8dB below the signal (since the distortion is so large, noise terms, such as would be caused by aperture uncertainty, are comparatively small). This value of signal to noise ratio indicates an effective accuracy of about five bits.

Figure 6b shows the performance improvement seen when the T/H is activated. The signal to noise ratio improves to 48.3dB (7.7-bit accuracy) and the total harmonic distortion improves to −53dB.

6(a)



6(b)

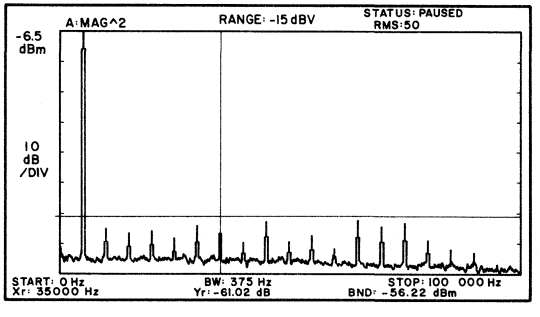


Figure 6: Operating at 24MSPS, a 10.005MHz, $2V_{pp}$ analog input signal yields elevated harmonics and noise floor (a). In (b), the CLC940 is activated and both the harmonics and noise floor are decreased, resulting in a SNR of 48.3dB.

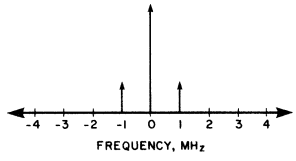
INTERPRETING THE FREQUENCY-DOMAIN GRAPHS

As mentioned previously, the test system shown in figure 3 samples the analog input signal at 24MHz yet reconstructs the signal at 200kHz. This provides the advantage of operating the reconstruction D/A at full accuracy and allows higher-speed A/Ds to be accommodated. The only disadvantage of this approach is the complexity of interpreting the frequency-domain results; fortunately, this complexity clears quickly as the theory is understood.

Aliasing

The concept of aliasing is straightforward. Simply put, the spectrum of the input signal is replicated at multiples of the sampling frequency (see figure 7). It is useful to note that the original signal is composed of both positive and negative frequency components, both of which are replicated through sampling. For example, a sinusoidal signal at 1MHz which is sampled at 10MHz will appear in the frequency domain at 1MHz, 9MHz, 11MHz 19MHz, 21MHz, etc. It will also have negative frequency domain components: −1MHz, −9MHz, −11MHz, etc.

7(a)



7(b)

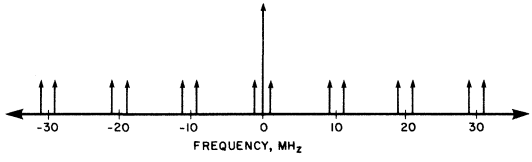


Figure 7: The frequency domain representation of a 1MHz sine wave is shown in (a). When this signal is sampled at 10MHz, the original spectrum is replicated at multiples of the sampling rate (b).

If the analog frequency is increased, its frequency domain representation will change. For an analog input signal of 7MHz the frequency components will be found at 3MHz, 7MHz, 13MHz, 17MHz, etc. with negative components existing as well. If the frequency increases to 14MHz, frequency components will be found at 4MHz, 6MHz, 14MHz, etc. Now take an 18MHz signal; its components will be at 2MHz, 8MHz, 12MHz, 18MHz, etc. Notice that in each case, the sampled signal is replicated in the $f_s/2$ Nyquist band once and only once regardless of the input signal. Through the concept of superposition, this discussion can be related to the spectrum of a complex signal.

Consider an analog signal composed of the four signals described above: 1MHz, 7MHz, 14MHz, and 18MHz (see figure 8). When it is sampled at a frequency f_s, the frequency components will be spread throughout the frequency domain (as one would expect); however, in the $f_s/2$ range, the frequency components appear once and only once. For a sampling frequency of 10MHz, these components appear at 1MHz, 2MHz, 3MHz, and 4MHz. (Noise present at the analog input signal is aliased the same way—all of the noise, regardless of frequency, is aliased into the $f_s/2$ band once and only once.)

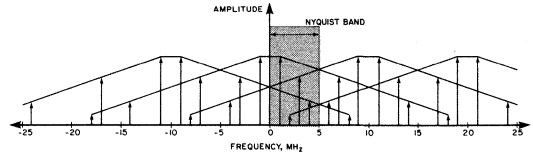


Figure 8: A complex signal having frequency components at 1MHz, 7MHz, 14MHz, and 18MHz is shown being sampled at 10MHz. The original spectrum is replicated at multiples of the sampling frequency. Note that the Nyquist band (f_s/z) contains all of the original components—each component is aliased in once and only once.

This same idea can be related directly to the test system where the analog frequency and all of its harmonics are greater than the 200kHz reconstruction frequency, but are aliased into the Nyquist band nonetheless. (In fact, the harmonics appear in ascending order due to the choice of the beat frequency.)

Signal to Noise Ratio Calculations

Signal to noise ratio is calculated as it would be for any ordinary signal but with one exception. The D/A converter functions as a zero-order hold and consequently, introduces a sinx/x characteristic having the first null at 200kHz. It is not corrected by the hardware, but fortunately, the effects of this can often be ignored since the attenuation is just 3.9dB at 100kHz ($f_s/2$) where the harmonics are of lesser magnitude. Also, the sinx/x characteristic reduces integrated system noise by 1.1dB. This and a 0.3dB error caused by the analyzer have been taken into account in the SNR value stated earlier.

Reference

B. Peetz, A. Muto, and J. Neil, "Measuring Waveform Recorder Performance," Hewlett Packard Journal, pp 21-29, November 1982.

Comlinear Corporation

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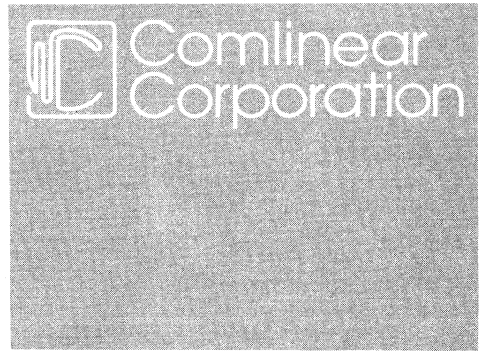
Spice Models
Contents

Simulation Macro-Models For Comlinear's Op Amps

Rea Schmid
Kumen Blake

This application note is updated as new products are released. Please check with Comlinear for latest revision.



MACROMODELS FOR HIGH SPEED AMPLIFIERS

INTRODUCTION

This application note is intended to support the *PSpice* macromodels for Comlinear's High Speed amplifiers. The macromodels offers the design engineer the ability to model typical amplifier circuit topologies. These models are intended to work with Pspice, but similar spice simulators can be used with the appropriate syntax modifications. The user is responsible for making those changes. The products available for simulation are summarized in the diskette's **readme** file using file names as shown in Table 1.

CLC400.CIR	CLC410.CIR	CLC430.CIR
CLC401.CIR	CLC414.CIR	CLC501.CIR
CLC402.CIR	CLC415.CIR	CLC502.CIR
CLC404.CIR	CLC420.CIR	CLC505.CIR
CLC406.CIR	CLC425.CIR	CLC520.CIR
CLC409.CIR		

The macromodel's net lists are saved on an IBM-compatible 1.2 MByte floppy diskette in ASCII format.

QUICK START

Place the diskette in a 1.2MByte drive and execute the **DIR** command. To print a listing of the macromodel subcircuits type the following command:

print [{drive}:\{file name}]

Comlinear suggests that files be copied to the Pspice library. If the user intends to access the diskette from a floppy drive, then the proper path must be established for Pspice. To access the macromodels from the floppy, use the Pspice **include command** in the circuit net list.

example: .INC A:\{file name}

UPDATE INFORMATION

The application diskette shows a revision number on the label. Please refer to this revision number when contacting Comlinear Corporation for additional assistance or model availability.

APPLICATION INFORMATION

The macromodels are configured as sub-circuits to allow easy inclusion into larger simulation files.

- Connect: NON-INVERTING INPUT
- | INVERTING INPUT
- | | OUTPUT
- | | | $+V_{cc}$
- | | | | $-V_{cc}$
- | | | | |
- SUBCKT() 3 2 6 7 4

Several schematic capture software programs require a different pin order for the inputs, outputs, supplies, etc., in the subckt (name) command line. If Comlinear's models do not work properly, check to see that the order is compatible with your software. Changing Comlinear pin order in the subckt command will not effect modeling capability. You must maintain the same pin **node** numbers. Substitution of high speed op amps into existing designs is welcome. If satisfactory results are not obtained for current feedback op amps then Comlinear suggests that you read application note OA-13, "Current Feedback Amplifier Loop Gain Analysis and Performance Enhancements". If you have a specific design application and need help choosing a correct part for your design, contact the application department of Comlinear.

These macromodels accurately simulate the **typical** performance for the following parameters:

DC Effects

- VIO, IBI, IBN
- Supply current vs. supply voltages
- Common Mode Input/Output Voltage range.
- Load current from supplies

AC Effects

- Frequency response vs. gain & load
- Open loop gain & phase
- Noise
- Small signal Input/Output Impedance.
- CMRR

Time Domain

- Rise and fall times
- Slew Rates

Special Features

- Output limiting
- Supply current adjustment
- Offset voltage adjustment
- Disable/enable time

Performance characteristics that are **NOT** modeled include:

- Breakdown & leakages due to excessive Vcc
- Part to Part variation
- Variation in performance vs. temperature.
- Fine scale settling performance
- Harmonic distortion
- Differential gain
- Differential phase
- Thermal tail
- Overdrive recovery time
- PSRR

LIMITATIONS

The macromodels were developed from measured data to match the actual performance on each of the devices modeled. Typical simulation results should closely match the characteristic performance plots shown in each of the op amp data sheets. Slight variations from the data sheet plots can be expected based on part to part variation and slight test fixture parasitics. Board and component parasitics, if known, should be included in any simulation for the most accurate performance. These macromodels are intended to provide the designer an easy means of evaluating full circuit performance with a variety of external components, and operating conditions. Good engineering practice advocates that a physical implementation of the desired circuit also be implemented prior to production. Since the macromodels do not incorporate worst case performance characteristics, the data sheet specifications should be used as a predictor of the range of operation that would be expected. Comlinear offers a selection of evaluation boards to assist in the engineering evaluation of any of the parts discussed in these macromodels.

The macromodels use internal references to a global ground node. Ground currents in simulation are simply a modeling artifact since none of the physical op amps use a separate ground reference.

An example Pspice simulation file using the CLC400 to test the small signal frequency response at a gain of +2 is shown below. Comparing the results of the simulation, in Figure 2, to the data sheet typical plots shows excellent correlation.

```
* CLC400 magnitude plot @ gain 2
* subcircuit included
* connections
*
* non-inverting input
* |  inverting input
* |  |  output
* |  |  |  +Vcc
* |  |  |  |  -Vcc
* |  |  |  |  |  offset adj.
* |  |  |  |  |  |
x1 3  2  6  7  4  1  CLC400
*
* Define power pins
  +Vcc 7 0 5V
  -Vcc 4 0 -5V
*
* Define signal sources
  Vin 10 0 AC 2
*
* External resistors and caps
*
  Rs    10 3  50
  Rf    6  2  250
  Rg    2  0  250
  Rload 6  0  100
  Rin   3  0  50
  C     1  0  .1u
*
* Simulation parameters
*
.INC CLC400.CIR
*
.AC DEC 20 100KHZ 500MEG
*
.PROBE ALL
.END
```

PRODUCT HIGHLIGHTS

CLC400
FAST SETTLING, WIDEBAND LOW-GAIN MONOLITHIC OP AMP

- -3dB bandwidth of 200MHz (A_v = +2)
- 0.05% settling in 12ns
- low power, 150mW
- low distortion, -65dBc @ 10MHz
- rise and fall times of 1.6ns
- input offset voltage adjustment

CLC401
FAST SETTLING, HIGH-GAIN MONOLITHIC OP AMP

- -3dB bandwidth of 150MHz
- 0.1% settling in 10ns
- low power (150mW)
- ±7 to ±50 gain

CLC402
LOW-GAIN OP AMP WITH FAST 14-BIT SETTLING

- 0.0025% settling in 25ns (32ns max.)
- 0.5mV input offset voltage, 3µV/°C drift
- ±1 to ±8 closed-loop gain range
- low power (150mW)
- 0.01%/0.05° differential gain/phase

CLC404
HIGH-SLEW RATE WIDEBAND MONOLITHIC OP AMP

- 165MHz large signal bandwidth ($5V_{pp}$)
- 2600 V/µs slew rate
- low distortion, -53dBc @ 20MHz
- 0.07% differential gain, 0.03° differential phase

CLC406
WIDEBAND, LOW POWER MONOLITHIC OP AMP

- 160MHz small signal bandwidth (A_v = +6)
- 50mW power (±5V supplies)
- 0.02%/0.02° differential gain/phase
- 12ns settling to 0.05%
- 1500V/µs slew rate
- 2.2ns rise and fall time ($2V_{pp}$)

CLC409
VERY WIDEBAND, LOW-DISTORTION MONOLITHIC OP AMP
- 350 MHz small signal bandwidth @ A_v = +2
- -65/-72dBc 2nd/3rd harmonics (20MHz)
- low noise
- 8ns settling to 0.1%
- 1200 V/µs slew rate

CLC410
FAST SETTLING, VIDEO OP AMP WITH DISABLE.
- -3dB bandwidth of 200MHz (A_v = +2)
- 0.05% settling in 12ns
- low power, 160mW(40mW disabled)
- low distortion, -65dBc @ 10MHz
- fast disable (200ns)
- low differential gain/phase: 0.01%/0.01°
- input offset voltage adjustment

CLC414
QUAD, LOW-POWER MONOLITHIC OP AMP
- 90MHz small signal bandwidth
- 2mA quiescent supply current per amplifier
- 70dB channel isolation @ 5MHz
- 3.3ns rise and fall time (2Vpp)

CLC415
QUAD, WIDE-BANDWIDTH MONOLITHIC OP AMP
- 160MHz small signal bandwidth
- 5mA quiescent supply current per amplifier
- 70dB channel isolation @ 5MHz
- 0.03%/0.03° differential gain/phase

CLC420A
HIGH-SPEED UNITY GAIN VOLTAGE FEEDBACK
- 300MHz small signal bandwidth (A_v = +1)
- 1100 v/µs slew rate
- 0.01% settling in 18ns
- 2pA √Hz input current noise
- 4.2 nv/√Hz input noise voltage

CLC425
ULTRA LOW NOISE WIDEBAND OP AMP
- 1.7GHz gain-bandwidth product
- 1.05nV/√Hz input noise voltage
- 1.6pA/√Hz input current noise
- 100µV input offset voltage, 2µV/°C drift
- 100dB CMRR, 95dB PSRR
- 350Vµs slew rate
- 15mA to 5mA adjustable supply current
- gain range ±10 to ±1000V/V

CLC430
LOW-GAIN OP AMP WITH DISABLE
- 55MHz small signal bandwidth (4Vpp) (Av = +2)
- 2000 V/µs slew rate
- ±5V to ±15V supplies
- 100ns disable to high-impedance output
- 0.05%/0.05° differential gain/phase
- high common mode input voltage

CLC501
HIGH-GAIN, OUTPUT-LIMITING AMPLIFIER
- 110MHz small signal bandwidth (A_v = +20)
- bipolar output limiting (V_{high} and V_{low})
- 1ns recovery from clamping/overdrive
- 0.05% settling in 12ns

CLC502
CLAMPING, LOW-GAIN OP AMP WITH FAST 14-BIT SETTLING
- output clamping with fast recovery
- 0.0025% settling in 25ns (32ns max.)
- low power (170mW)
- low distortion, -50dBc at 20MHz

CLC505
WIDEBAND ADJUSTABLE SUPPLY CURRENT MONOLITHIC OP AMP
- specified operation at 1mA, 3.3mA, and 9mA
- 3.4mA I_{cc} provides 100MHz bandwidth (A_v = +6)
- 0.04%/0.06° differential gain/phase at I_{cc} = 3.4mA

CLC520
AMPLIFIER WITH VOLTAGE CONTROLLED GAIN, AGC+*Amp*
- 160MHz, -3dB bandwidth
- 2000 V/µs slew rate
- 0.04% signal nonlinearity at $4V_{pp}$ output
- -43dB feedthrough at 30MHz
- user adjustable gain range
- differential voltage input and single-ended voltage output

NOTICE

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January 1993

Packaging and Die Information

Contents

*where applicable

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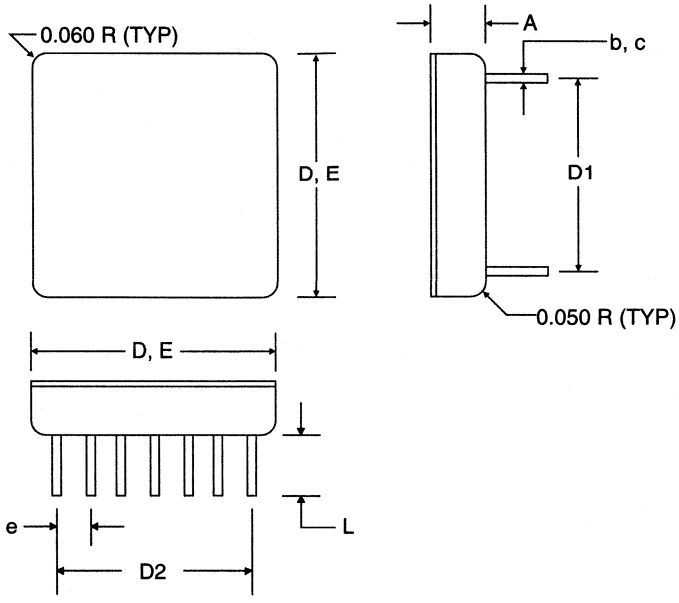
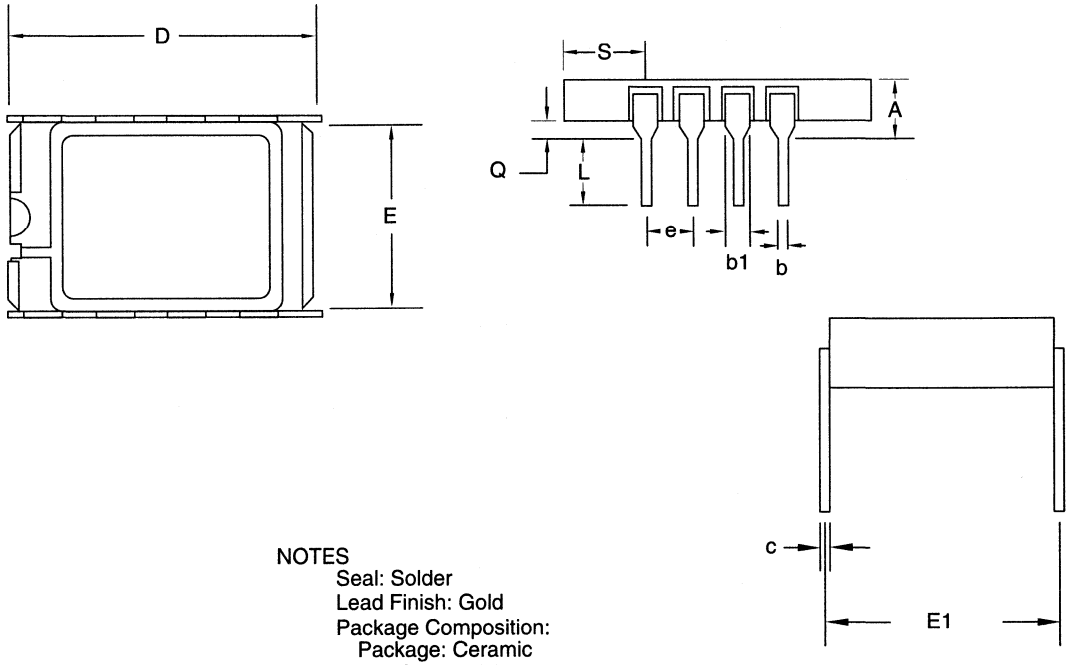
14-Pin Double-Wide DIP Package



NOTES Seal: Seam Weld
Lead Finish: Gold
Package Composition:
Package: Metal Package Properties
Lid: Type A per MIL-M-38510

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.140	0.180	3.56	4.57
b,c	0.016	0.020	0.41	0.51
D,E	0.740	0.760	18.80	19.30
D1,D2	0.590	0.610	14.99	15.49
e	0.090	0.110	2.29	2.79
L	0.240	0.260	6.10	6.60

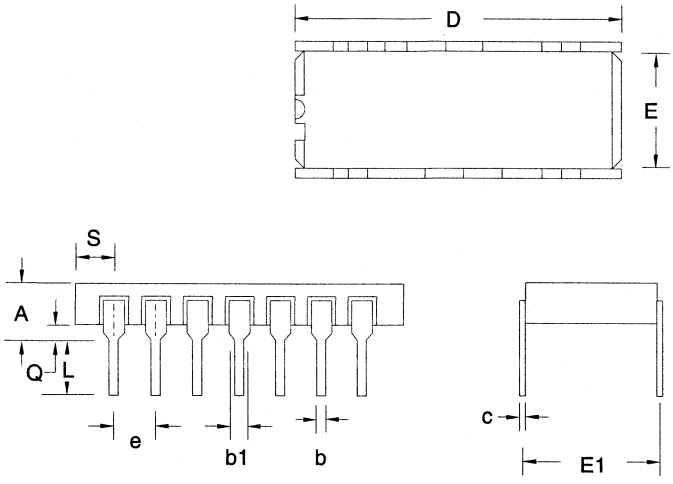
8-Pin Side-Brazed Ceramic DIP



NOTES
- Seal: Solder
- Lead Finish: Gold
- Package Composition:
  - Package: Ceramic
  - Lid: Gold Finish
  - Lead Material: Iron/Nickel Alloy
  - Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.200		5.08
b	0.014	0.026	0.36	0.66
b1	0.054 BSC		1.37 BSC	
c	0.008	0.018	0.20	0.46
D	0.386	0.405	9.80	10.29
E	0.220	0.310	5.59	7.87
E1	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S	0.030	0.060	0.76	1.52

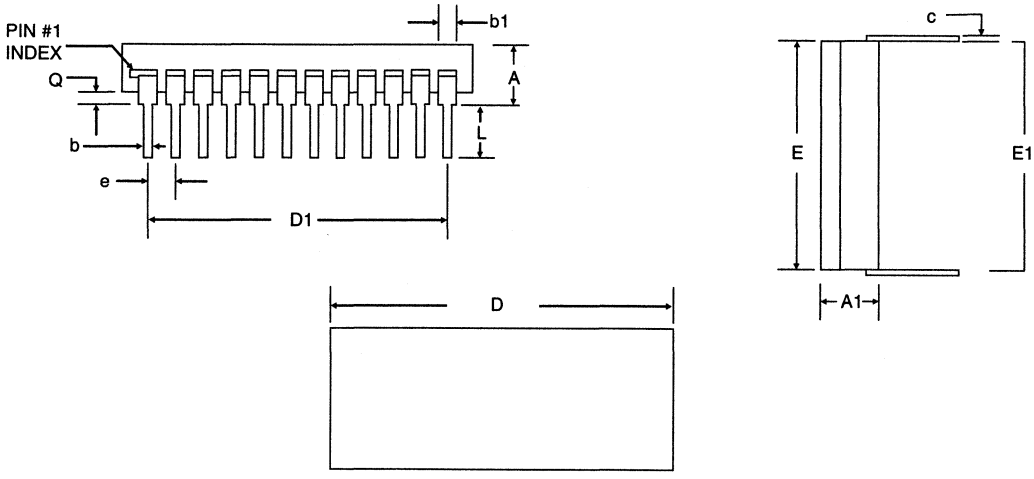
14-Pin Side-Brazed Ceramic DIP



NOTES Seal: Solder
Lead Finish: Gold
Package Composition:
Package: Ceramic
Lid: Gold Finish
Lead Material: Iron/Nickel Alloy
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.200		5.08
b	0.014	0.026	0.36	0.66
b1	0.054 BSC		1.37 BSC	
c	0.008	0.018	0.20	0.46
D	0.693	0.705	17.60	19.94
E	0.220	0.310	5.59	7.87
E1	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S	0.030	0.060	0.76	1.52

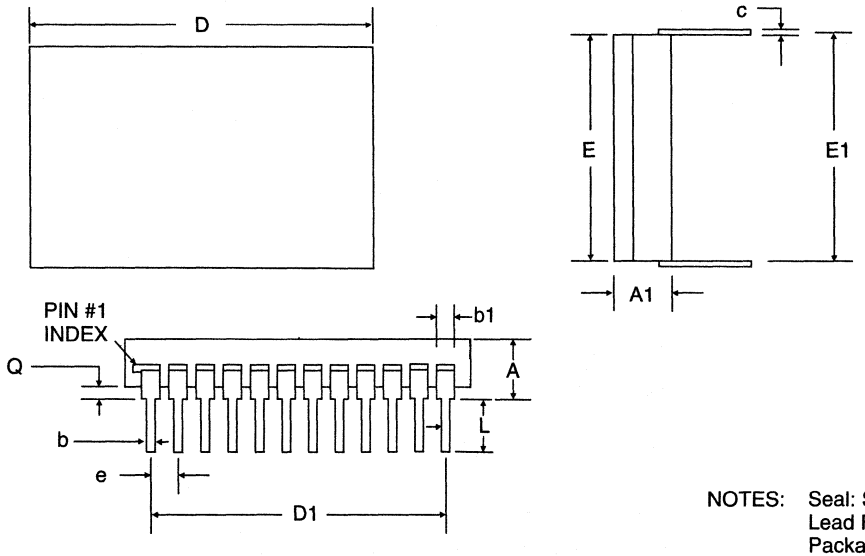
24-Pin 0.6" Side-Brazed Ceramic DIP



NOTES Seal: Seam Weld
Lead Finish: Gold Finish
Package Composition:
Package: Ceramic
Lid: Kovar/Nickel
Leadframe: Alloy 42
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.225		5.72
A1	0.139	0.192	3.53	4.88
b	0.014	0.026	0.36	0.66
b1	0.050 BSC		1.27 BSC	
c	0.008	0.018	0.20	0.46
D	1.190	1.290	30.23	32.77
D1	1.095	1.105	27.81	28.07
E	0.500	0.610	12.70	15.49
E1	0.600 BSC		15.24 BSC	
e	0.100 BSC		2.54 BSC	
L	0.165 BSC		4.19 BSC	
Q	0.015	0.075	0.38	1.91

24-Pin 0.8" Side-Brazed Ceramic DIP

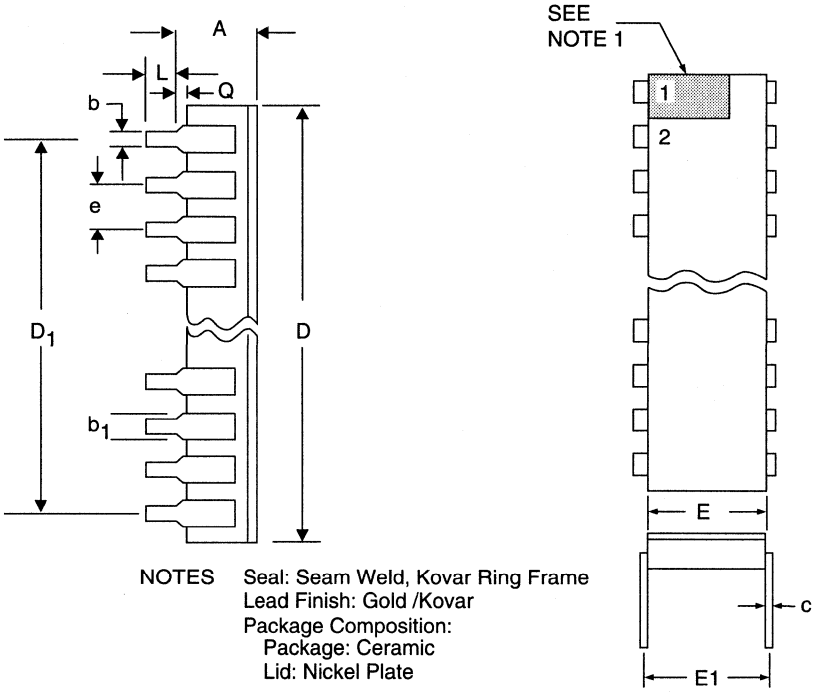


NOTES: Seal: Seam Weld
Lead Finish: Gold
Package Composition:
Package: Ceramic
Lid: Kovar/Nickel
Leadframe: Alloy 42
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A-METAL LID	0.180	0.240	4.57	6.10
A-CERAMIC LID	0.195	0.255	4.95	6.48
A1-METAL LID	0.145	0.175	3.68	4.45
A1-CERAMIC LID	0.160	0.190	4.06	4.83
b	0.014	0.026	0.36	0.66
b1	0.050 BSC		1.27 BSC	
c	0.008	0.018	0.20	0.46
D	1.275	1.310	33.39	33.27
D1	1.095	1.105	27.81	28.07
E	0.785	0.815	19.94	20.70
E1	0.790	0.810	20.07	20.57
e	0.100 BSC		2.54 BSC	
L	0.165 BSC		4.19 BSC	
Q	0.015	0.075	0.38	1.91

13

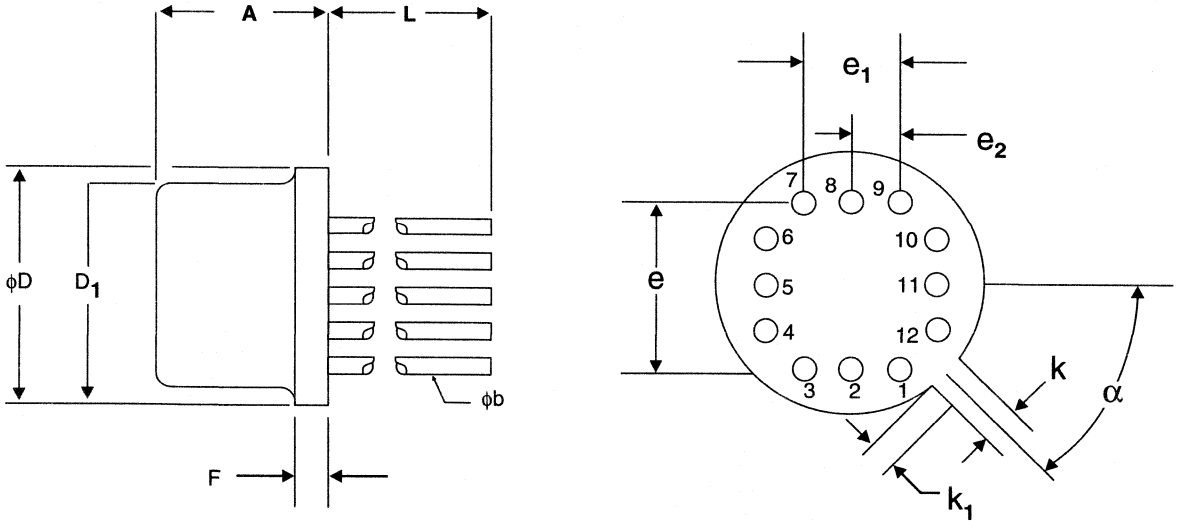
40-Pin Side-Brazed Ceramic DIP



NOTES
Seal: Seam Weld, Kovar Ring Frame
Lead Finish: Gold /Kovar
Package Composition:
Package: Ceramic
Lid: Nickel Plate

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.198	0.252	5.03	6.40
b	0.014	0.026	0.36	0.66
b1	0.050 BSC		1.270 BSC	
c	0.008	0.018	0.20	0.46
D	2.075	2.115	52.71	53.72
D1	1.892	1.908	48.06	48.46
E	1.100 BSC		27.940 BSC	
E1	1.096 BSC		27.84 BSC	
e	0.100 BSC		2.54 BSC	
L	0.175 BSC		4.45 BSC	
Q	0.015	0.070	0.38	1.78

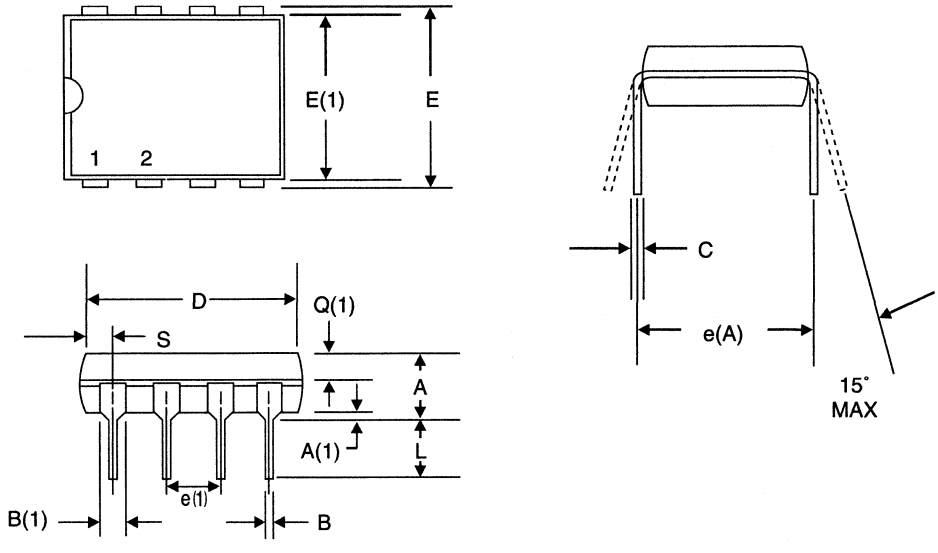
12-Pin TO-8 Metal Can



NOTES Seal: Cap Weld
Lead Finish: Gold per MIL-M-38510
Package Composition:
Package: Metal
Lid: Type A per MIL-M-38510

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.142	0.181	3.61	4.60
ϕb	0.016	0.019	0.41	0.48
ϕD	0.595	0.605	15.11	15.37
ϕD_1	0.543	0.555	13.79	14.10
e	0.400 BSC		10.16 BSC	
e_1	0.200 BSC		5.08 BSC	
e_2	0.100 BSC		2.54 BSC	
F	0.016	0.030	0.41	0.76
k	0.026	0.036	0.66	0.91
k_1	0.026	0.036	0.66	0.91
L	0.310	0.340	7.87	8.64
α	45° BSC		45° BSC	

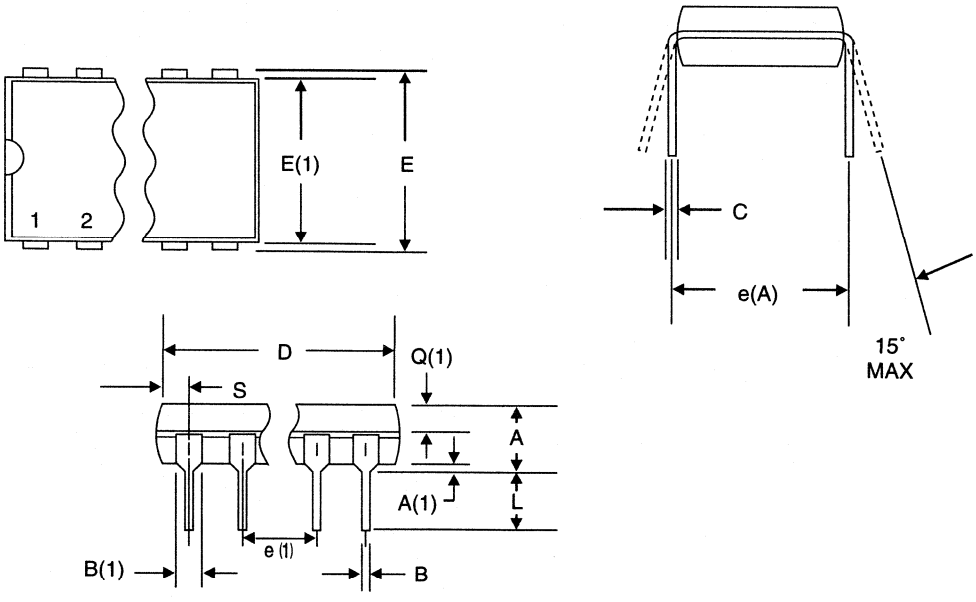
8-Pin Plastic DIP



NOTES Lead Finish: Solder
Package Composition:
Package: Plastic
Lead Frame: Copper/Iron
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.145	0.200	3.68	5.08
A(1)	0.015	0.050	0.38	1.27
B	0.015	0.020	0.38	0.51
B(1)	0.035	0.065	0.89	1.65
C	0.008	0.012	0.20	0.30
D	0.370	0.460	9.40	11.68
E	0.300	0.325	7.62	8.26
E(1)	0.220	0.280	5.59	7.11
e(1)	0.090	0.110	2.29	2.79
e(A)	0.290	0.310	7.37	7.87
L	0.120	0.150	3.05	3.81
Q(1)	0.050	0.080	1.27	2.03
S	0.040	0.080	1.02	2.03

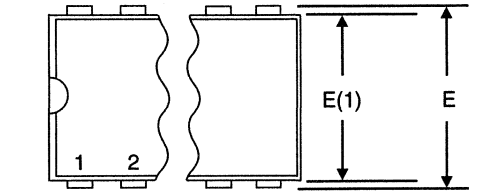
14-Pin Plastic DIP

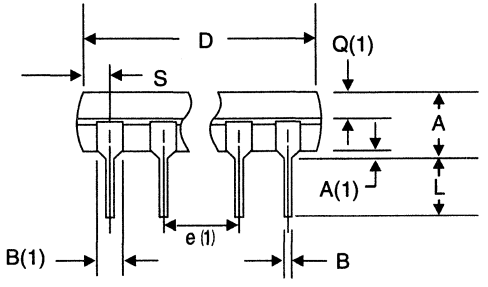


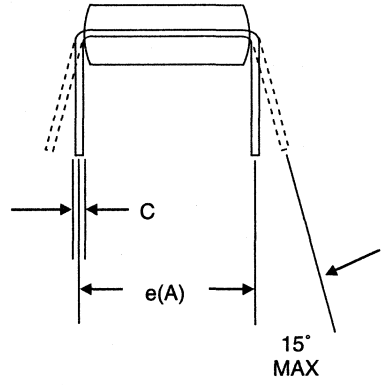
NOTES Lead Finish: Solder
Package Composition:
Package: Plastic
Lead Frame: Copper/Iron
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.145	0.200	3.68	5.08
A(1)	0.015	0.050	0.38	1.27
B	0.015	0.020	0.38	0.51
B(1)	0.035	0.065	0.89	1.65
C	0.008	0.012	0.20	0.30
D	0.680	0.770	17.27	19.56
E	0.300	0.325	7.62	8.26
E(1)	0.220	0.280	5.59	7.11
e(1)	0.090	0.110	2.29	2.79
e(A)	0.290	0.310	7.37	7.87
L	0.120	0.150	3.05	3.81
Q(1)	0.050	0.080	1.27	2.03
S	0.040	0.080	1.02	2.03

16-Pin Plastic DIP



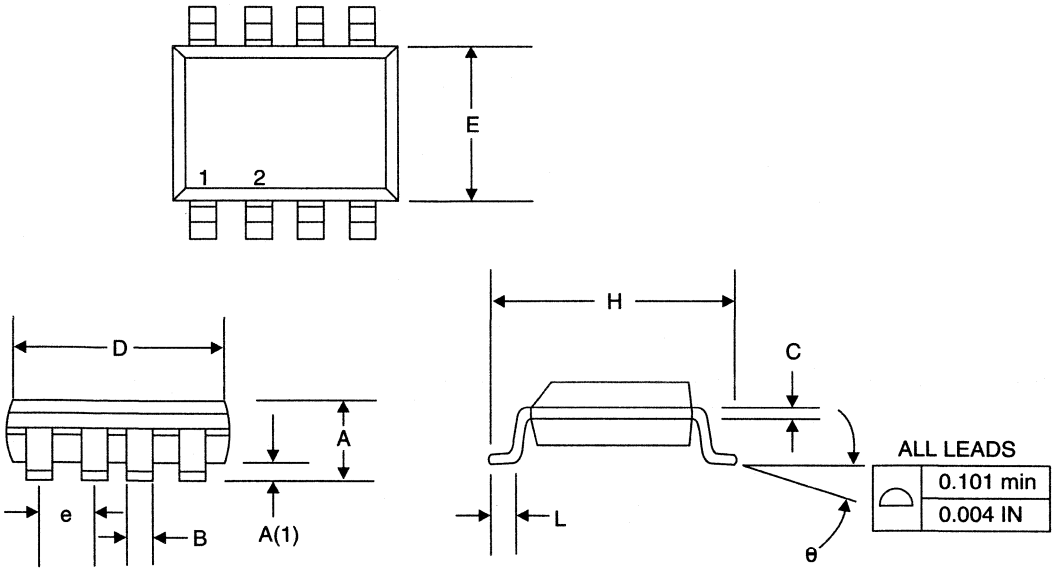




NOTES
Lead Finish: Solder
Package Composition:
Package: Plastic
Lead Frame: Alloy 42
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.145	0.200	3.68	5.08
A(1)	0.015	0.050	0.38	1.27
B	0.015	0.020	0.38	0.51
B(1)	0.035	0.065	0.89	1.65
C	0.008	0.012	0.20	0.30
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E(1)	0.220	0.280	5.59	7.11
e(1)	0.090	0.110	2.29	2.79
e(A)	0.290	0.310	7.37	7.87
L	0.120	0.150	3.05	3.81
Q(1)	0.050	0.080	1.27	2.03
S	0.015	0.060	0.38	1.52

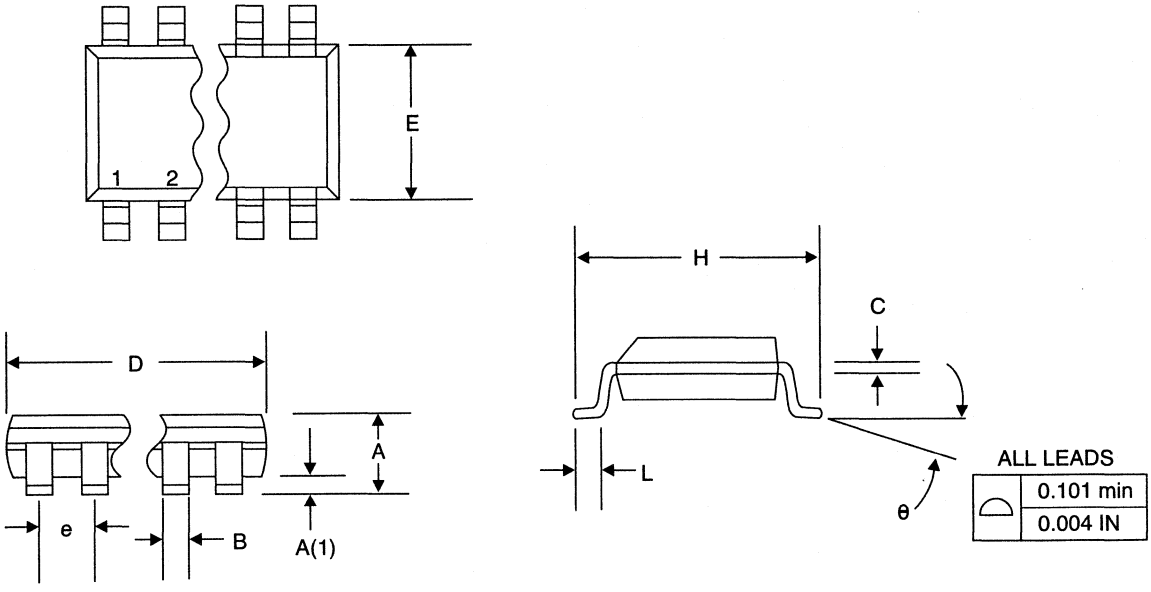
8-Pin Plastic SOIC



NOTES Lead Finish: Solder
Package Composition:
Package: Plastic
Lead Frame: Copper/Iron
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.053	0.069	1.35	1.75
A(1)	0.004	0.010	0.10	0.25
B	0.014	0.019	0.36	0.48
C	0.007	0.009	0.18	0.23
D	0.181	0.205	4.60	5.20
E	0.140	0.160	3.56	4.06
e	0.050 BSC		1.27 BSC	
H	0.224	0.248	6.59	6.30
L	0.016	0.50	0.40	1.27
θ	0°	8°	0°	8°

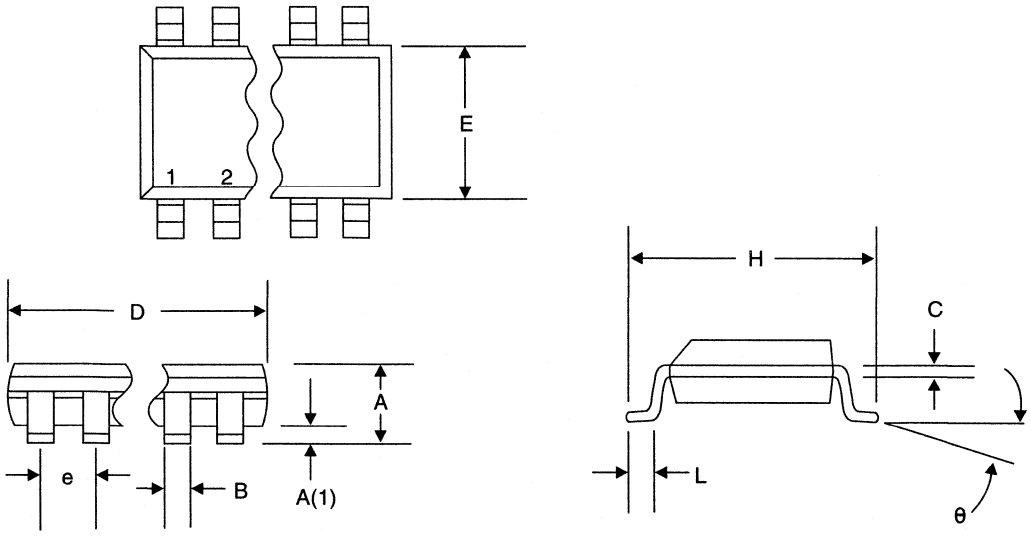
14-Pin Plastic SOIC



NOTES Lead Finish: Solder
Package Composition:
Package: Plastic
Leadframe: Copper/Iron
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.053	0.069	1.35	1.75
A(1)	0.004	0.010	0.10	0.25
B	0.014	0.019	0.36	0.48
C	0.007	0.009	0.18	0.23
D	0.329	0.352	8.36	8.94
E	0.140	0.160	3.56	4.06
e	0.050 BSC		1.27 BSC	
H	0.224	0.248	5.69	6.30
L	0.016	0.50	0.40	1.27
θ	0°	8°	0°	8°

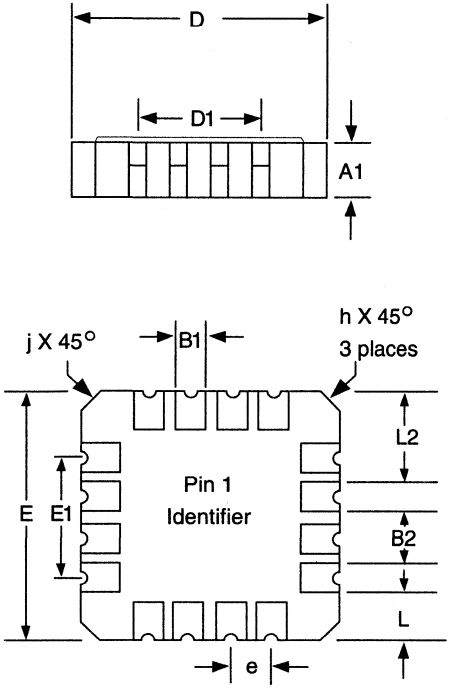
16-Pin Plastic SOIC



NOTES Lead Finish: Solder
Package Composition:
Package: Plastic
Leadframe: Copper
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.053	0.069	1.35	1.75
A(1)	0.004	0.010	0.10	0.25
B	0.014	0.019	0.36	0.48
C	0.007	0.009	0.18	0.23
D	0.378	0.402	9.60	10.21
E	0.140	0.160	3.56	4.06
e	0.050 BSC		1.27 BSC	
H	0.224	0.248	5.69	6.30
L	0.016	0.50	0.40	1.27
θ	0°	8°	0°	8°

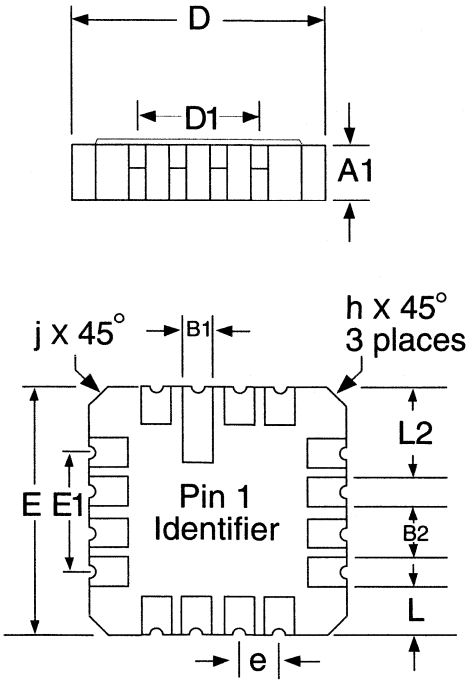
16-Terminal Leadless Chip Carrier



Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A1	0.050	0.088	1.27	2.23
B1	0.022	0.028	0.56	0.71
B2	0.072 REF		1.83 REF	
D,E	0.245	0.308	6.22	7.82
D1,E1	0.150 BSC		3.81 BSC	
e	0.050 BSC		1.27 BSC	
h	0.040 REF		1.02 REF	
j	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41

NOTES Seal: Solder
Lead Finish: Solder
Package Composition:
Package: Ceramic
Lid: Gold
Die Attach: Eutectic

20-Terminal Leadless Chip Carrier

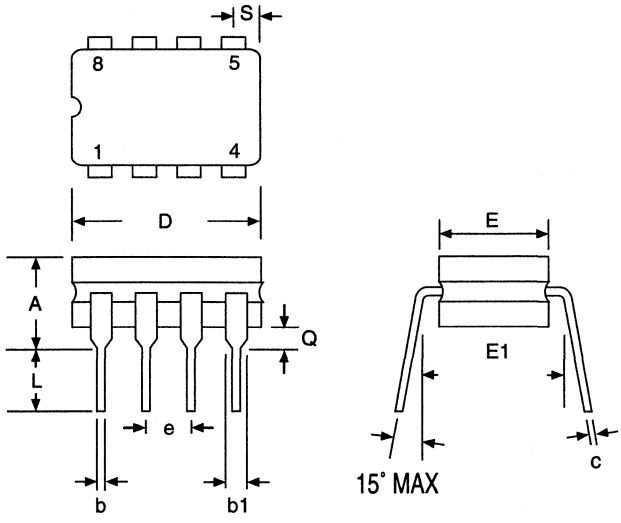


Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A1	0.050	0.088	1.27	2.23
B1	0.022	0.028	0.56	0.71
B2	0.072 REF		1.83 REF	
D,E	0.342	0.358	8.69	9.09
D1,E1	0.200 BSC		5.08 BSC	
e	0.050 BSC		1.27 BSC	
h	0.040 REF		1.02 REF	
j	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41

NOTES
Seal: Solder
Lead Finish: Solder
Package Composition:
Package: Ceramic
Lid: Gold
Die Attach: Eutectic

13

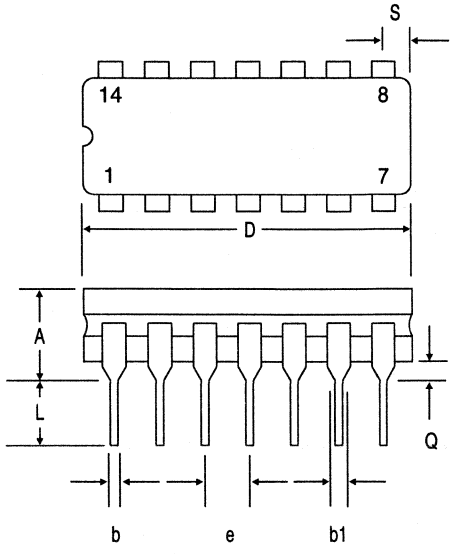
8-Pin CERDIP

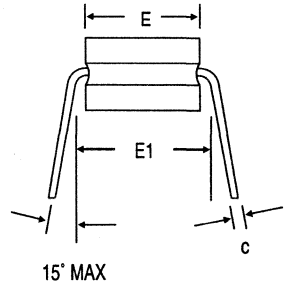


NOTES Seal: Glass
Lead Finish: Solder
Package Composition:
Package: Ceramic
Leadframe: Kovar
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.200		5.08
b	0.014	0.026	0.36	0.66
b1	0.054 BSC		1.37 BSC	
c	0.008	0.018	0.20	0.46
D	0.386	0.405	9.80	10.29
E	0.220	0.310	5.59	7.87
E1	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S	0.030	0.060	0.76	1.52

14-Pin CERDIP

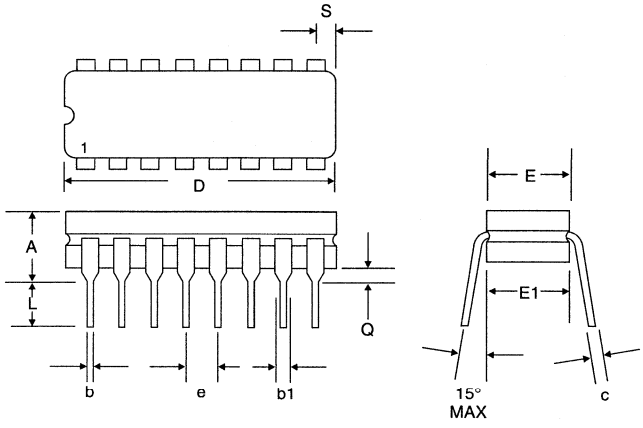




NOTES Seal: Glass
Lead Finish: Solder
Package Composition:
Package: Ceramic
Leadframe: Kovar
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.200		5.08
b	0.014	0.026	0.36	0.66
b1	0.054 BSC		1.37 BSC	
c	0.008	0.018	0.20	0.46
D	0.693	0.785	17.60	19.94
E	0.220	0.310	5.59	7.87
E1	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S	0.030	0.060	0.76	1.52

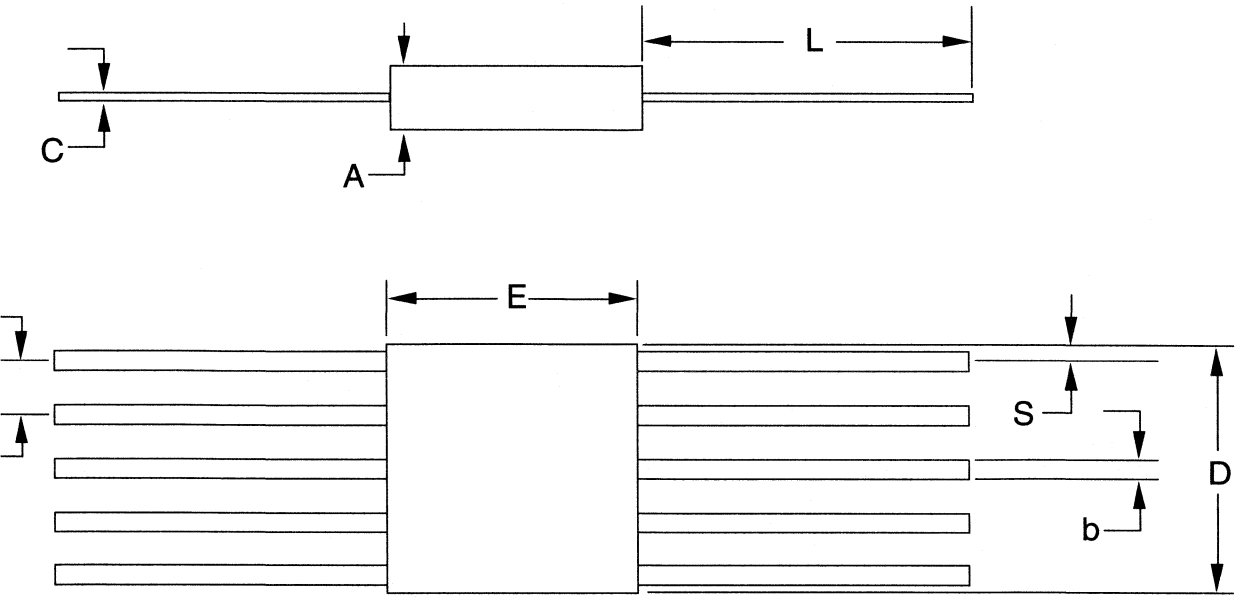
16-Pin CERDIP



NOTES Seal: Glass
Lead Finish: Solder
Package Composition:
Package: Ceramic
Leadframe: Kovar
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.200		5.08
b	0.014	0.026	0.36	0.66
b1	0.054 BSC		1.37 BSC	
c	0.008	0.018	0.20	0.46
D		0.840		19.94
E	0.220	0.310	5.59	7.87
E1	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S	0.030	0.060	0.76	1.52

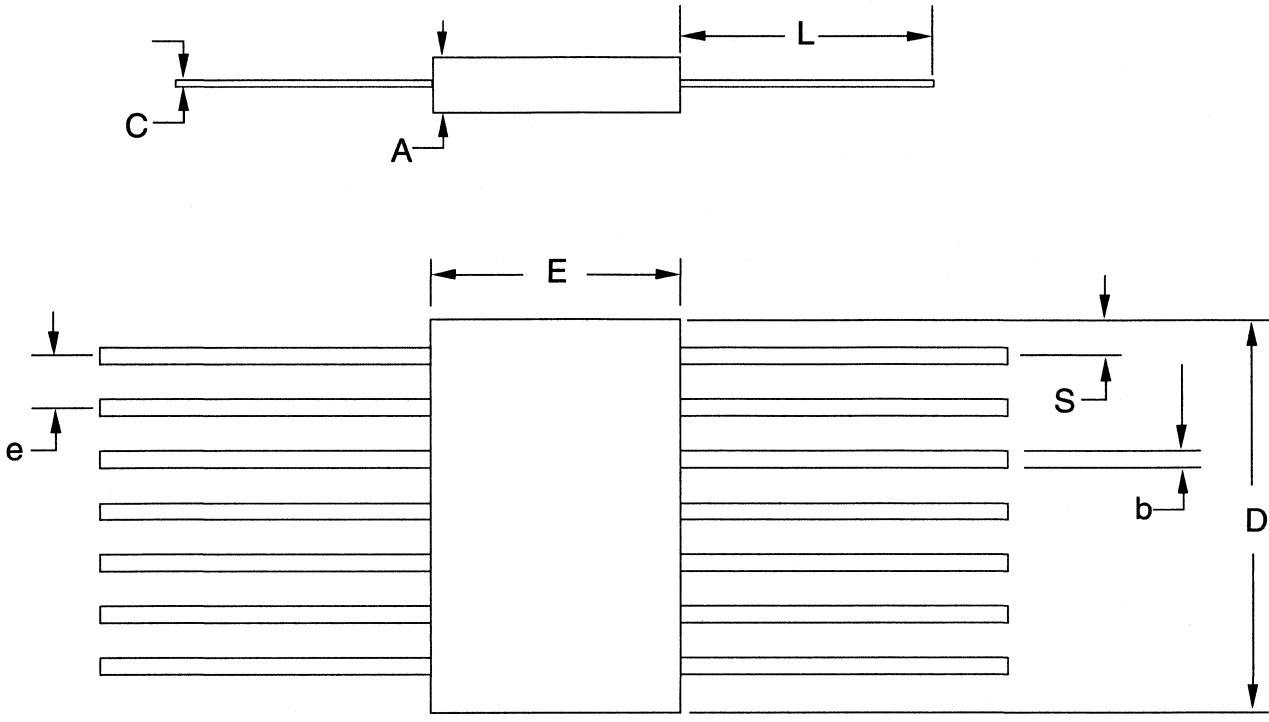
10-Pin CERPACK



NOTES Seal: Glass
Lead Finish: Solder
Package Composition:
Package: Ceramic
Leadframe: Kovar
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.045	0.090	1.14	2.29
b	0.010	0.022	0.25	0.56
C	0.003	0.009	0.08	0.23
D		0.280		7.11
E	0.238	0.260	6.05	6.60
e	0.050 BSC		0.127 BSC	
L	0.250	0.370	6.35	9.40

14-Pin CERPACK



NOTES Seal: Glass
Lead Finish: Solder
Package Composition:
Package: Ceramic
Leadframe: Kovar
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.045	0.085	1.14	2.16
b	0.010	0.022	0.25	0.56
C	0.003	0.009	0.08	0.23
D		0.390		9.906
E	0.235	0.260	5.97	6.60
e	0.050 BSC		0.127 BSC	
L	0.250	0.370	6.35	9.40

DIE INFORMATION

In an effort to better serve our customers' high performance, high speed, custom needs, Comlinear is offering the monolithic products in die form. Both the ALC and AMC versions are 100% probe tested to +25°C data sheet electricals and 100% visually inspected. In addition, the AMC version includes element evaluation per method 5008 of MIL-STD-883.

PHYSICAL CHARACTERISTICS

Metalization:	Top – Gold, 1 μm min. thickness (Bond Pads); Back – Gold
Passivation:	S_iON, 0.7 μm min.
Die Thickness:	14 mils, ± 2 mils
Die Size:	See applicable data sheet
Bond Pad:	4 mils × 4 mils min.

ELECTRICAL CONNECTIONS

The back side of the die is internally connected to $-V_{cc}$. It is not necessary to electrically connect the back side to the minus supply.

VISUAL INSPECTION

All wafers are visually inspected per the requirements outlined in MIL-STD-883, method 2010, Level B.

TRACEABILITY

All devices are traceable back to the wafer lot. All documentation relating to each wafer lot will be maintained for a minimum of three years.

PACKAGING

All dice are packaged in anti-static waffle pack (10 per pack minimum), face-up oriented for automatic assembly. All dice are considered static sensitive per MIL-M-38510 and should be handled as such. For class ratings see Section 13.

ORDERING INFORMATION

See Section 15 or contact factory.

PROCESS FLOWS

ALC DICE PROCESSING FLOWCHART

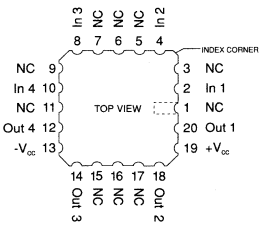
100% DC Probe to
+25°C Data Sheet Electricals
↓
Wafer Saw
and DI Water Rinse
↓
Wafer Inspection
↓
Wafer Lot
Qualification
↓
Die Sort
Into Waffle Packs
↓
100% Die Visual
Inspection to
M2010 MIL-STD-883
↓
QA Sample Visual
Inspection and
Document Review
↓
Seal in
Waffle Pack
↓
Stock
(storage in Dry N_2)

AMC DICE PROCESSING FLOWCHART

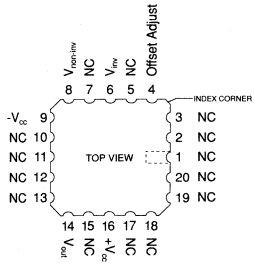
100% DC Probe to
+25°C Data Sheet Electricals
↓
Wafer Saw
and DI Water Rinse
↓
Wafer Inspection
↓
Element Evaluation
MIL-H-38534
1. Electrical Test per Device SCD
DC at – 55°C, + 25°C, + 125°C
2. Wire Bond Evaluation
↓
Die Sort
Into Waffle Packs
↓
100% Die Visual
Inspection to
M2010 MIL-STD-883
↓
QA Sample Visual
Inspection and
Document Review
↓
Seal in
Waffle Pack
↓
Stock
(storage in Dry N_2)

LCC Pin Outs

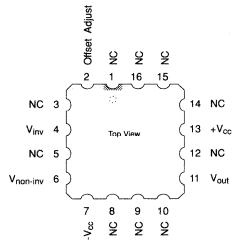
CLC114A8L-2A



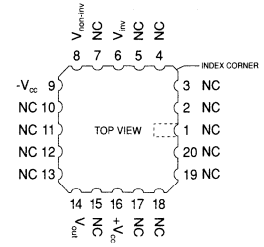
CLC400A8L-2A



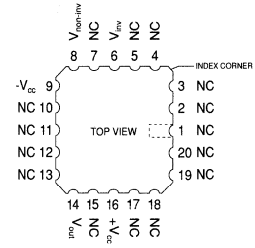
CLC400A8L-1



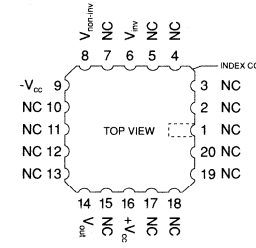
CLC402A8L-2



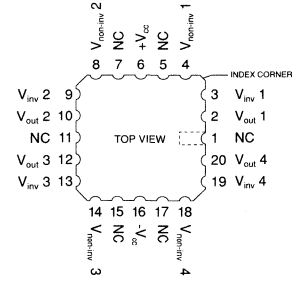
CLC406A8L-2A



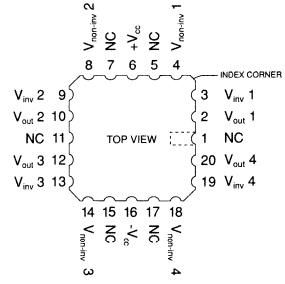
CLC409A8L-2A



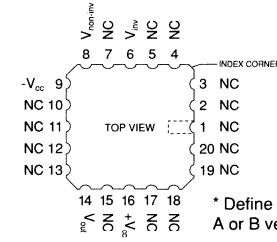
CLC414A8L-2A



CLC415A8L-2A

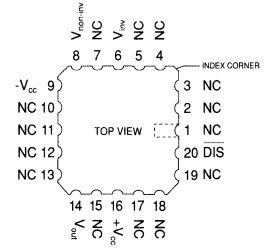


CLC420(*)8L-2A

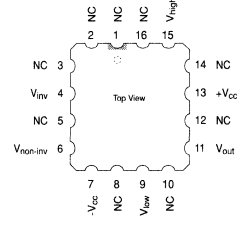


* Define either A or B version

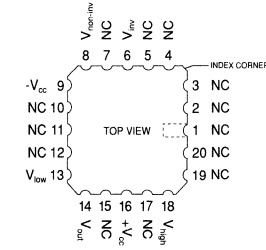
CLC430A8L-2



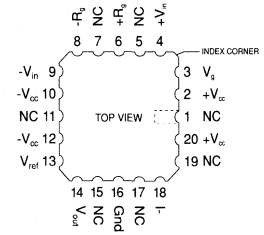
CLC501A8L-1A



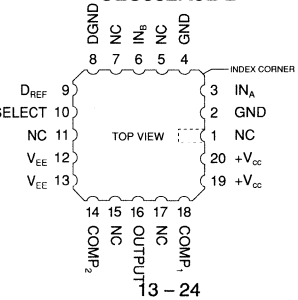
CLC502A8L-2



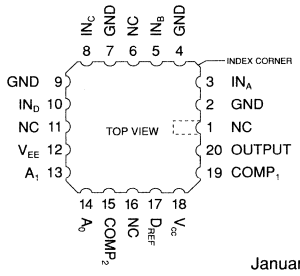
CLC520A8L-2



CLC532A8L-2



CLC533A8L-2



PRODUCT ACCESSORIES Section One

The following product accessories, for use in evaluation of Comlinear products, are available by contacting either your area representative, distributor, or Comlinear directly.

CLC103/203 Evaluation Boards Part Numbers 730005, 730006

Evaluation Boards

To aid in the evaluation of the CLC103 and CLC203 operational amplifiers, Comlinear has created evaluation PC boards: P/N 730005 is for inverting gain applications and P/N 730006 is for non-inverting gain applications. Both boards will accommodate either the CLC103 or the CLC203.

Note to CLC203 Users

The CLC203's superior input offset voltage and settling characteristics allow the composite amplifier (the LF356 and associated circuitry) to be omitted.

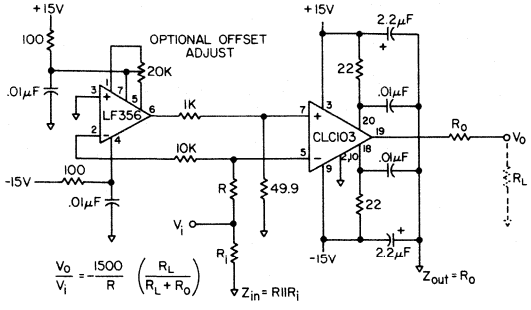


Figure 1: Inverting circuit with offset adjust circuitry

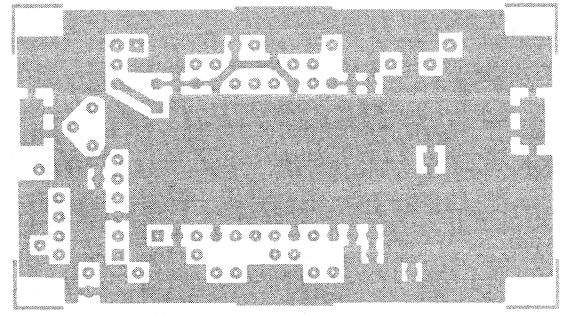


Figure 3: Circuit side (bottom) as viewed from component side, inverting

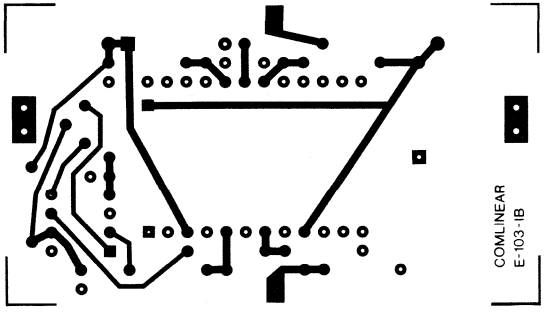


Figure 2: Component side (top), inverting

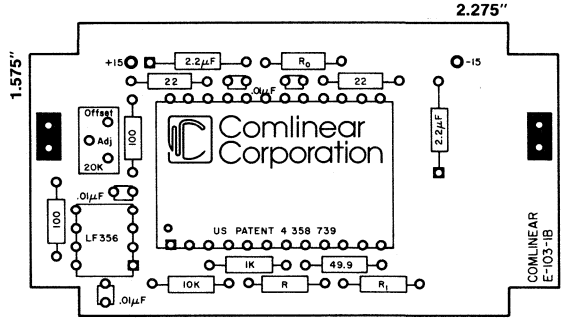


Figure 4: Component placement guide, inverting

14

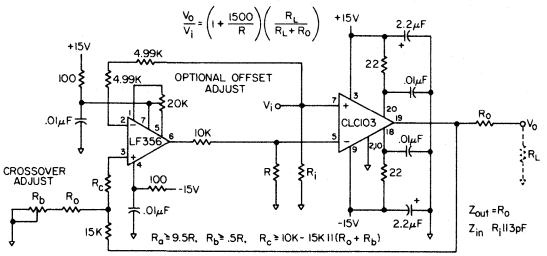


Figure 5: Non-inverting circuit with offset adjust circuitry

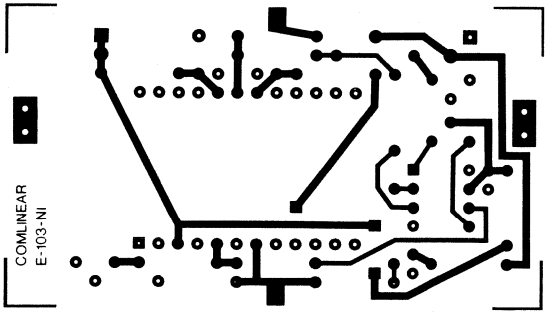


Figure 6: Component side (top), non-inverting

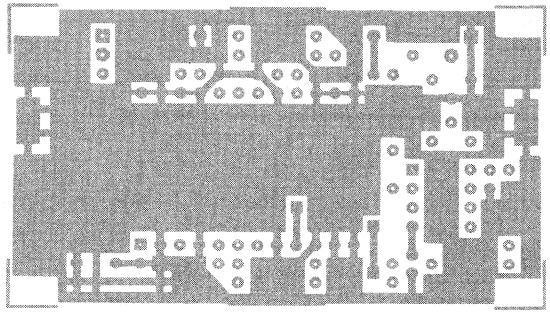


Figure 7: Circuit side (bottom) as viewed from component side, non-inverting

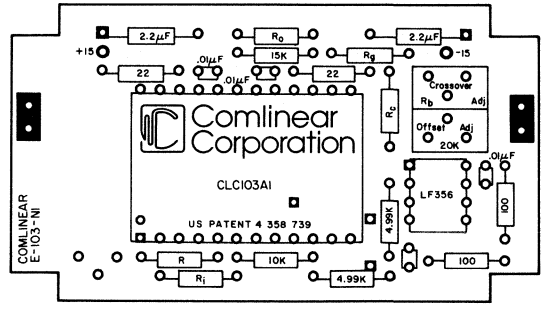


Figure 8: Component placement guide, non-inverting

Evaluation Board

To aid in the evaluation of the CLC104 amplifier, Comlinear has created an evaluation PC board: P/N 730007. The PC board schematic, layout, and component placement guide are shown below. Other application information is presented in the CLC104 data sheet.

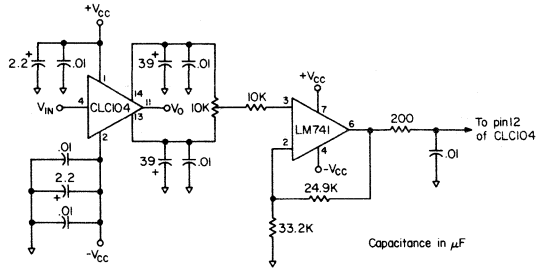


Figure 1: Circuit diagram showing offset voltage adjustment circuitry

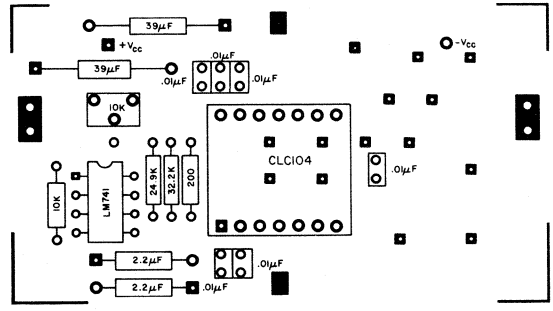


Figure 3: Component placement guide

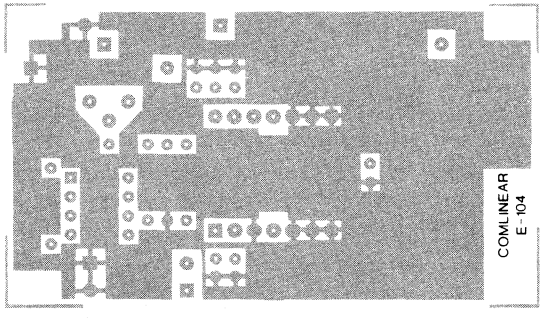


Figure 2: Component side (top)

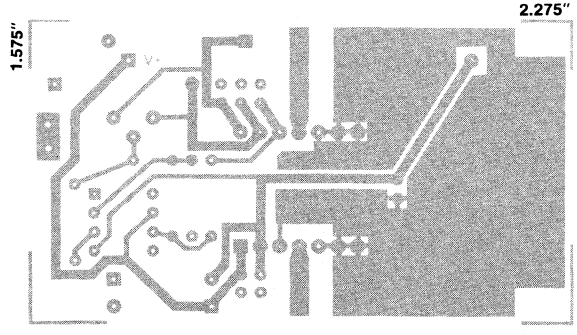


Figure 4: Circuit side (bottom) as viewed from component side

14

Printed Circuit Layout and Supply Bypassing

As with any high-frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the CLC110, which has a typical bandwidth of 730MHz.

To minimize capacitive feedthrough, the pins not connected internally (pins 2, 3, 6, and 7) should be connected to the ground plane. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the CLC110. On a 0.065 inch epoxy PCB material, a 50Ω transmission line (commonly called stripline) can be constructed by using a trace width of 0.1" over a complete ground plane.

Figure 1 shows recommended power supply bypassing. The ferrite beads are optional and are recommended only where additional isolation is needed from high-frequency (>400MHz) resonances of the power supply.

Parasitic or load capacitance directly on the output of the CLC110 will introduce additional phase shift in the device, which can lead to decreased phase margin and frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the CLC110 data sheet illustrate the required resistor value and the resulting performance vs. capacitance. Precision buffed resistors (PRP8351 series from Precision Resistive Products), which have low parasitic reactances, were used to develop the data sheet specifications. Precision carbon composition resistors or standard spirally-trimmed RN55D metal film resistors will work, though they will cause a degradation of AC performance due to their reactive nature at high frequencies.

Evaluation Board

An evaluation board, part number 730012, is available to assist in the evaluation of the CLC110. It may also be used as a guide in developing a printed circuit layout. Figure 1 shows the board's schematic; Figures 2 through 4 show the board layout.

Evaluation Board Parts List:

R_{in}	select for desired input impedance
R_{out}	select for desired output impedance
C_1, C_2	0.1μF ceramic radial lead
C_3, C_4	6.8μF (Sprague 150D series)
L_1, L_2	ferrite beads (optional) (Ferroxcube #VK 200 19/4B)

Hardware (optional)
Sockets Cambion flush-mount connector jacks
(#450-2598-01-06-00)
SMA Connectors (female)
Amphenol 901-144 (straight)
Amphenol 901-143 (angled)

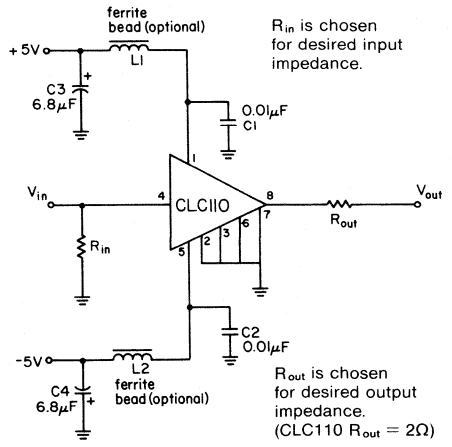


Figure 1: Recommended circuit and evaluation board schematic

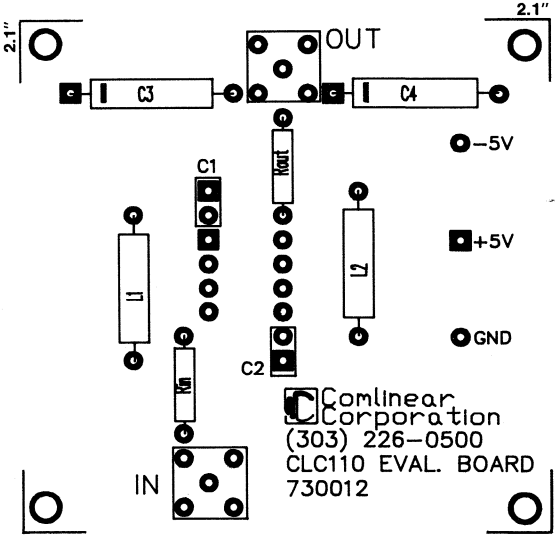


Figure 2: Component placement guide

14

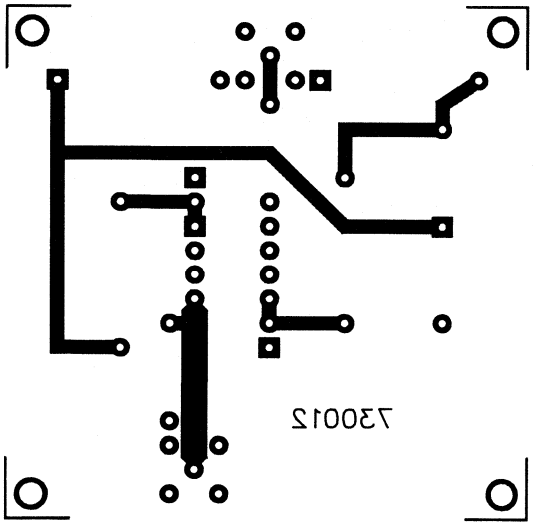


Figure 3: Solder side (bottom) as viewed from component side (top)

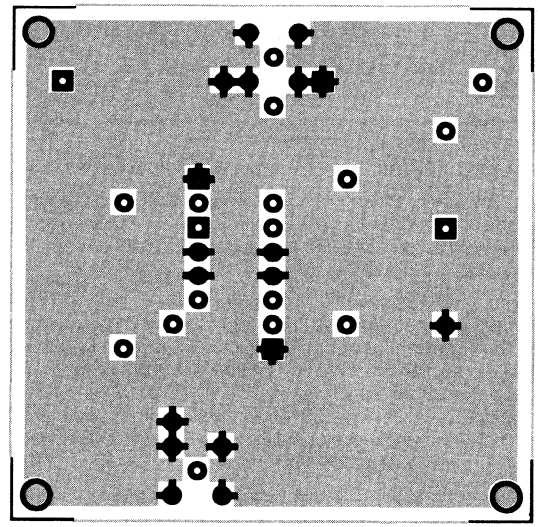


Figure 4: Component side (top) showing extensive ground plane

The 730023 is an evaluation board designed to aid in the evaluation and characterization of the CLC114 and CLC115 closed-loop quad buffers. The CLC114 is intended for use in applications requiring lower power operation while the CLC115 is intended for use in systems requiring wider bandwidth and higher output drive capability. Both of these quads offer four unity gain buffers in one 14-pin package. The individual data sheets provide more detailed information on applications and specifications.

The 730023 evaluation board allows for the construction of a number of different circuits utilizing both the CLC114 and the CLC115. Two of the four channels on the board are arranged for the evaluation of signal buffering in a 50Ω environment while two other channels integrate on-board , user-selected, RC active filters. Each type of filter, low pass or bandpass, can be implemented by selecting the appropriate RC component. The filters are designed to use all four of the buffers configured in series: an input buffer, one or two cascaded active filter stages and an output buffer.

The complete schematic of the 730023 evaluation board, showing all component locations, is shown in Figure 3. The parallel resistor/capacitor locations are intended for use with either a resistor or a capacitor with the choice of component depending upon the type of filter. Figure 4 shows the component placement for a cascaded bandpass filter and Figure 5 shows the component placement for the cascaded low pass filter. Each of the two low pass filter sections can be configured as either a second or a third order filter. Configuration of the third order filter requires the placement of additional components. Channel 1 requires R_1, C_1 and channel 4 requires R_6, C_6. It will be necessary to cut the 50Ω strip line from the input of channel 3 (pin 5) in order to evaluate the active filter circuit. Separate evaluation of the buffer circuits requires a 50Ω resistor to be placed at the input of channels 1 and 4 (R_4 and R_9) to insure stability of the unused buffers.

Low Pass Filter Design with the 730023 Evaluation Board

Figure 5 shows the schematic for a low pass filter. The two filter sections may be configured as either a second or a third order filter and therefore, configured in series, provide for a fourth or fifth order low pass filter.

Low Pass Filter Design Equations

It is a common practice in filter design to begin with the synthesis of a filter normalized in frequency and impedance. This method simplifies the derivation of design equations and allows for the convenient calculation of component values. Circuit resistors are normalized to 1Ω and resonant, or cut-off frequencies, are normalized to 1rad/sec [3]. Now, the design effort is reduced to the calculation of capacitor values in an RC active filter. For simplicity, the filter design equations below use the component designations of channel 1, shown in Figure 5.

Second-Order Filter

Using R_2,R_3=1Ω (R_1=0, C_1=0 for second order), the normalized transfer function is

$$H(s) = \frac{1}{C_3 C_5 s^2 + 2C_3 s + 1}$$

The roots of this transfer function are a complex pole-pair at $s=\alpha \pm j\beta$.

H(s) can then be expressed in terms of this pole-pair.

$$H(s) = \frac{1}{\frac{s^2}{\alpha^2+\beta^2} + \frac{2\alpha s}{\alpha^2+\beta^2} + 1}$$

equating coefficients in these two equations for the two capacitors yields

$$C_5 = \frac{1}{\alpha}\ ,\ C_3 = \frac{\alpha}{\alpha^2+\beta^2}$$

The pole locations (values for α and β) for all filter types (Butterworth, Bessel, Chebyshev etc.) can be found in the references listed at the end of this application note.

Third-Order Filter

Using R_1,R_2,R_3=1Ω, the normalized transfer function is

$$H(s) = \frac{1}{As^3 + Bs^2 + Cs + 1}$$

where

$A = C_1C_4C_5$; $B = 2C_4(C_2 + C_5)$; $C = C_1 + 3C_4$

Solving for the capacitor values in terms of the pole locations is cumbersome. As a practical matter, the capacitor values have been tabulated [2] for this filter topology. The design of an n^{th} order filter is done by looking up capacitor values for a filter normalized to a −3dB frequency of 1rad/sec.

Once the normalized capacitor values have been found, the actual component values are found by scaling for frequency and impedance. The normalized capacitor values are frequency scaled by dividing them by the desired cut-off frequency ω_c, $\omega_c = 2\pi f_c$. Impedance scaling is then performed by dividing the frequency scaled capacitor values by a resistor of value R. This resistor value is chosen such that impedance scaling produces reasonable capacitor values. All resistances have been assumed equal for a particular filter section. The resistors (normalized to 1Ω) are then impedance

scaled by multiplying by the impedance scaling factor R. The following equation summarizes these two steps for calculating actual capacitor values.

$$C = \frac{C_{normalized}}{2\pi f_c R}$$

Design Example. Fifth-Order Bessel Low Pass, $f_c = 1MHz$.

A fifth-order Bessel (maximally flat delay) low pass filter can be built from a cascade of a third and a second-order filter section. A fifth-order polynomial must first be factored into second and third order polynomials (whose product is the desired fifth-order Bessel polynomial). The cascade of a second and a third-order Bessel polynomial does not yield a fifth-order Bessel polynomial. For a fifth-order circuit, the following normalized capacitor values are found [2].

third-order section: $C_5 = 1.010F$; $C_4 = 0.3095F$; $C_1 = 0.8712F$

second-order section: $C_5 = 1.041F$; $C_4 = 0.3100F$

Scaling for frequency and impedance, the calculated component values are as follows:

third-order section:

$R = 2.37k\Omega$; $C_5 = 68pF$; $C_4 = 20.8pF$; $C_1 = 58.8pF$

second-order section:

$R = 1.82k\Omega$; $C_5 = 91pF$; $C_4 = 27.1pF$

Due to buffer input capacitance, C_1 and C_4 were slightly decreased in value. A circuit was built according to Figure 5 with these component values:

R_{in1}, R_{in2}, $R_{11} = 50\Omega$; R_1, R_2, $R_3 = 2.37k\Omega$; R_7, $R_8 = 1.82k\Omega$

C_{11}, $C_{14} = 6.8\mu F$; C_{12}, $C_{13} = 0.1\mu F$; $C_1 = 56pF$, $C_4 = 18pF$; $C_5 = 68pF$, $C_9 = 24pF$, $C_{10} = 91pF$; $R_6, C_6 = 0$

In the passband, the group delay (τ) for a fifth-order Bessel lowpass filter [1] is

$$\tau = \frac{2.4}{2\pi f_c sec} \quad \text{for } f_c = 1MHz,\ \tau = 382nsec.$$

Figure 1 shows the frequency response of the magnitude, phase and group delay. The group delay can be approximated from the phase from the equation

$$\tau = \frac{\Delta\varphi(degrees)}{360°(\Delta f)}$$

where Δ is the delay aperture, $\Delta\varphi$ is the phase change over the delay aperture. In this filter, the group delay was constant within 3% to 1.3MHz, using a delay aperture of 25kHz.

Figure 5. Fifth-Order Bessel Low Pass Response

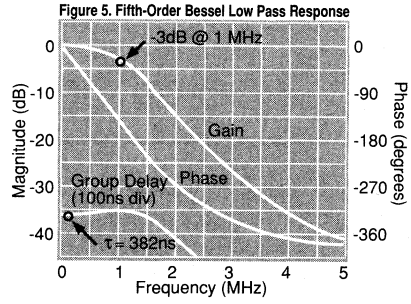


Figure 1

Second-Order Bandpass Filter Performance Equations

The circuit of Figure 4 is a cascade of two second-order bandpass filters to yield a fourth-order bandpass filter. This circuit is often simplified [4] by choosing R_2, R_4, $R_5 = R$ and C_2, $C_3 = C$. This approach is adequate when the gain of the amplifier, K, can be chosen by the designer. When K is fixed (as in the case of a unity-gain buffer) only the resistor and capacitor values are left to determine circuit performance. Furthermore, it can be shown [3] that the equal-R, equal, equal-C design has poor performance sensitivity to component variation. For example, making $C_2 > C_3$ will increase the Q of the circuit (other components remaining the same as the equal-C case) while simultaneously decreasing the Q-sensitivity to other circuit parameters.

Below are equations for ω_o, Q and midband gain for two extremes of circuit component constraints. The equal-R, equal-C equations offer the simplest circuit design with the most restricted performance. Conversely, allowing free choice of all component values allows the designer to optimize any design parameter. These parameters cannot, however, be chosen independent of one another. An example of trade-offs to be considered is the C_2/C_3 ratio. Increasing this ratio (while other component values remain the same) raises the circuit Q, but it also reduces the midband gain (increases the insertion loss) of the filter. Finding the best compromise is left as a challenging exercise for the motivated designer.

$$H(s) = \frac{\frac{K}{R_2C_2}s}{s^2 + s\left(\frac{1}{R_2C_2} + \frac{1}{R_4C_4} + \frac{1}{R_4C_2} + \frac{1-K}{R_5C_2}\right) + \frac{R_2+R_5}{R_2R_4R_5C_2C_3}}$$

$$\omega_o^2 = \frac{R_2+R_5}{R_2R_4R_5C_2C_3}; \quad Q = \frac{\sqrt{\frac{R_5C_2(R_2+R_5)}{R_2R_4C_3}}}{1 + \frac{R_5}{R_2} + \frac{R_5}{R_4}\left(1 + \frac{C_2}{C_3}\right) - K}$$

$$\text{midband gain } (\text{at } \omega_o) = \frac{\frac{K}{R_2C_2}}{\frac{1}{R_2C_2} + \frac{1}{R_4C_3} + \frac{1}{R_4C_2} + \frac{1-K}{R_5C_2}}$$

where K is the gain of the CLC114/CLC115.
For the equal-R, equal-C case:

$$\omega_o^2 = \frac{2}{RC},\ Q = \frac{\sqrt{2}}{4-K},\ \text{midband gain } (\text{at } \omega_o) = \frac{K}{4-K}$$

References

1) A.I. Zverev, "Handbook of Filter Synthesis", John Wiley and Sons, New York, 1967.
2) A.B. Williams, and F.J. Taylor, "Electronic Filter Design Handbook, Second Edition", McGraw-Hill, New York, 1981.
3) R. Schaumann, M.S. Ghausi, and K.R. Laker, "Design of Analog Filters", Prentice Hall, Englewood Cliffs, 1990.
4) A. Budak, "Passive and Active Network Analysis and Synthesis", Houghton Mifflin Company, Boston, 1974.

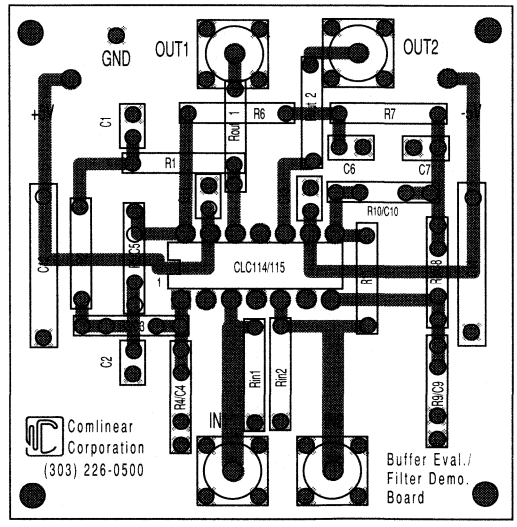


Figure 2
Board Layout and Component Placement

Figure 3
Board Schematic

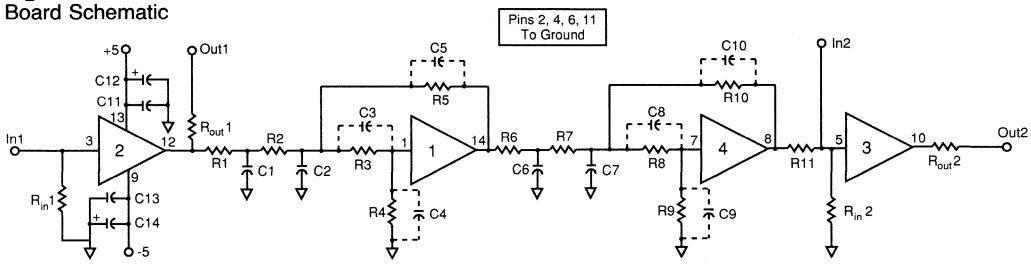


Figure 4
Bandpass Filter Schematic

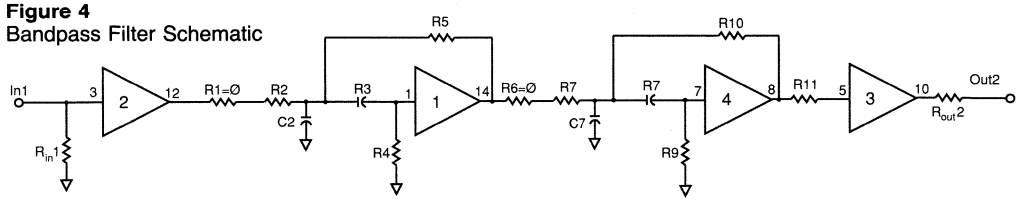
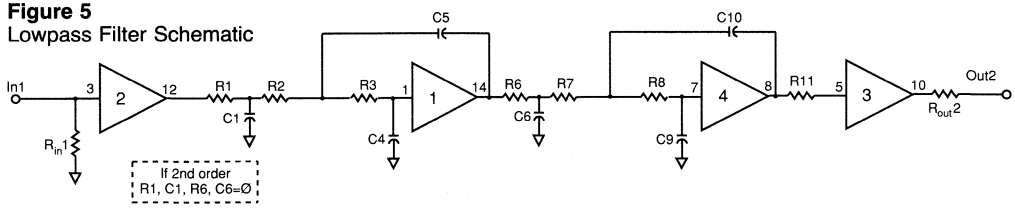


Figure 5
Lowpass Filter Schematic



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CLC2XX Series Evaluation Boards
Part Numbers 730008, 730009

Evaluation Board for CLC200, 201, 205, 206, 207, 220, 221, 231, and 232

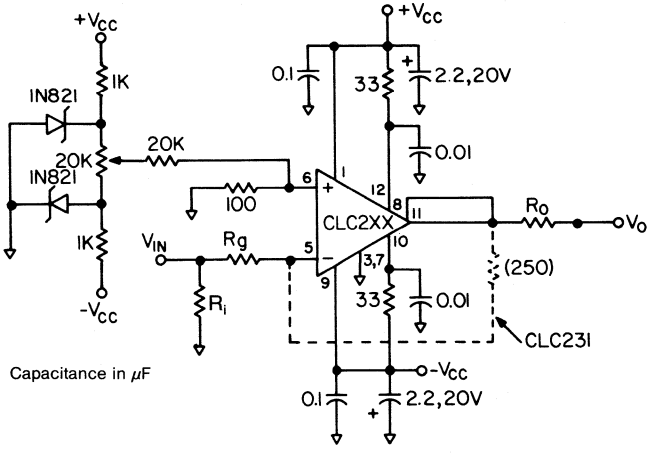
Description

Comlinear part numbers 730008 (inverting) and 730009 (non-inverting) are evaluation boards designed to help design engineers evaluate and use the CLC2XX Series op amps. In addition, the boards can serve as a guide for engineers who are developing printed circuit layouts for op amps.

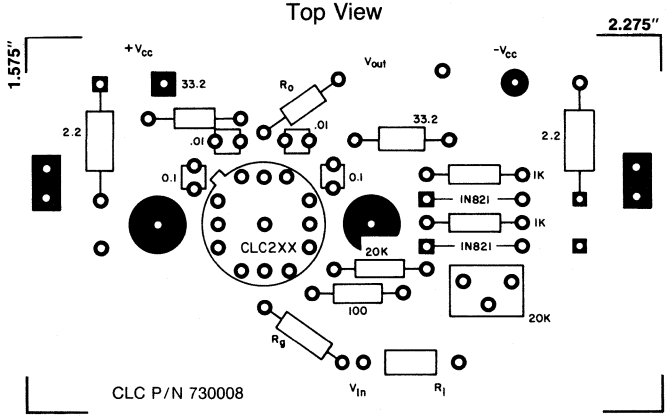
Part number 730008 is designed for inverting gains, and part number 730009 is designed for non-inverting gains. Each is discussed individually.

Part Number 730008 – Inverting Gains

Schematic



Top View

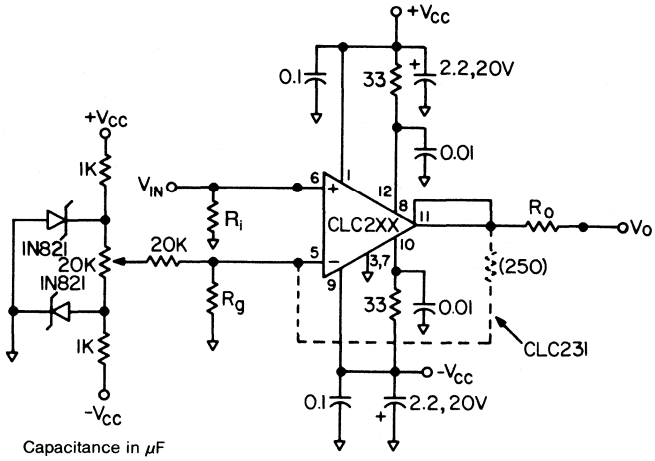


Note to CLC231/232 Users: Cut traces between pins 11 and 8 on bottom at board and add a 250 Ω resistor between pins 5 and 11 (on bottom).

Comlinear Corporation • 4800 Wheaton Drive, Fort Collins, CO 80525 • (303) 226-0500 • FAX (303) 226-0564

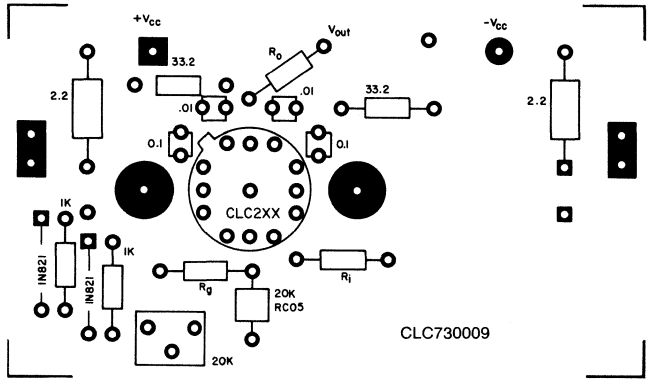
Part Number 730009 - Non-Inverting Gains

Schematic



Capacitance in μF

Top View



Note to CLC231/232 Users: Cut traces between pins 11 and 8 on bottom at board and add a 250 Ω resistor between pins 5 and 11 (on bottom).

Parts List

RESISTORS:

Designator	Value or Equation	
	Non-Inverting	Inverting
R_o	Z (out)	Z (out)
R_g	$R_f/(A_v - 1)$	$R_f/\|A_v\|$
R_i	Z (in)	Z (in) $R_g/[R_g - Z\text{ (in)}]$

All resistors metal film RN55D or equivalent except:
20k trimpot (offset adjust)
20k RC05 (or equivalent)

CAPACITORS:

Designator	Value
.01	.01 uf, 20V ceramic
.1	0.1 uf, 20V ceramic
2.2	2.2 uf, 20V tantalum

HARDWARE:

Sockets	Cambion flush-mount connector jacks (#450-2598)

Evaluation Boards

To aid in the evaluation of CLC300 operational amplifiers, Comlinear has created an evaluation PC board, P/N 730010. This board is designed for use in either inverting or non-inverting configurations, as Figures 1 through 4 illustrate.

Operational Hints

A few suggestions will help to maximize the usefulness of this board:

Optimum performance is obtained without the use of sockets. However, if sockets are necessary, flush mount connector jacks from Cambion (P/N 450-2598-01-03-00) are recommended. To minimize capacitance between pins, jacks should be used only where contact to the CLC300 must be made (pins 6, 8, 11, 12, 13, 16, 24).

In an effort to simplify this layout, $-V_{cc}$ has been routed through pin 10 of the CLC300. This routing, however, causes approximately 0.2dB of frequency-response peaking. This peaking can be eliminated by floating pin 10 either by cutting that pin away from the package or by rerouting the $-V_{cc}$ trace.

The board is shaped to fit the Modpak case 7042.

General Layout Considerations

To assure optimum performance, the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. Avoid wire-wrap type PC boards and methods.

During PC board layout, keep all traces short and direct. The resistive bodies of R_f and R_g should be as close as possible to pin 8 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 6, 7 and 8. In other areas, use as much ground plane as possible on one side of the PC board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF should be close to pins 13 and 16. Larger tantalum capacitors should also be placed within one inch of these pins.

To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches. Since the PC board forms such an important part of the circuit, much time can be saved if prototype boards of any high-frequency sections are built and tested early in the design phase.

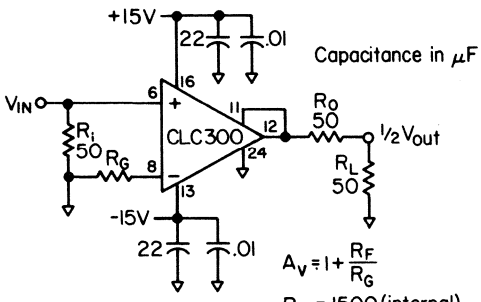


Figure 1: Non-inverting gain test fixture

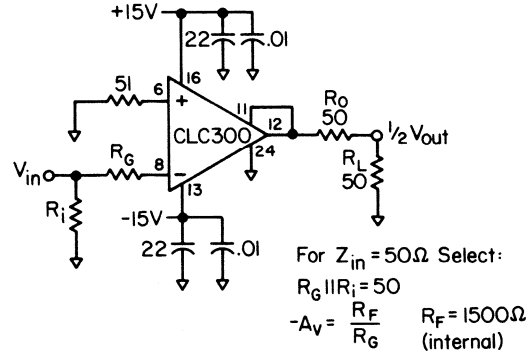


Figure 2: Inverting gain test fixture

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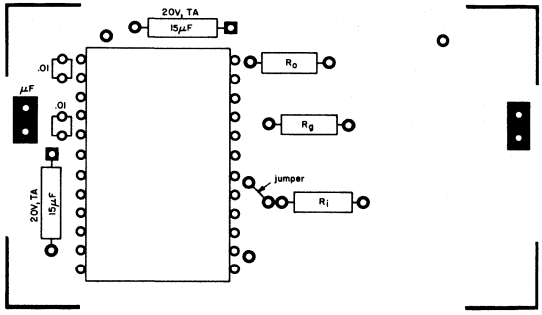


Figure 3: Component placement guides, non-inverting

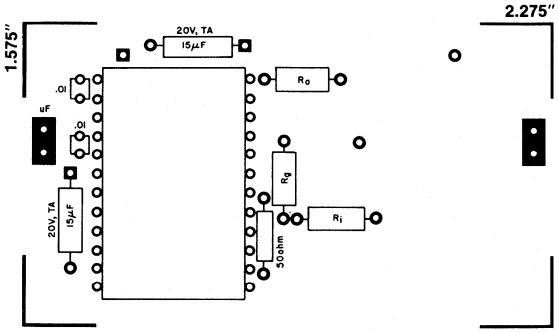


Figure 4: Component placement guides, inverting

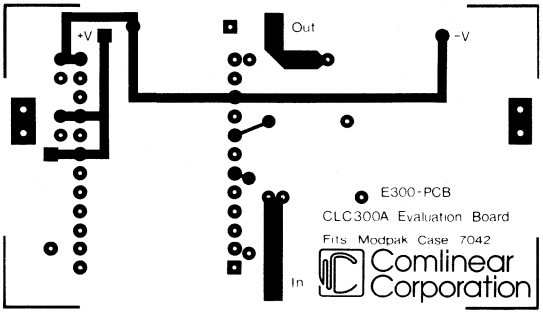


Figure 5: Component (top) side

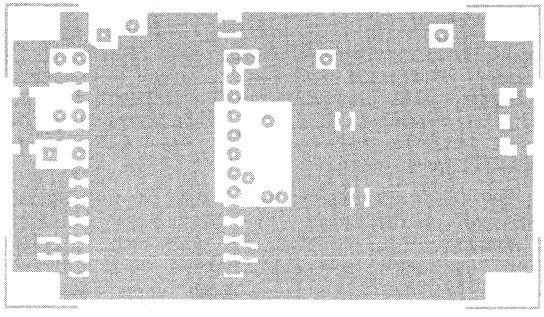


Figure 6: Solder (bottom) side as viewed from component (top) side

8-Pin Monolithic Amplifier Evaluation Boards (Part Numbers 730013, 730027)

DESCRIPTION

The 730013 (Rev.C) is an evaluation board configured to accommodate most of Comlinear's 8-pin monolithic amplifier products in a standard through-hole DIP. A companion board, the 730027 (Rev. C) is also available for easy evaluation of the 8-pin plastic SOIC (surface mount) packages (AJE suffix). These boards are set up to yield a non-inverting gain determined by the R_f and R_g resistors. Additionally, typical op amp topologies, such as inverting and differential amplification, can be easily implemented by slight modifications to the board. With the introduction of the Rev. C board (July, 1991) the following Comlinear amplifier products may be evaluated using this board. (Unless specifically stated otherwise, all of these are current feedback amplifiers using +/-5V supplies.)

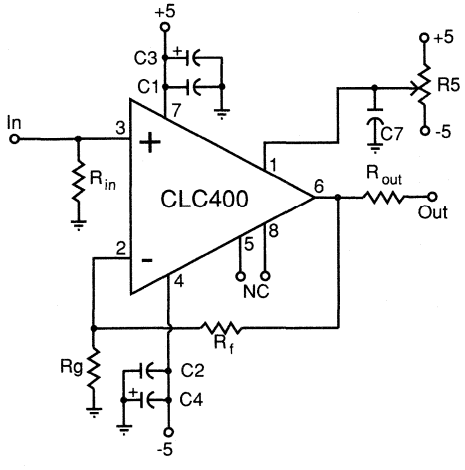
CLC400 → A wideband amplifier optimized for low gain operation
CLC401 → A wideband amplifier optimized for high gain operation
CLC402 → A high accuracy (.0025%) amplifier for low gain operation
CLC404 → A wideband, high slew rate amplifier for intermediate gains
CLC406 → An intermediate gain amplifier with low quiescent power
CLC409 → A low gain, wideband amplifier with low harmonic distortion
CLC410 → A low gain amplifier with a shutdown capability
CLC411 → A wideband, low gain amplifier using +/-15V power supplies
CLC420 → A unity gain stable, wideband, voltage feedback amplifier
CLC422 → A very high gain-bandwidth product voltage feedback amplifier
CLC425 → A very low-noise, wideband, voltage feedback amplifier.
CLC430 → An intermediate performance amplifier using +/- 15V supplies
CLC501 → A high gain amplifier with output clamping capability
CLC502 → A low gain amplifier with output clamping and .0025% settling
CLC505 → An intermediate gain amplifier with adjustable supply current

Please refer to the detailed data sheets on each of these parts for a full description of their performance capabilities.

The high frequency signal path required by each of these parts is identical. Hence, the AC portion of the layout can be used as a guide to good high frequency layout for any of these amplifiers. See application note OA-15 for additional layout suggestions. For good high frequency performance, close power supply de-coupling to a low inductance ground plane is required. Capacitors C1 through C4 provide this for any of the parts built up on this board.

Since all of the above listed parts are op amps, their non-inverting input impedance is typically quite high, while the output impedance is very low. Hence, the board input/output impedance is set for all of these parts using the R_{in} and R_{out} resistors.

The following diagrams show a typical circuit implementation for each of the devices accommodated by this board. The circuit and the component values shown for each part correspond to the non-inverting test configuration used to generate the specifications shown on each part's data sheet. Please refer to the specific data sheets for a discussion of any external components shown on the following schematics but unique to the use of that part.

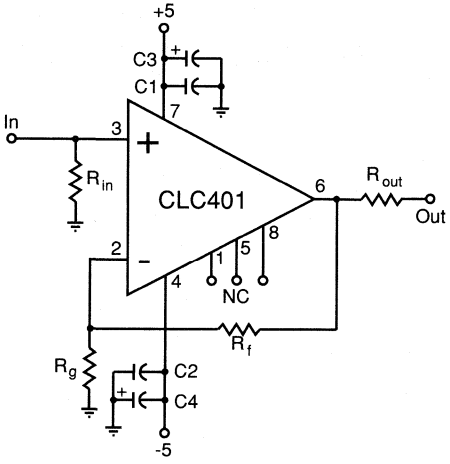


The CLC400 is a wideband current feedback op amp optimized for low gains.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$
$R_f = R_g = 250\Omega$ ($A_V = +2$)
C1 = C2 = .1µF ceramic
C3 = C4 = 6.8µF tantalum
R5 = 20kΩ pot (optional input offset voltage null)
C7 = .01µF ceramic (should be used for best fine scale settling even if R5 not used)

Components not used:
C5, C6, C8
R1, R2, R3, R4, R6, R7, R8



CLC401 is a wideband current feedback op amp optimized for high gains.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$

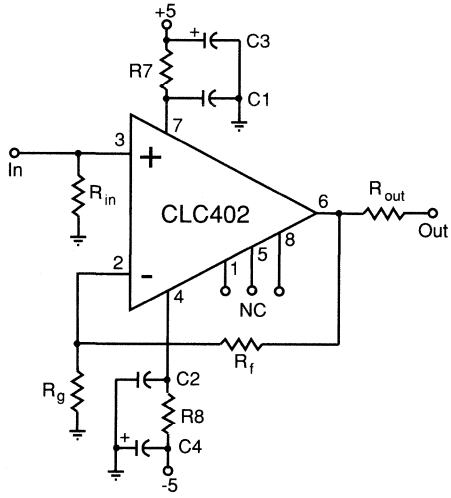
$R_f = 1.5k\Omega$

$R_g = 78.7\Omega$ ($A_V = +20$)

C1 = C2 = .1µF ceramic

C3 = C4 = 6.8µF tantalum

Components not used:
C5, C6, C7, C8
R1 → R8



The CLC402 is a wideband current feedback op amp optimized for low gains, offering extremely fast settling to .0025% accuracy.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$

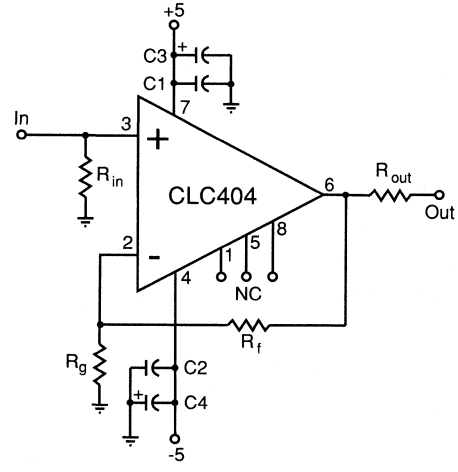
$R_f = R_g = 250\Omega$ ($A_V = +2$)

C1 = C2 = .1µF ceramic

C3 = C4 = 6.8µF tantalum

R7 = R8 = 10Ω (optional series supply resistors - component side supply traces shorting R7 & R8 should be cut to use these resistors.)

Components not used:
C5, C6, C7, C8
R1 → R6



The CLC404 is a wideband op amp optimized for intermediate gain with extremely broad full power bandwidth.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$

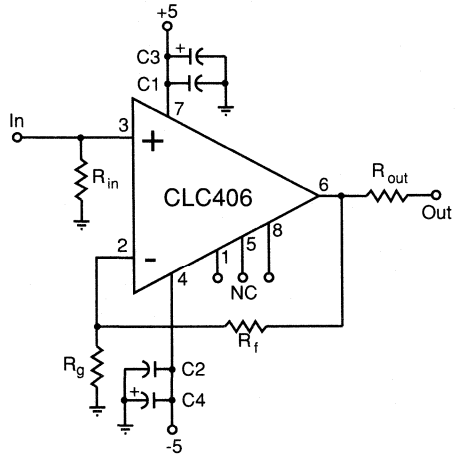
$R_f = 500\Omega$

$R_g = 100\Omega$ ($A_V = +6$)

C1 = C2 = .1µF ceramic

C3 = C4 = 6.8µF tantalum

Components not used:
C5, C6, C7, C8
R1 → R8



The CLC406 is an intermediate performance, low quiescent power op amp optimized for midrange gains (+/-1 to +/-10)

Recommended Values:

$R_{in} = R_{out} = 50\Omega$

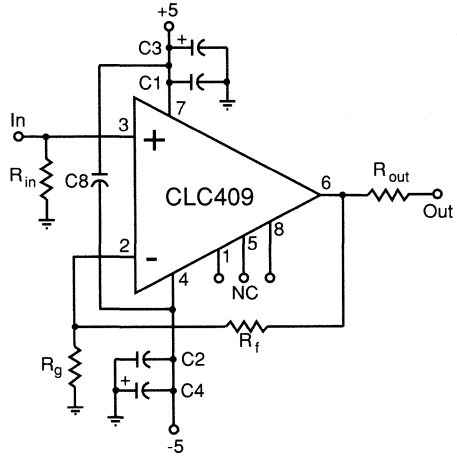
$R_f = 500\Omega$

$R_g = 100\Omega$ ($A_V = +6$)

C1 = C2 = .1µF ceramic

C3 = C4 = 6.8µF tantalum

Components not used:
C5, C6, C7, C8
R1 → R8



The CLC409 is a very wideband op amp optimized for low gains and offering exceptionally low harmonic distortions.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$

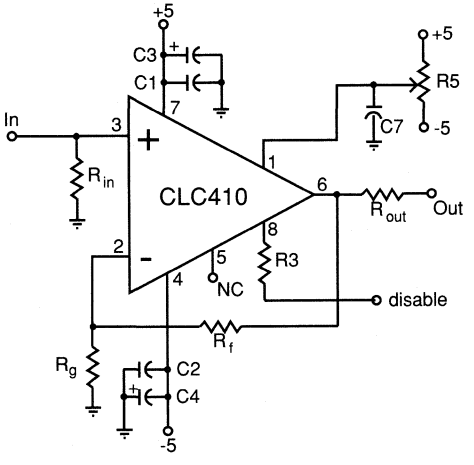
$R_f = R_g = 250\Omega$ ($A_V = +2$)

C1 = C2 = .1µF ceramic

C3 = C4 = 6.8µF tantalum

C8 = .01uF (optional supply to supply de-coupling for reduced distortion)

Components not used:
C5, C6, C7
R1 → R6



CLC410 is a wideband op amp optimized for low gains (very similar to the CLC400) with an output disable capability.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$

$R_f = R_g = 250\Omega$ ($A_V = +2$)

C1 = C2 = .1µF ceramic

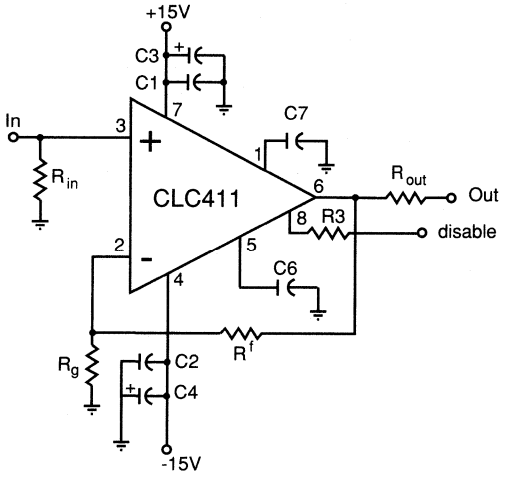
C3 = C4 = 6.8µF tantalum

R5 = 20kΩ pot (optional input offset voltage null)

C7 = .01µF ceramic (should be used for best fine scale setting even if R5 not used)

R3 = 0-1kΩ (open collector disable control.
Note: trace connecting R3 to $+V_{cc}$ must be cut; R3 connects to disable logic.)

Components not used:
C5, C6, C8
R1, R2, R4, R6, R7, R8



The CLC411 is a wideband op amp optimized for low gains and using +/-15V power supplies.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$

$R_f = R_g = 500\Omega$ ($A_V = +2$)

C1 = C2 = .1µF ceramic

C3 = C4 = 6.8µF tantalum

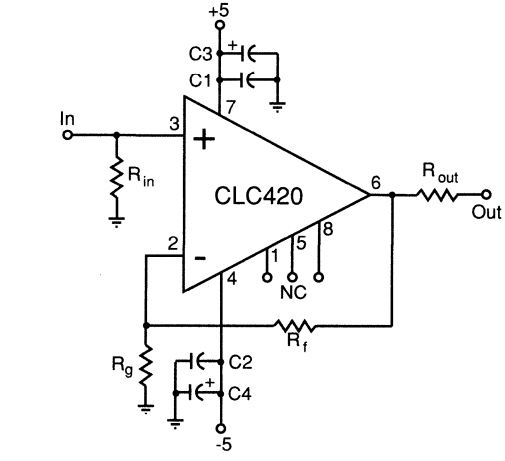
C6 =C7= .01µF ceramic

R3 = 0-1kΩ (open collector disable control. Note: trace connecting R3 to $+V_{cc}$ must be cut; R3 connects to disable logic.)

Components not used:

C5, C8

R1, R2, R4, R5, R6, R7, R8



The CLC420 is a wideband, unity gain stable, voltage feedback op amp with very low quiescent power dissipation.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$

$R_f = R_g = 500\Omega$ ($A_V = +2$)

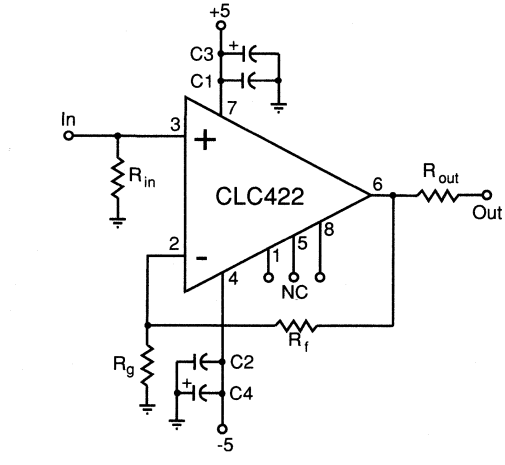
C1 = C2 = .1µF ceramic

C3 = C4 = 6.8µF tantalum

Components not used:

C5, C6, C7, C8

R1 → R8



The CLC422 is a very high gain-bandwidth (8 GHz) voltage feedback op amp optimized for high gains.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$

$R_f = 1.5k\Omega$

$R_g = 38.3\Omega$ ($A_V = +40$)

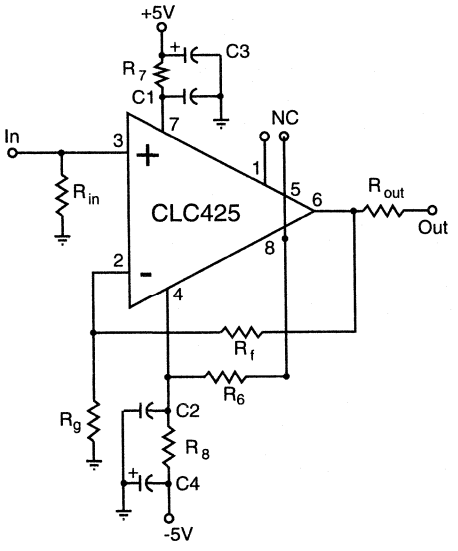
C1 = C2 =.1µF ceramic

C3 = C4 = 6.8µF tantalum

Components not used:

C5, C6, C7, C8

R1 → R8



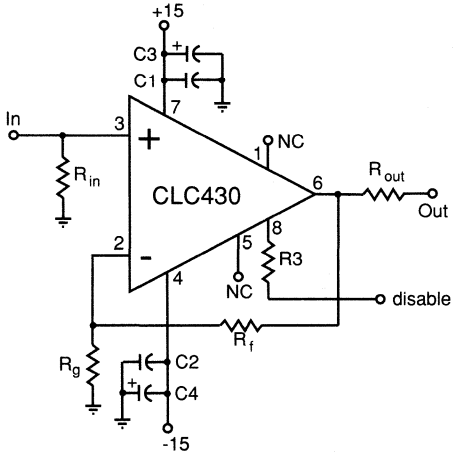
The CLC425 is a very low noise, wideband, voltage feedback op amp with an adjustable supply current feature.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$
$R_f = 500\Omega$
$R_g = 26\Omega$ ($A_V = +20$)
C1 = C2 = .1µF
C3 = C4 = 6.8µF tantalum
R6 = (sets supply current-see data sheet)
R7 = R8 = 10Ω (optional series supply resistors-see CLC425 discussion)

Components not used:

R1, R2, R3, R4, R5
C5, C6, C7, C8



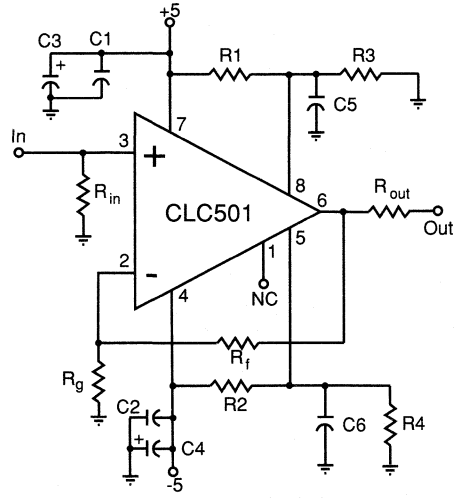
The CLC430 is an intermediate performance op amp using +/-15V supplies, optimized for low gains, and offering a disable feature.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$
$R_f = R_g = 750\Omega$ ($A_V = +2$)
C1 = C2 = .1µF ceramic
C3 = C4 = 6.8µF tantalum
R3 = 0-1kΩ (open collector disable control. Note: trace connecting R3 to +Vcc must be cut; R3 connects to disable logic.)

Components not used:

C5, C6, C7, C8
R1, R2, R4, R5, R6, R7, R8



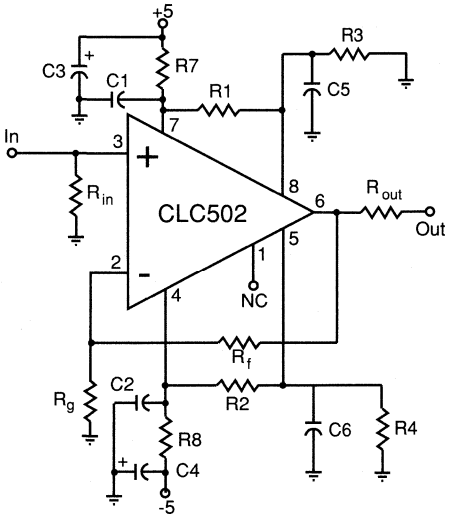
The CLC501 is a wideband op amp optimized for high gains and offering an extremely fast output voltage clamping capability.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$
$R_f = 1.5k\Omega$
$R_g = 48.7\Omega$ ($A_V = +32$)
C1 = C2 = .1µF ceramic
C3 = C4 = 6.8µF tantalum
R1 = R2 = 825Ω
R3 = R4 = 1.27kΩ (clamps at +/-3V)
C5 = C6 = .01µF ceramic (optional clamp de-coupling)

Components not used:

C7, C8
R5 → R8



The CLC502 is a wideband op amp optimized for low gains with exceptional settling to .0025% accuracy and a high speed output clamping capability.

Recommended Values:

$R_{in} = R_{out} = 50\Omega$

$R_f = R_g = 250\Omega$ ($A_V = +2$)

C1 = C2 = .1µF ceramic

C3 = C4 = 6.8µF tantalum

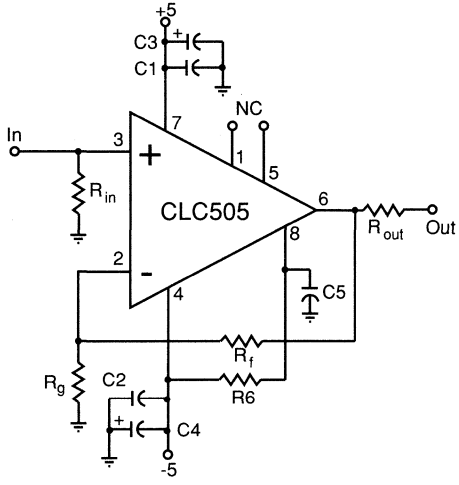
R1 = R2 = 825Ω

R3 = R4 = 1.27kΩ (clamps at +/-3V)

C5 = C6 = .01µF ceramic (optional clamp de-coupling)

R7 = R8 = 10Ω (optional series supply resistors - see CLC402 discussion)

Components not used:
C7, C8
R5, R6



The CLC505 is a wideband op amp optimized for intermediate gains and offering an adjustable supply current feature.

Recommended Values:

$R_{in} = 50\Omega$

R_{out} = (see data sheet)

$R_f = 1k\Omega$

$R_g = 200\Omega$ ($A_V = +6$)

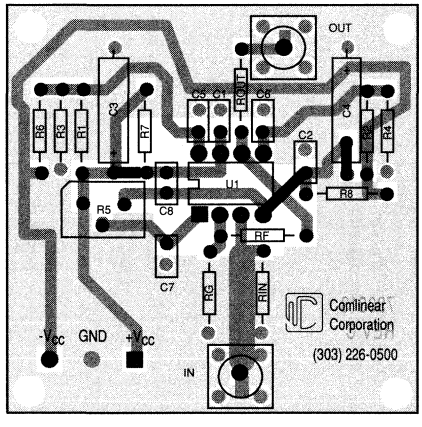
C1 = C2 = .1µF ceramic

C3 = C4 = 6.8µF tantalum

C5 = 100pF ceramic

R6 = (sets supply current - see data sheet)

Components not used:
C6, C7, C8
R1, R2, R3, R4, R5, R7, R8



Input and Output connectors are SMA board mount type - such as
Amphenol 901-144 (straight)
Amphenol 901-143 (angled)

The amplifier may be socketed using Cambion flush mount connector jacks (P/N 450-2598).

Resistor types - For best AC performance, low reactance precision buffed resistors from Precision Resistive Products (PRP8351 series) should be used. Precision carbon composition resistors will also yield excellent results while standard spirally trimmed RN55D precision metal film resistors will also work with a slight decrease in AC performance.

CLC414/415 Evaluation Board
Part Number 730024

The 730024 is an evaluation board designed to facilitate the characterization of the CLC414 and CLC415 quad current-feedback amplifiers. The CLC414 is designed for low power applications, while the CLC415 provides wider bandwidth and higher output current drive. Both the CLC414 and CLC415 offer four high-speed amplifiers in one 14-pin package. Please refer to the individual data sheets for more detailed information on the specifications and application of these devices.

The 730024 evaluation board configures the CLC414 and CLC415 as non-inverting amplifiers in a 50Ω environment. Inverting gain and differential amplifier circuits can be built with slight modifications to the board. It also serves as a layout guide for engineers developing their own printed circuit boards. Particular attention should be paid to the use of a ground plane and power supply bypassing. Figure 1 shows the layout of the board. Figure 2 is the complete board schematic.

Recommended Component Values

RIN1, RIN2, RIN3, RIN4 = 50Ω

ROUT1, ROUT2, ROUT3, ROUT4 = 50Ω

RF1, RF2, RF3, RF4 = 500Ω

RG1, RG2, RG3, RG4 = 100Ω

C1, C2 = 0.1μF ceramic

C3, C4 = 6.8μF tantalum

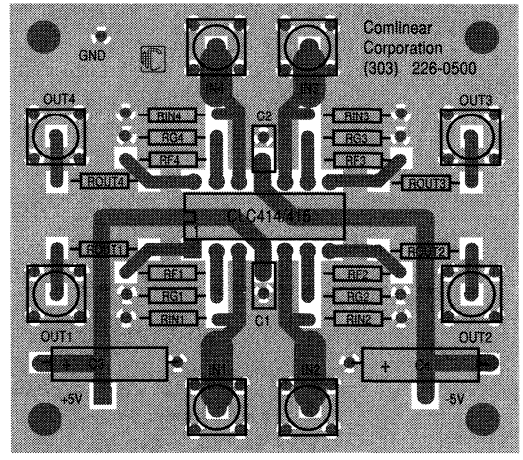


Figure 1: Board Layout and Component Placement

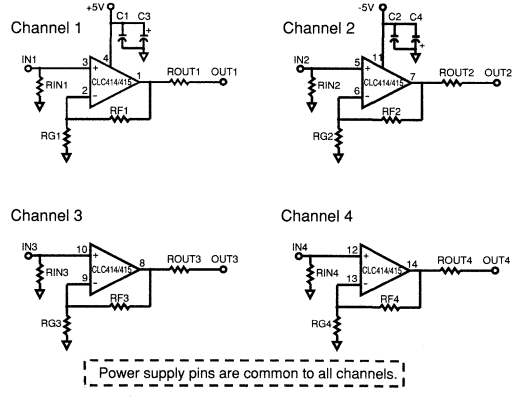


Figure 2: Board Schematic

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The #730029, Rev. B (through-hole) evaluation board provides an easy means of testing the operation and performance of both the CLC520 and the CLC522 in their 14-pin DIP packages. **Note, this board obsoletes an earlier CLC520 evaluation board - part #730021.** A similar board, #730033, Rev. B, (SOIC) accommodates the CLC520 and CLC522 surface mount versions. Please refer to the CLC520 and the CLC522 data sheets for complete performance information.

I. Basic Operation

Figure1 shows the complete evaluation circuit implemented on this board. The primary connections are shown with solid lines, while several optional circuit connections are shown with dashed lines.

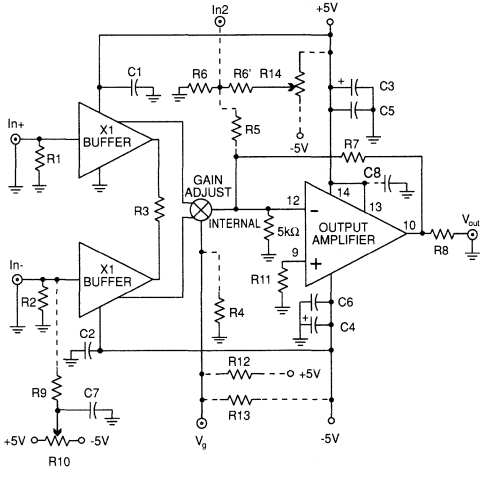

Figure 1: External components & amplifier internal block diagram

The CLC520 and the CLC522 have the same pin definitions with the only exception of an additional $+V_{CC}$ connection on pin 13 of the CLC522, whereas pin 13 is a no-connect on the CLC520. The evaluation board hard-wires pin 13 and pin 14 together, applying $+V_{CC}$ to both pins allowing the board to accommodate both devices. The key operational differences between the CLC520 and the CLC522 are found with the gain-adjust input (V_g: pin 2). The gain-adjust input voltage range of the CLC520 is 0-2V while that for the CLC522 is ±1.0V. Also the gain-adjust input resistance (pin 2 to ground) is typically 750Ω for the CLC520 and typically 100kΩ for the CLC522. One wiring difference should be noted, the ground connection from pin 9 (R11 on the evaluation board) of the output amplifier's non-inverting input should be a very low inductance short to ground for the CLC520 and 20Ω for the CLC522.

II. Basic CLC520 Connection

Figure 2 represents the simplest board configuration for the CLC520. The specific resistor values depicted here configure the CLC520 with a maximum gain of +10V/V; this is the condition used to specify the part in its data sheet.

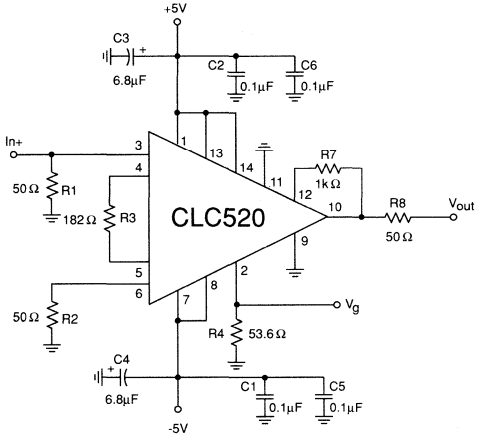

Figure 2: Basic CLC520 connection

The circuit of Figure 2 implements a non-inverting variable-gain amplifier with a 50Ω input impedance (R1), a 50Ω output impedance (R8), and a maximum gain of +10V/V (1.85•(R7/R3)). Recognizing the combination of the 50Ω series output resistor and the 50Ω load results in a voltage divider, the gain to this matched load is one half of the maximum device gain setting, i.e. +5 (14dB). The gain-adjust input has a 0-2V range with V_g > 2.0V yielding the maximum gain while V_g = 0V yields the maximum signal attenuation. Note, the CLC520's parallel combination of R4 (53.6Ω) and its internal 750Ω resistor to ground on pin 2 results in a 50Ω input impedance for V_g. The inverting input (In-) is ground-referenced through 50Ω while the output amplifier's non-inverting input is ground-referenced at pin 9. The evaluation board provides a component location at pin 9 (R11) used as a ground connection for the CLC520. This ground connection should be very short from the hole for R11 directly to the top-side ground plane, not a long wire in place of R11. In an application board layout, the CLC520's pin 9 should be taken directly into a very low-inductance ground plane with as little lead length as possible. This will

prevent the possibility of a high-frequency resonance (>400 MHz) in the output amplifier's input stage from causing any stability or frequency response problems. Earlier discussions of the CLC520 implied that pin 9 could be used to introduce a DC offset into the output amplifier. Due to its limited input voltage range and the need for a broadband low source impedance on pin 9, this method of introducing a DC offset is not recommended. As will be discussed later, an additional signal or DC offset can be more effectively introduced through the inverting input (pin 12).

III. Basic CLC522 Connection

Figure 3 shows the simplest configuration for evaluating the CLC522. The specific resistor values depicted here configure the CLC522 with a maximum gain of +10V/V; this is the condition used to specify the part in its data shee

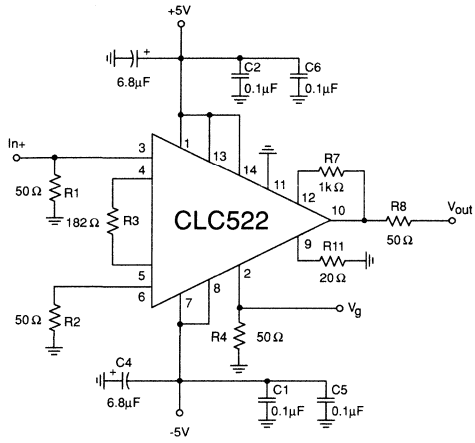

Figure 3: Basic CLC522 connection

This circuit is nearly identical to that of the CLC520. The only two circuit changes are seen at the gain-adjust input (pin 3), terminated here in 50Ω as opposed to the CLC520's 53.6Ω (the difference lies in the fact that the CLC522 has a much greater input impedance through pin 2 than the CLC520) and the ground-reference of the output amplifier (pin 9) is taken to ground through a 20Ω resistor (R11). The input gain-adjust voltage range of the CLC522 is ±1V. -1V for minimum gain (maximum attenuation) to +1V for maximum gain set by 1.85·(R7/R3). Again, the ground connection on pin 9 is very critical to the high-frequency stability of the amplifier. In this case the 20Ω resistor acts to stabilize a high frequency (>400 MHz) resonance in the output stage. An optional power-supply decoupling capacitor (C8) is shown with the CLC522 on pin 13 of Figure 1. A 0.01µF capacitor located at C8 can be used to slightly improve the device's fine scale pulse settling time, however, in most cases this capacitor is not required for evaluation.

IV. Gain Control Input Resistor Options

Two additional resistor locations (R12 & R13) are included on the gain-adjust line. The resistor locations may be used to introduce a DC bias on pin 2. Figure 4 provides an example of how R12 and R13 can be used to fix the CLC520 and the CLC522 at their maximum gains by applying a resistive DC-bias voltage on pin 2 in the absence of an applied V_g input. Note, the CLC520 presents an approximate 750Ω resistance on pin 2 while the CLC522 is typically 100kΩ.

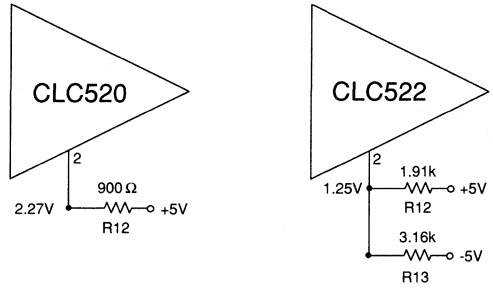

Figure 4: Setting up for the fixed maximum gain

One CLC520 application (shown above) is a fixed maximum-gain connection combined with an open-collector pull-down (not shown) to disable the gain channel. If an open-collector gate is used to pull pin 2 low, the signal channel would see its maximum attenuation. While this arrangement will greatly improve the downstream signal isolation, it will not cause the CLC520's output to rise to a high impedance nor reduce its quiescent current.

A related CLC522 application (shown above) reverses the positions of the two resistors, resulting in a negative DC bias on pin 2. This arrangement will place the part into a default maximum-attenuation mode and therefore, in the absence of an applied V_g voltage, isolate the part from signal transmission. Since the resistors used here are relatively large, any DC source for V_g can be used to drive pin 2 to the desired gain-control voltage.

V. Summing Signals and Offsets into the Output Stage

The output amplifier's inverting node (pin 12) is available to introduce any additional signals or offsets into the output. Since pin 12 is a virtual ground, additional signals may be summed into this node without a substantial impact of the signal current flowing from the adjustable-gain path. Briefly, adding an additional impedance on the inverting input of the output amplifier will result in a slight bandwidth reduction of the output amplifier and an increase in the noise gain for the output amplifier's non-inverting input noise voltage. Refer to application note OA-13 for a more thorough discussion of current feedback amplifiers in inverting summing applications. Figure 5 shows an example of using the optional components on the board to sum in a high-speed signal with a gain of -2 to the output pin (or -1 to the matched 50Ω load).

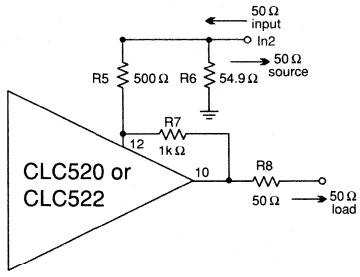

Figure 5: Summing a high-speed signal into the output

Note, R6 can be used in either of two locations on this board. In Figure 5 R6 is positioned as part of the output op amp's inverting input (In2) termination. Alternatively, it can be positioned to pick off the wiper voltage of an offset-adjust pot (R14 Figure 1) which is to be fed into the inverting node of the output amplifier. Figure 6 shows this application where an output offset, independent of the gain adjustment stage, is introduced into the inverting node of the output amplifier.

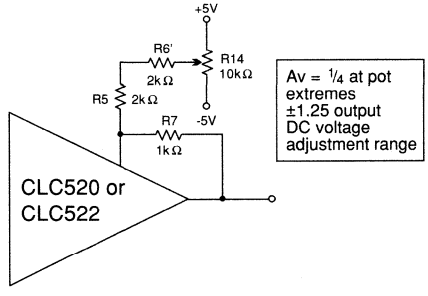

Figure 6: Summing in an output DC offset

VI. Nulling the Output DC Offset

Both the CLC520 and the CLC522 consist of three major functional sections each of which contributes a DC offset voltage to the output of the device; the differential input buffer, the multiplier core and the output amplifier. The offsets produced by the input buffer and the output amplifier can be nulled with the appropriate external circuitry. It will not be possible to completely null the offset effects of the multiplier core because of its nonlinear nature. As a result, a small nonlinear DC offset voltage gain over the adjustment range will always be present at the output of the device. Figure 7 shows the required external circuitry necessary to add the appropriate nulling offsets at both the input buffer and the output amplifier.

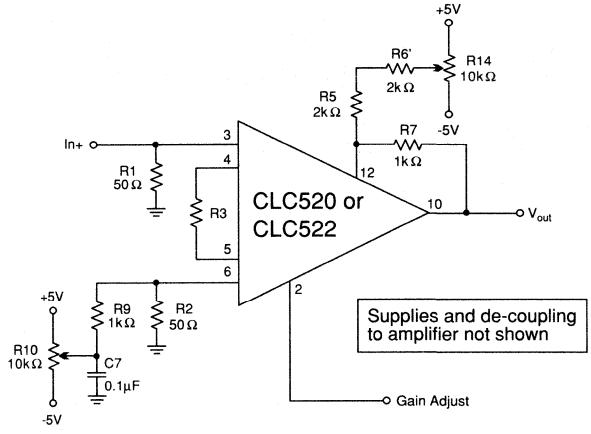

Figure 7: Input and output stage DC nulling

The output stage offset should be trimmed prior to the input stage. With the gain adjust pin set at minimum gain (maximum attenuation), the output stage offset may be nulled independently from the input stage. R14 should be adjusted to yield the desired output error voltage (typically <1mV). Having corrected for the input offset voltage and bias current errors of the output amplifier, returning the gain adjust pin to the maximum gain voltage will allow the input buffer stage DC offset errors to be corrected. With no input signal present, but with matched source impedances at each of the two buffer inputs, R10 of Figure 7 can be adjusted to bring the output to within the desired error band.

Adjusting the input and the output stage offsets at the two gain extremes will hold the output DC error at a minimum at these two points in the gain range. If a more limited gain range is anticipated, the adjustments should be made at these operating points. The non-linear DC error introduced by the multiplier core will cause a residual, gain dependent, offset to appear at the output as the gain is swept from minimum to maximum. Also, neither the input nor the output offset adjustments described here will improve temperature drift effects. Please see the CLC522 data sheet for a more complete discussion of DC offset control.

VII. Printed Circuit Board Layout

The CLC520/522 evaluation boards show a careful attention to parasitic effects in the layout. Generally, any parasitic coupling path to an AC ground (this includes both power and ground planes) should be avoided at any of the signal input and output pins. At the same time, a very good, close proximity, ground plane needs to be provided for the power supply de-coupling capacitors. These boards show the ground plane totally opened up around the part, but close enough to provide minimum parasitic inductance for the the de-coupling capacitor connections. The ground plane on the evaluation boards is also part of a 50Ω transmission line impedance implemented on the two buffer input and gain adjust traces.

Best frequency response flatness is obtained if there is minimal parasitic capacitance to ground on the output of the two input buffers, pins 4 & 5. The gain setting resistor (R3 on these boards) should be in very close proximity to these pins with short, symmetric, PC board traces connecting to pins 4 & 5. As application note OA-16 describes, this trace symmetry to the gain setting resistor will improve the high frequency CMRR in differential amplifier applications.

All of the I/O pins associated with the output stage amplifier are particularly sensitive to parasitic capacitance to an AC ground. The non-inverting input pin (pin 9) should be tied directly to the ground plane for the CLC520, while a 20Ω resistor to ground (R11) should be used for the CLC522. The output amplifier's feedback resistor,(R7), should also be connected between the output and the inverting input (pins 10 & 12) with minimum trace length and parasitic coupling to any AC ground. And finally, the output pin should be buffered from the load by a resistor, (R8), that is acting as either an impedance matching resistor, for driving a doubly terminated transmission line, or as an isolation resistor, when driving capacitive loads. Please see the amplifier data sheets for the recommended series resistor value vs. capacitive load.

Figures 8 and 9 show the board layouts for these two evaluation boards.

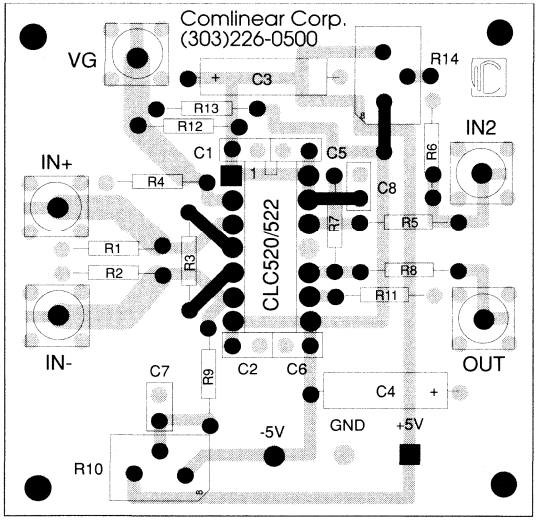

Figure 8: 730029, Rev. B

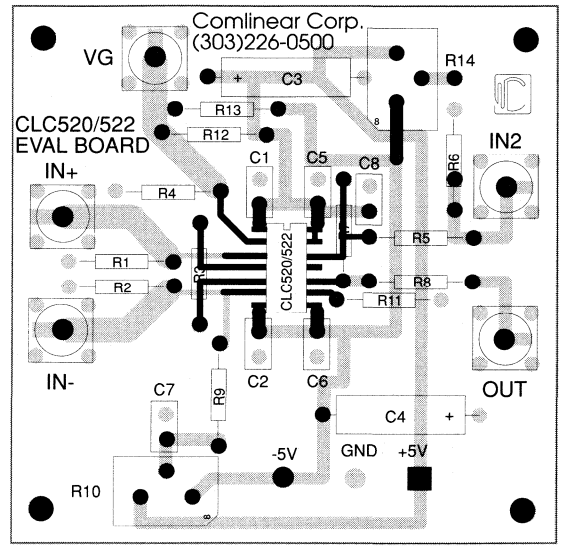

Figure 9: 730033, Rev. B

Evaluation Board Parts List - See the device data sheets along with the discussion and examples shown here when selecting component values.

		Recommended Type
R1,R2	- Input terminating resistors	RN55D 1% metal film
R3	- Gain setting resistor	RN55D
R4	- Gain adjust termination resistor	RN55D
R5,R6	- Output signal summing	RN55D
R7	- Output amplifier feedback res.	RN55D
R8	- Output impedance matching res.	RN55D
R9	- Input offset injection resistor	RN55D
R10	- Input offset adjustment pot	Bournes 10k cermet pot
R11	- Output non-inverting ground res.	RN55D
R12,R13	- Gain adjust default setup	RN55D
R14	- Output offset adjustment pot	Bournes 10k cermet pot

Notes: R11 should be a simple grounding strap for the CLC520. Slightly improved AC response can be obtained by using very low reactance resistors (Precision Resistive Products type PRP-8351) for R7 & R3.

C1,C2,C5,C6,C7	- .1μF Ceramic capacitor
C8	- .01μF Ceramic capacitor
C3,C4	- 6.8μF Tantalum capacitor (Sprague 150D or equivalent.)

The I/O connector styles are:
-SMA (straight) Amphenol 901-144
-SMA (right-angled) Amphenol 901-143

The device through-holes on the 730029 board are large enough to accommodate flush-mount socket pins if it is desired to socket the part. These should be Cambion P/N 450-2598 or equivalent. It is important not to use a standard 14-pin socket since the relatively long connector distance above the board will severely degrade the AC performance of the CLC520 and CLC522.

The 730028 (Rev. B) evaluation board is designed to aid in the evaluation and characterization of the CLC532, 2:1 analog multiplexer. Designed for very wide dynamic range systems, the CLC532 provides a wideband, unity gain, two-channel multiplexer with exceptional switching speeds. High channel isolation and fast pulse settling, make the CLC532 ideal for 12-bit ADC input-multiplexing applications. The CLC532 data sheet provides more detailed performance and applications information.

Basic Operation

The complete circuit schematic of the 730028 evaluation board, including components for optional circuit configurations, is illustrated in Figure 1. The primary connections are shown with solid lines while the optional input and digital interface connections are shown with dashed lines.

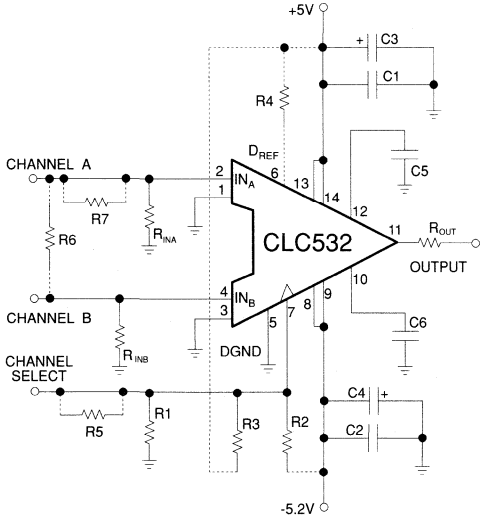

Figure 1: CLC532 Evaluation Board Schematic

The CHANNEL A and B (pins 2 & 4) analog inputs of the CLC532 are buffered high-impedance pins. The two input termination resistors (R_{INA} & R_{INB}) provide impedance matching for the analog sources; a 50Ω environment is assumed. The closed-loop active output of the CLC532 provides a very low output impedance, typically 1.2Ω. For driving 50Ω systems, a 48.7Ω series output resistor (R_{OUT}) will provide a close back matched impedance for 50Ω cables.

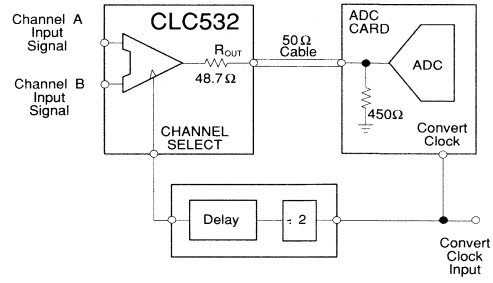

Figure 2: Driving Remote A/D Converter Inputs

Figure 2 illustrates the CLC532 evaluation board connections when driving the high-impedance input of a remote A/D converter. Most high quality, high-resolution, A/D converters employ a high-impedance input stage. This allows the CLC532 to operate with relatively high load resistors (>200Ω), greatly improving CLC532 distortion performance. When the CLC532 drives the A/D converter remotely from a separate board, a 48.7Ω series output resistor prior to a 50Ω connecting cable followed by a 450Ω termination resistor at the input of the A/D converter, results in an effective 500Ω load. When driving A/D converter inputs directly, a 500Ω termination load is recommended with no series resistance.

The CLC532 is capable of functioning with ECL, TTL, and CMOS logic families. Logic compatibility is controlled by D_{REF}. In normal operation, D_{REF} is left floating and the channel SELECT responds to ECL level signals. For TTL and CMOS level SELECT inputs, D_{REF} should be tied to +5V (the CLC532 D_{REF} input is internally buffered through a 2300Ω resistor). TTL and CMOS operation requires the use of a resistor input network for the channel SELECT. Without the input network, SELECT logic levels above 3V will cause internal junction saturation and slow switching speeds.

14

The CLC532 evaluation board is labeled for ±5V supplies. Normal ECL logic, and many A/D converters, employ a -5.2V V_{EE} supply rather than the indicated -5.0V supply. Either value is acceptable with negligible impact on performance.

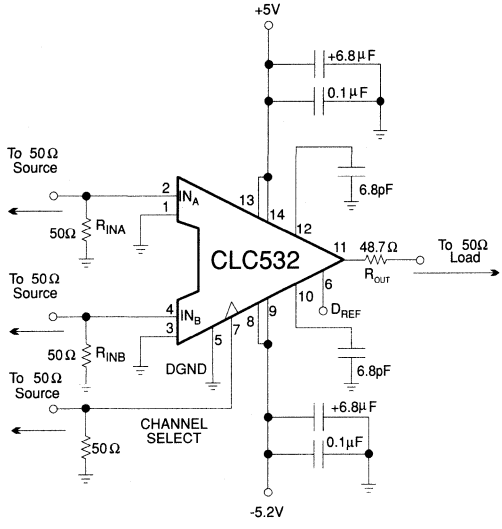

Figure 3: Basic Evaluation Schematic

Figure 3 illustrates the basic CLC532 multiplexer configuration. This configuration terminates both inputs with 50Ω and places a 48.7Ω back-terminating resistor (R_{OUT}) at the output. With D_{REF} left floating (ECL logic levels), the channel SELECT input is terminated with a 50Ω resistor to ground. This configuration assumes a 50Ω signal source provides the channel SELECT input. If standard ECL logic devices are available to drive the channel SELECT input directly, the evaluation board can be configured for standard Thevinen equivalent input terminations. A 50Ω termination resistor to a -2V bias supply can also be used. See *Channel SELECT Logic Interfaces section.* The overall gain seen at the matched load is 0.5V/V (-6dB). The compensation capacitors (C5 & C6) have been selected for a maximally-flat frequency response.

Compensation Capacitors

The compensation capacitors (C5 & C6) are used to *tune* the CLC532's frequency response for a given load. Figure 4 provides the compensation capacitor values for a maximally-flat frequency response. For symmetric slew rates, C5 and C6 should be equal. Figure 5 provides the -3dB bandwidth and slew rate vs. compensation capacitor values. The compensation capacitors can be used to limit the CLC532's noise-bandwidth. Given a single-pole frequency response, the noise bandwidth will be approximately ... (1.57)(f_{-3dB}).

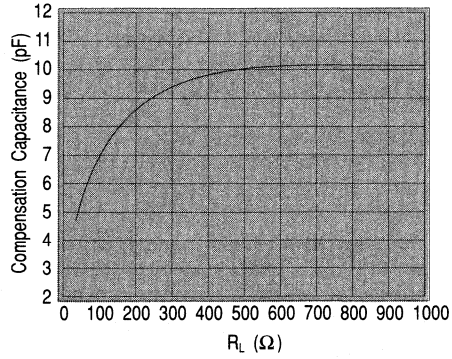

Figure 4: Maximally Flat Frequency Response

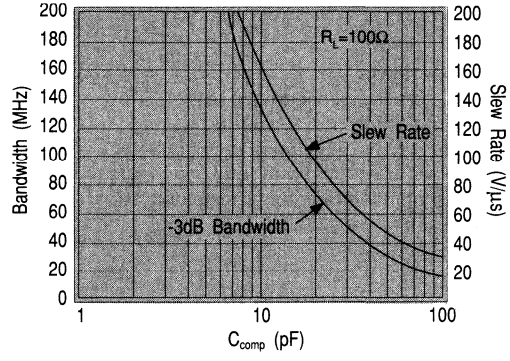

Figure 5: Slew Rate and Bandwidth vs. Compensation

Channel SELECT Logic Interfaces

The CLC532 accepts channel SELECT inputs from a variety of logic families and sources. During evaluation, a signal generator is commonly used to drive the channel SELECT input. Accordingly, the evaluation board has been initially configured with a 50Ω SELECT input termination resistor to ground. When driving channel SELECT with actual ECL, TTL or CMOS logic gates, it will be necessary to add an appropriate input network. The 730028 evaluation board provides the necessary component locations for these networks, and Figure 6 illustrates the recommended TTL and CMOS configurations.

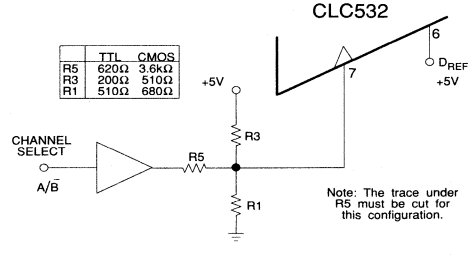

Figure 6. Recommended TTL/CMOS Interface Networks

The TTL and CMOS networks limit the maximum voltage swing at the channel SELECT input (pin 7) to less than 3.0V. Exceeding 3.0V will saturate the internal switching logic and cause slower switching speeds. If the input of the TTL or the CMOS networks is left floating, CHANNEL A will be selected. Use of the series resistor (R5) requires the cutting of the channel SELECT input trace below R5. This is easily accomplished on the back side of the evaluation board.

Driving the CLC532 with standard ECL logic gates requires one of the standard ECL terminations at the channel SELECT input. The network of Figure 7 provides a Thevinen equivalent termination of 50Ω to -2V. If a -2V bias supply is available, the standard 50Ω to -2V is certainly acceptable. Allowing the input to this network to float will select CHANNEL B.

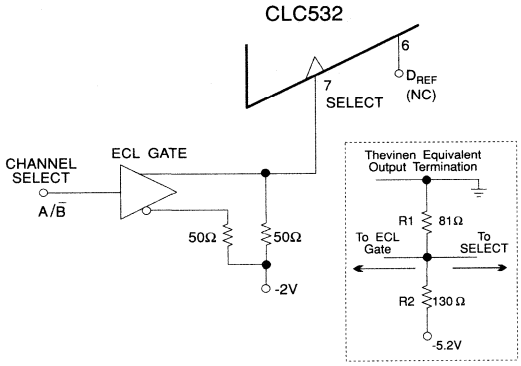

Figure 7: Standard ECL Terminations

Signal Input Options

The CLC532 evaluation board is capable of implementing a switched gain stage by driving CHANNEL B with an attenuated version of the CHANNEL A input signal. Illustrated in Figure 8, this circuit quickly switches between the full amplitude signal at CHANNEL A and the -6dB version of that signal at the input of CHANNEL B. This circuit provides a simple 50Ω termination for the channel SELECT input, although any of the previous circuits are equally acceptable. The series resistor at the input of CHANNEL A (R7) matches its source impedance to that of CHANNEL B (ie. R7=R6||R_{INB}), generating equal poles from the parasitic input capacitances . This type of source impedance matching will also minimize input bias current induced offset errors.

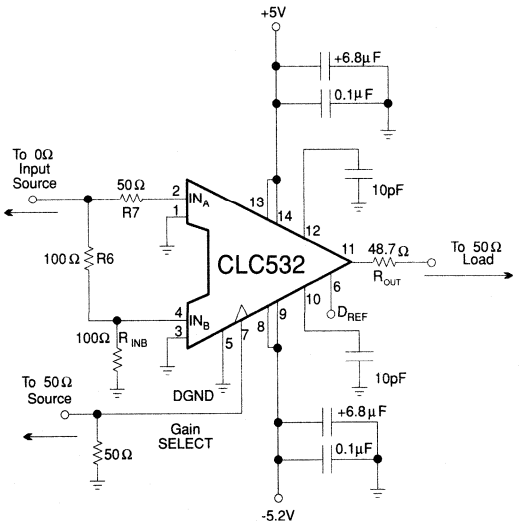

Figure 8: Basic Gain Select Configuration

The switched-gain circuit of Figure 8 should be driven from a low output impedance, wideband, amplifier. Figure 9 uses a CLC406 at a gain of +2V/V to drive both inputs of the CLC532 switched gain circuit. With CHANNEL A selected, the signal at V_{OUT} will be a 0dB (unity gain) version of the input signal. With CHANNEL B selected, the CLC532 will produce a -6dB (0.5V/V) representation of the input signal at V_{OUT}. Figure 10 shows the signal at V_{OUT} using a 10MHz analog input signal, with the channel SELECT toggled at 500kHz. This approach can be easily extended to different gain settings.

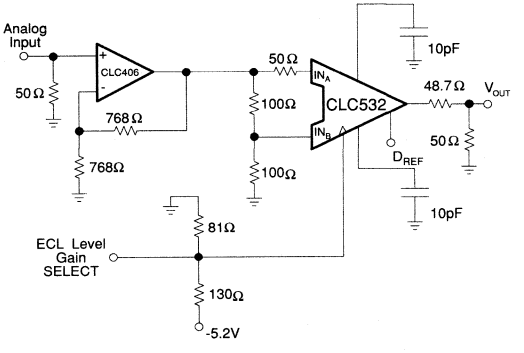

Figure 9: CLC406 Driver for the Switched Gain Configuration

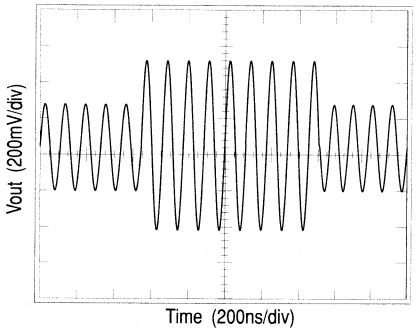

Figure 10: Gain Select Output with 500kHz Toggle Rate

Board Layout Suggestions

The 730028 board has been designed to provide the maximum channel isolation and best fine-scale pulse-settling performance. Channel isolation requires good trace separation between the two inputs, while a ground plane placed between the inputs and the output will serve to isolate the unselected channel from the output.

On the CLC532 evaluation board, the ground connections for the analog input terminating resistors play a strong role in channel isolation performance. The input termination resistor ground connection for CHANNEL B has been placed immediately adjacent to its input SMA connector. The input termination resistor ground connection for CHANNEL A has been placed at right angles to the input trace, and away from the CHANNEL B input. The optimum geometry for input termination resistor ground connections will likely vary from design to design. Some empirical testing may be required.

To achieve high-speed 14-bit settling accuracy, careful attention must be given to ground currents and the electrolytic power supply bypass capacitors. The ground connections of the electrolytic bypass capacitors must have a short and symmetric path to the ground connection of the CLC532 output load. In the case of the 730028 evaluation board, the output SMA connector provides the ground connection for the output load/return currents. Figures 11a,b illustrate the layout for the 730028 evaluation board.

The I/O connectors are SMA (straight) Amphenol 901-144 and SMA (right angled) Amphenol 901-143

The device thru holes are large enough to accommodate flush mount socket pins if socketing is desired. These should be - Cambion P/N 450-2598 or equivalent. Standard DIP sockets are specifically not recommended; the relatively long socket leads will severely degrade the ac performance of the CLC532.

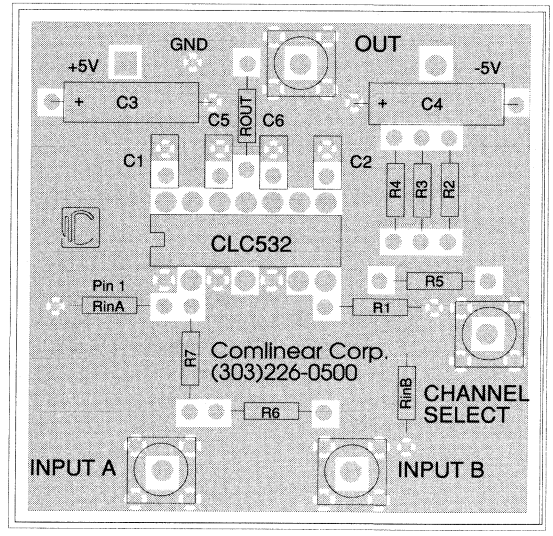

Figure 11a: 780028 Top Metal - Ground Plane (top view)

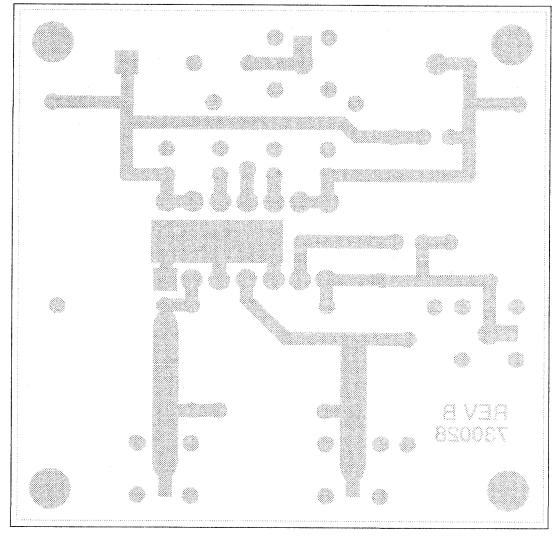

Figure 11b: 780028 Bottom Metal (top view)

CLC533 Evaluation Boards Part Numbers 730035/730039

The CLC533 is a high-speed 4:1 multiplexer with buffered inputs and outputs. This monolithic device has been designed using an advanced complimentary bipolar process. The CLC533 evaluation boards (two versions) have been designed as evaluation platforms for CLC533AJP (DIP package) and the CLC533AJE (SOIC package). The part number for the evaluation board supporting the DIP package is 730035, and that for the board supporting the SOIC is 730039.

Figure 1 shows the schematic of the circuit employed on the boards. For a detailed description of device performance please refer to the individual detail data sheet.

The evaluation board has been designed and layed out in a manner to maximize the isolation between the input channels. The steps that have been taken to aid in this include: separation of the inputs as much as is practical, strips of ground plane separating the input traces and the use of termination resistors that have been physically isolated from one another. A strip of ground plane has been placed between the two rows of pins to minimize the interference between the inputs and the outputs of the device.

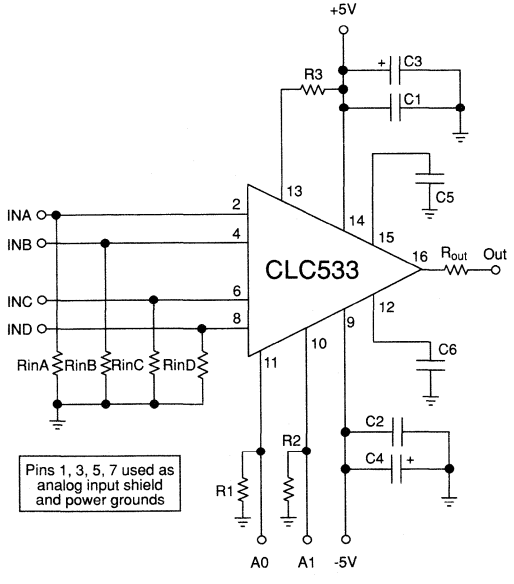

Figure 1: Schematic of CLC533 Evaluation Board

Digital Interface and Channel SELECT

The CLC533 functions with TTL, CMOS and ECL logic families. The D_{REF} pin determines logic compatibility. With D_{REF} left open (R_3 not inserted in board) A_0 and A_1 will respond to ECL level inputs. R_1 and R_2 can be used to set input termination networks as required by the driving gate logic family. If D_{REF} is tied to +5V through R_3 (approximately 1kΩ), then the select inputs will respond to TTL or CMOS input levels. Note that D_{REF} is internally isolated by a 2300Ω resistor. R_1 and R_2 should be left open in TTL or CMOS mode.

Input Signal Termination

The analog inputs to the board are brought in through four SMA connectors. The input signals are terminated with RinA, RinB, RinC, and RinD, these resistors should be chosen to match the transmission line impedance of the cable bringing the signals to the board, typically 50Ω or 75Ω.

Power Supplies

The CLC533 operates off of two power supplies, nominally +5V and -5V. Use of an ECL -5.2V supply rather than the -5V supply is allowed/recommended for ECL. The supplies used should be capable of providing 100mA of current each.

Applications Support

Comlinear maintains a staff of applications engineers who are available for design and applications assistance.

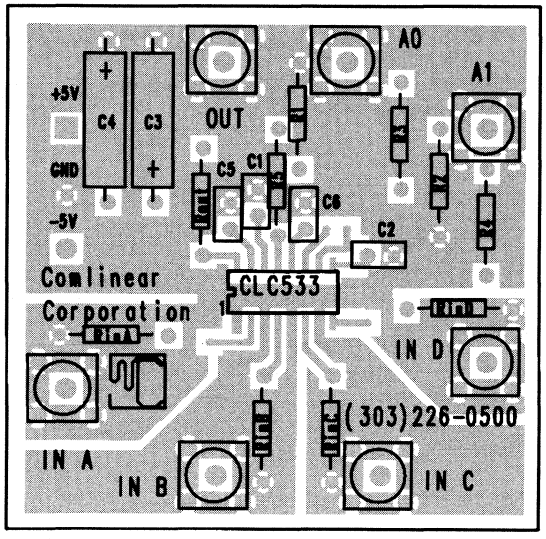

Figure 2: Top layer metal - circuit side (top view)
730039 SOIC version

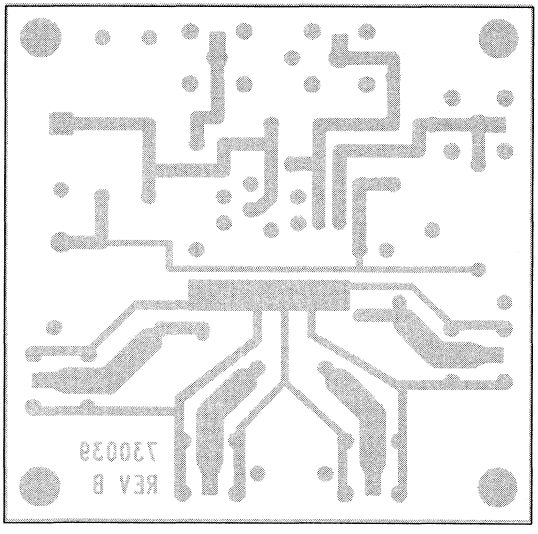

Figure 3: Bottom layer metal (top view)
730039 SOIC version

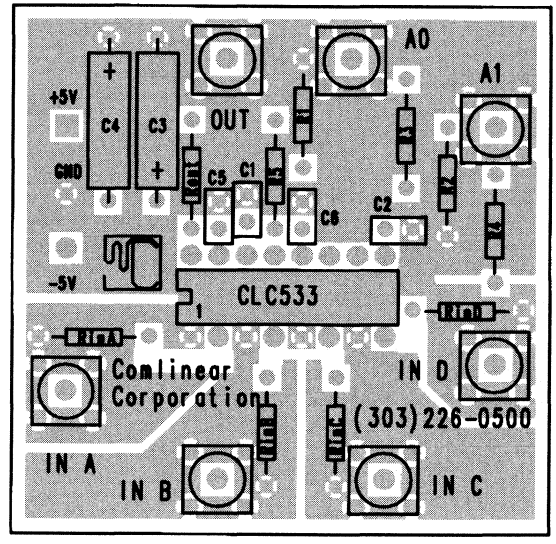

Figure 4: Top layer metal - circuit side (top view)
730035 DIP version

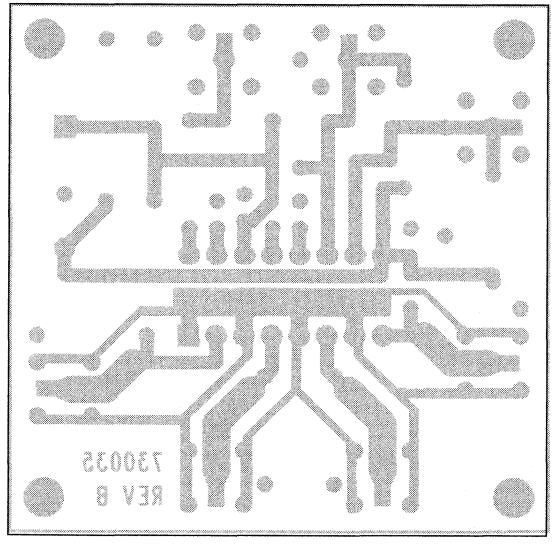

Figure 5: Bottom layer metal - (top view)
730035 DIP version

The #730019 PCB from Comlinear is intended to allow the easy evaluation of either the CLC560 or CLC561. These are hybrid DriveR amplifiers primarily intended to drive high signal levels into a matched load with excellent distortion and full power bandwidth capabilities. The CLC560 is optimized for the best pulse settling characteristics, with some sacrifice in full power bandwidth, while the CLC561 is optimized for the highest slew rate, and hence full power bandwidth, with some sacrifice in the long term pulse settling accuracy.

Figure 1 shows the circuit implemented by the board. Refer to the individual amplifier data sheets for a detailed description of operation. Briefly, however, the DriveR amp topology achieves an equivalent output impedance without the need for a discrete matching resistor in series with the output. The CLC560/561 are primarily intended for non- inverting applications with the input impedance set by R_{ni}. R_f primarily determines the output impedance while R_g, having set a particular R_f, will set the no load gain. The actual voltage gain to the load must also include any voltage divider effect from the output impedance to the load. Figure 2 summarizes the design equations for achieving a desired output impedance and gain. Note that an external compensation capacitance, C_x, must be included for flat frequency response. The equation shown assumes a load matched to the output impedance.

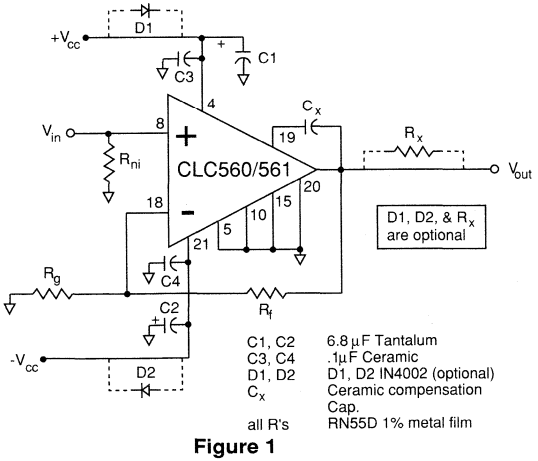

Figure 1

Several optional features are included in the schematic of Figure 1. First, since reversed supplies will destroy the CLC560/561 amplifiers, a provision for series diodes (type 1N 4002 or equiv.) has been provided on the board. If D1 and D2 are inserted into the board, the power supply traces in parallel should be cut. Dropping the power supply voltage through these diodes will slighty decrease the full scale output voltage swing and worsen the 2nd harmonic distortion by about 1dB.

SUMMARY DESIGN EQUATIONS AND DEFINITIONS

$$R_f = (G + 1)R_o - A_v R_i$$

R_f - Feedback resistor from output to inverting input

$$R_g = \frac{R_f - R_o}{A_v - 1}$$

R_g - Gain setting resistor from inverting input to ground

$$C_x = \frac{1}{\frac{R_o}{300\left(1 - \frac{2}{R_g}\right)} - .08}$$

C_x - External compensation capacitor from output to pin 19 (in pF)

Where:

- R_o - Desired equivalent output impedance
- A_v - Non-inverting input to output voltage gain with no load
- G - Internal current gain from inverting input to output = 10 ± 1%
- R_i - Internal inverting input impedance = 14Ω ± 5%

Figure 2

Second, it is sometimes advantageous to implement a portion of the desired output impedance with a discrete series resistor in the output, R_x. Inserting an R_x into the board will require the output trace on the opposite side of the board from R_x to be cut. Using R_x will decrease the achievable swing at the load, but will improve the output VSWR as shown in the data sheet plots and help protect the part from output short circuit damage.

The evaluation board has been layed out with careful attention to frequency response, distortion characteristics, and thermal managment (see Figure 3,4, and 5) Specially, a continuous ground plane beneath the part has been maintained to allow the use of thermally conductive pad beneath the part as described in the device data sheets. Using this pad to conduct heat into the board, greatly decreases the case temperature in operation. Also, the .1µF supply decoupling capacitors have been carefully placed to achieve a very symmetric ground return path (through the ground plane under the part) to the output load. This is very critical to achieving the specified 2nd harmonic distortion. Finally, the compensation capacitor has been placed to achieve the broadest bandwidth capability for a single sided component loading scheme.

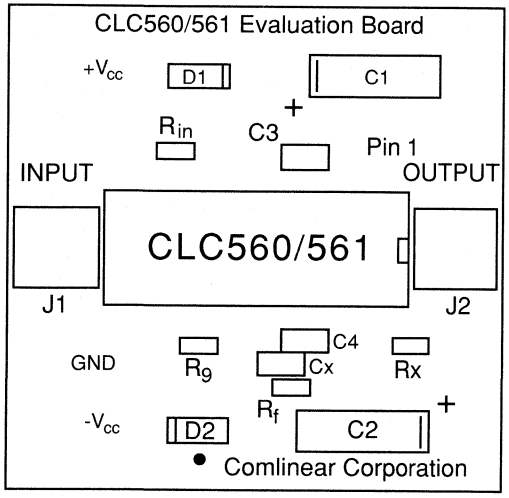

Figure 3: Top side component placement silkscreen
J1, J2 – SMA connector Amphenol 901-144 (straight) or Amphenol 901-143 (right angled)

The CLC560 or CLC561 can be socketed using Cambion flush mount connection jacks.
P/N 450-2548

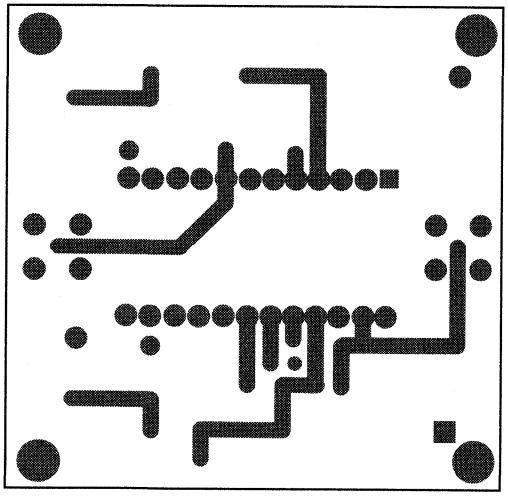

Figure 4: Bottom side metal (viewed from top side)

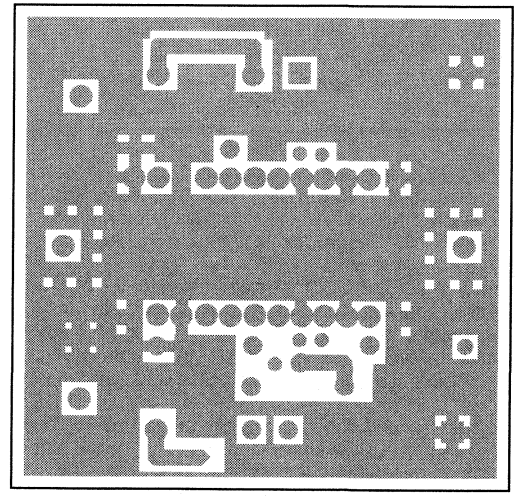

Figure 5: Top side metal

Description

The CLC92X evaluation board (Comlinear part number 730015) is designed to support simple, effective evaluation of the converter. It uses a standard Eurocard connector to make power, ground, and digital connections. Although the board is labelled as a CLC925 Evaluation Board, it can also accommodate the CLC922 and CLC926 ADC's.

Power and Ground

The power supply and ground connections to the Eurocard connector should be as short as possible in order to minimize power supply resonances.

The CLC92X has a well-designed power and ground system internal to the device. Nonetheless, care should be used when adding peripheral digital circuitry to avoid corrupting the ground plane by injecting large amounts of digital switching noise into the ground plane near the CLC92X.

+15V is not used in the CLC922 (Pin 34). For this reason J1-A26, B26 may be connected to ground, connected to +15V, or left open.

Inputs

The convert signal may be provided through the Eurocard connector or through a standard SMA connection on the board. The analog input signal is provided through an SMA connector.

Outputs

For applications requiring a high degree of drive capability (such as driving long lengths of ribbon cable), external TTL drivers with greater drive capability should be used.

Convert Clock

In order to maintain the signal-to-noise performance, the phase noise (or jitter) of the convert pulse must be kept as low as possible. See the CLC92X data sheet for a more complete discussion.

Schematic and Component Placement

The schematic and component placement guide for the evaluation board are shown below.

CLC92X pin	function	connector pin
9	DI (MSB)	BI5
10	D2	BI4
11	D3	BI3
12	D4	BI2
13	D5	BII
14	D6	BI0
15	D7	B9
16	D8	B8
17	D9	B7
18	DI0	B6
19	DII	B5
20	DI2 (LSB)	B4
8	$\overline{DI}$	BI6

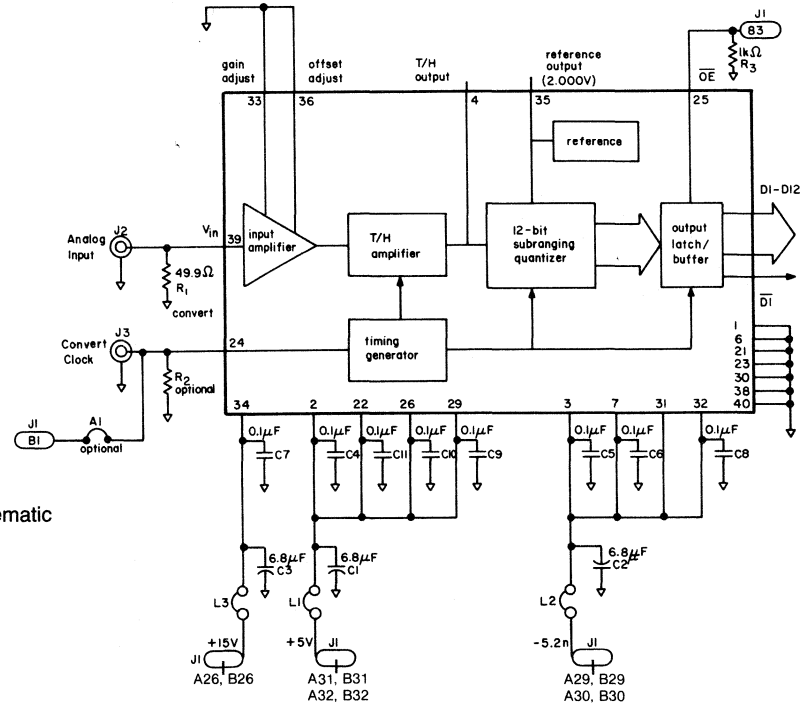

Figure 1: Evaluation board schematic

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EB922/925/926.01 January 1993

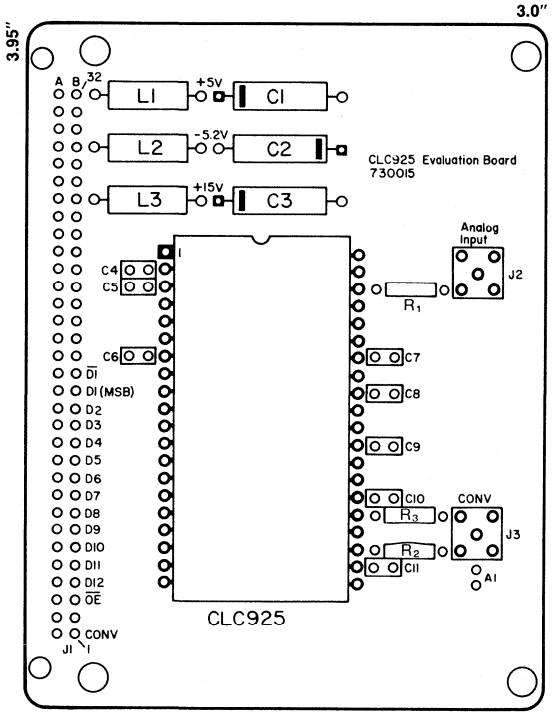


Figure 2: Component placement guide

Note: It is important to carefully note the location of pin #1 on the evaluation board and to insert the CLC92X correctly.

Parts List

CLC92X	12-bit, 10MSPS A/D
730015	printed circuit board
J_1	64-pin Eurocard connector male: Winchester 64P-6033-0431-0 (matching female connector: Winchester 64S-6033-0422-1)
J_2, J_3	SMA connector, female Amphenol 901-144 or equivalent
R_1	50Ω, 1/8W metal film
R_2	optional (may be used to terminate convert clock)
R_3	1kΩ, 1/8W metal film
C_1, C_2, C_3	6.8μF tantalum capacitor (Sprague 150D series or equivalent)
C_4-C_{11}	0.1μF ceramic radial lead
L_1, L_2, L_3	jumper wires
socket	2 pieces Samtec SL-120-T-30
A_1	jumper wires (optional)

Eurocard Connections

Function	Row A	Row B	Function	Row A	Row B
CONV	—	1*	+15V[1]	26	26
OE	—	3			
			GND	27	27
D12(LSB)	—	4	GND	28	28
D11	—	5			
D10	—	6	−5.2V	29	29
D9	—	7	−5.2V	30	30
D8	—	8			
D7	—	9	+5V	31	31
D6	—	10	+5V	32	32
D5	—	11			
D4	—	12			
D3	—	13			
D2	—	14			
D1(MSB)	—	15			
D1	—	16			

*The convert clock is connected to the Eurocard connector only when jumper A_1 is installed.

[1]Not required when using a CLC922.

CLC935/6/7 Evaluation Board Part Number 730025

Description

The CLC935 evaluation board has been designed as an effective evaluation platform for the CLC935 (12-bit, 15MSPS) the CLC936 (12-bit, 20MSPS), and the CLC937 (12-bit, 25.6MSPS) analog-to-digital converters. Connections are made using a standard Eurocard connector for digital and power signals, and standard SMA connectors for the sensitive conversion clock and analog signals.

The board is available blank (part number 730025) and fully assembled (part number E935PCASM). The E935PCASM includes a socket for the CLC935/6/7, but does not include the CLC935/6/7.

Power and Ground

Power supply and ground connections to the Eurocard connector should be kept as short as possible to minimize power supply resonances. Additionally, switching power supplies are strongly discouraged for applications requiring maximum performance.

The converters digital and analog grounds are connected via the analog ground plane. The DATA READY and D_1-D_{14} output drivers have a separate digital ground plane and -5.2V power feed. The two "GND" jumpers can be used to connect the converter and digital ground planes together (the E935PCASM is configured with both ground planes connected via the "GND" jumpers). This arrangement should facilitate ground-loop creation or elimination, as required, to minimize digital system noise corruption of the converter and any associated analog circuitry. Digital ground is available through the Eurocard connector at pins 2A/B and 19A/B. Analog ground in available through the Eurocard connector at pins 27A/B and 28A/B.

Analog Input

The ANALOG INPUT is provided through the SMA connector J1. The E935PCASM employs a 50Ω input termination resistor. Values larger than 200Ω are not recommended unless driven by a low-impedance analog input source. Often in evaluating converters, the ANALOG INPUT is driven by a single-tone source. It should be noted that any jitter present in this source will undermine the apparent quality of the conversion process, specifically SNR (signal-to-noise ratio). To avoid this situation, a very-low noise (low jitter) signal source should be used to provide the ANALOG INPUT signal. Bandpass filtering will likely be required given the generally high harmonic content of very-low noise signal sources.

CONVERT Clock Source

The evaluation board employs an ac-coupled sine-to-ECL converter. The input can come from either the Eurocard connector or the SMA connector J2. In normal operation, the circuit will function very well with a 2Vpp input signal. To maintain the specified SNR performance, a very-low phase noise (low jitter) signal source is absolutely essential in providing the CONVERT signal. Bandpass filtered crystal oscillators or low phase noise synthesizers such as the HP8662 or Fluke T6160B are suitable choices.

The CONVERT clock can be supplied through the Eurocard connector at pins 1A,B. U6 can be left in-circuit if buffering of the CONVERT signal is desired. Some "patch" wiring will be required to provide adequate termination of the Eurocard derived signals. It should be noted that the converter references the CONVERT input to analog ground. Please refer to the schematic on the following pages.

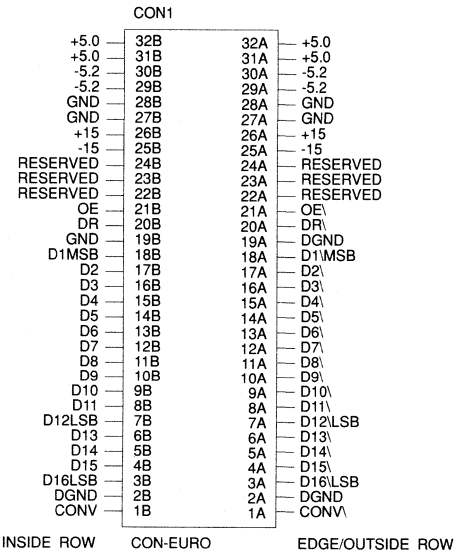
Outputs

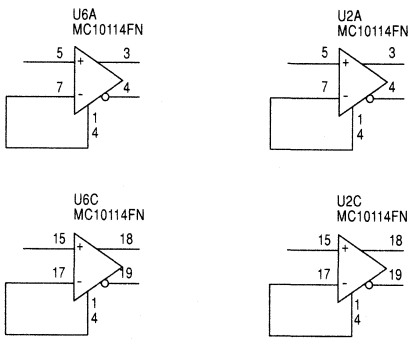
The CLC935/6/7 converters employ "constant current" ECL compatible outputs. This unique design minimizes noise inside the hybrid, but requires buffering, preferably near the converter. The evaluation board employs MC100E151 hex latches to perform this function.

Although no termination resistors are needed for the CLC935/6/7, the 100E151's, however, do require standard ECL terminations. Having been setup as differential outputs through the Eurocard connector, it is expected that the user will provide suitable ECL terminations on the receiving side of the evaluation board connector. Simple 390Ω pull-down resistors to -5.2V have proven effective given the speed range of the CLC935/6/7 converters.

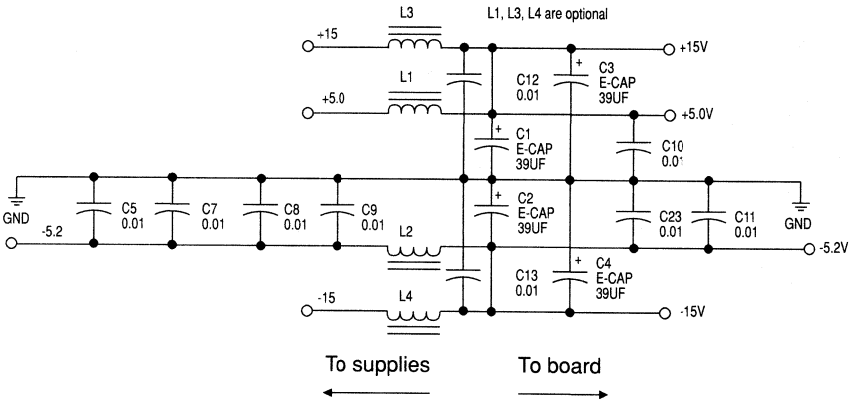
The DATA READY signal is also available from the Eurocard connector. This signal is derived in such a way as to minimize any loading or distortion effects on the CONVERT signal used for the converter itself. The DATA READY signal is also used to clock the output latches U3 to U5, and has been terminated on board. If desired, the DATA READY termination can be relocated to a more appropriate position in the evaluation system.

The output coding of the converter is controlled through two jumpers. The MSB and $\overline{\text{MSB}}$ jumper determines which of the converter's MSB outputs is presented to the latches, while JP1 controls the inversion of the LSB's (D_2 to D_{12}). The E935PCASM comes configured for binary output with the MSB jumper installed. Please refer to the CLC935/6/7 data sheet for more details on output coding.



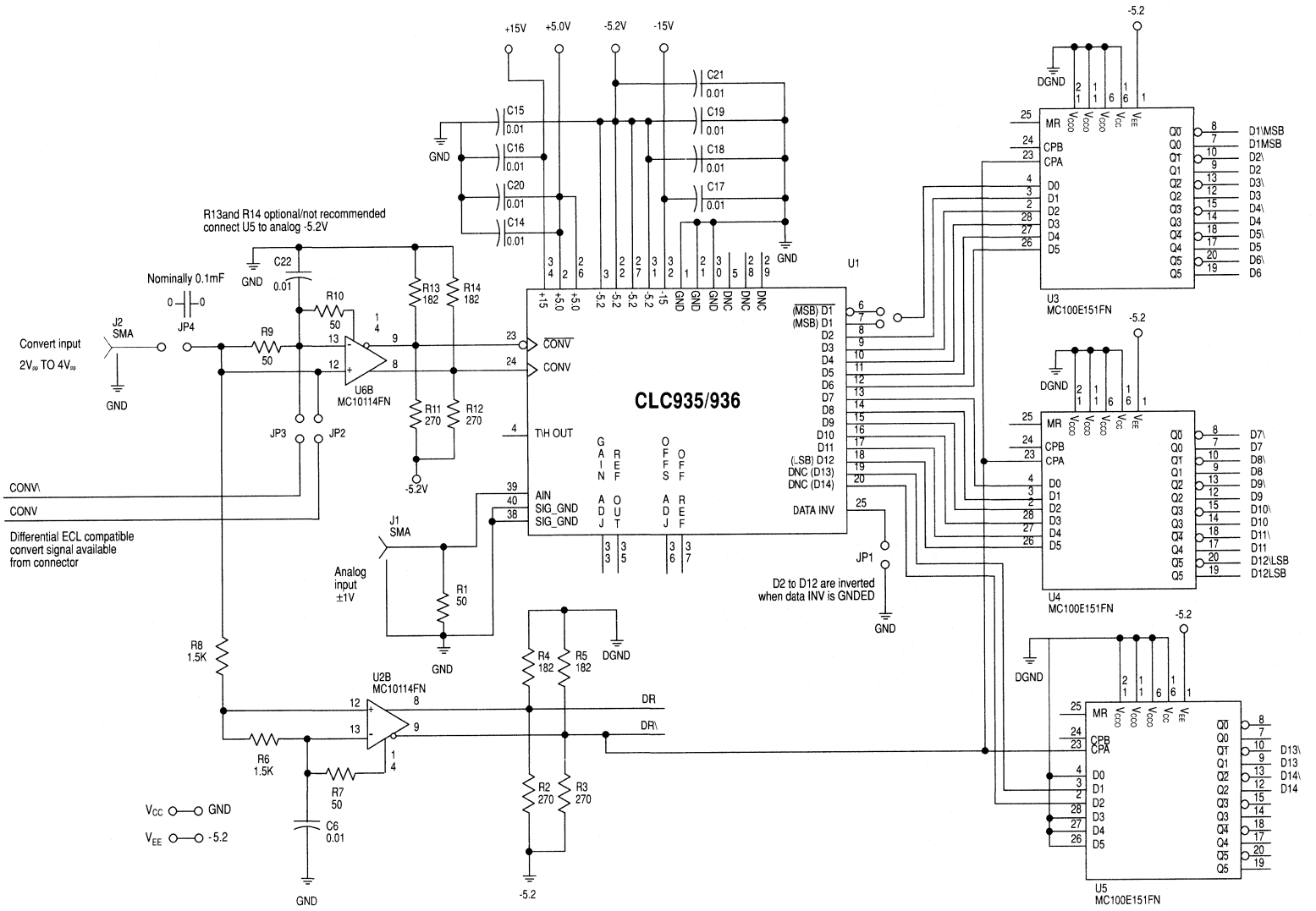


These circuits not used



Bill of Materials

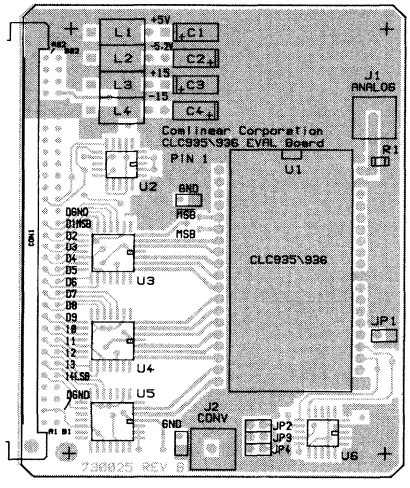
Quan.	Referency	Part
1	CON1	Eurocard Connector Male-Winchester 64P-6033-0431-0; Matching Female - Winchester 64s-6033-0422-01.
4	C1,C2,C3,C4	39µF Tantalum (Sprague 150D series or equivalent)
19	C5,C6,C7,C8,C9,C10, C11,C12,C13,C14,C15, C16,C17,C18,C19,C20, C21,C22,C23	0.01µF, Style 1206
4	JP1,JP2,JP3,JP4	JUMPER
2	J1,J2	SMA, Amphenol 901-144 or equivalent
4	L1,L2,L3,L4	Phillips, VK-200-19
4	R1,R7,R9,R10	50Ω, Style 1206
4	R2,R3,R11,R12	270Ω, Style 1206
4	R4,R5,R13,R14	182Ω, Style 1206
2	R6,R8	1.5kΩ, Style 1206
1	U1	CLC935/6/7
2	U2,U6	MC10114FN
3	U3,U4,U5	MC100E151FN
2	Socket Strip	Samantec SL-120-T-30
1	PCB	730025


+15V
+5.0V
-5.2V
-15V
C21 0.01
C19 0.01
C18 0.01
C17 0.01
C15 0.01
C16 0.01
C20 0.01
C14 0.01
GND
R13and R14 optional/not recommended
connect U5 to analog -5.2V
C22 0.01
Nominally 0.1mF
JP4
J2 SMA
Convert input
2Vpp TO 4Vpp
R9 50
R10 50
R13 182
R14 182
U6B MC10114FN
R11 270
R12 270
JP3
JP2
-5.2V
CONV\
CONV
Differential ECL compatible
convert signal available
from connector
J1 SMA
Analog
input
±1V
R1 50
R8 1.5K
R6 1.5K
R7 50
C6 0.01
U2B MC10114FN
R4 182
R5 182
R2 270
R3 270
DR
DR\
DGND
VCC GND
VEE -5.2
CLC935/936
GAIN REF
OFFS OFF
AIN
SIG_GND
SIG_GND
T\H OUT
CONV\
CONV
AOUT
AREF
U1
(MSB) D1
(MSB) D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
(-SB) D12
DNC (D13)
DNC (D14)
DATA INV
JP1
D2 to D12 are inverted
when data INV is GNDED
U3 MC100E151FN
U4 MC100E151FN
U5 MC100E151FN
D1\MSB
D1MSB
D2\
D2
D3\
D3
D4\
D4
D5\
D5
D6\
D6
D7\
D7
D8\
D8
D9\
D9
D10\
D10
D11\
D11
D12\LSB
D12LSB
D13\
D13
D14\
D14

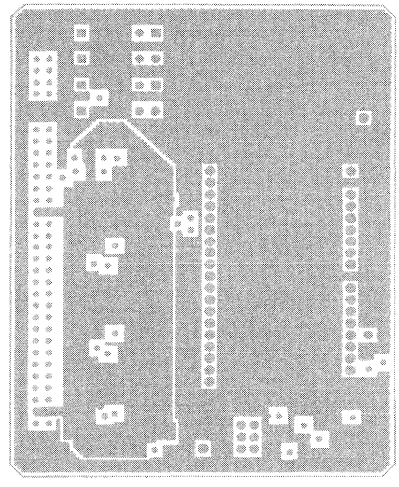
Layout Information

The four layers which makeup the CLC935/936/937 evaluation board are detailed below. The top and bottom layers also include silk-screen data indicating component placement. All reductions are TOP VIEW. Actual board dimensions are 4.00"x3.00". The bare printed circuit board is available from Comlinear Corporation as part number 730025. For further applications assistance, please call the Comlinear Applications Group, 1-800-776-0500.

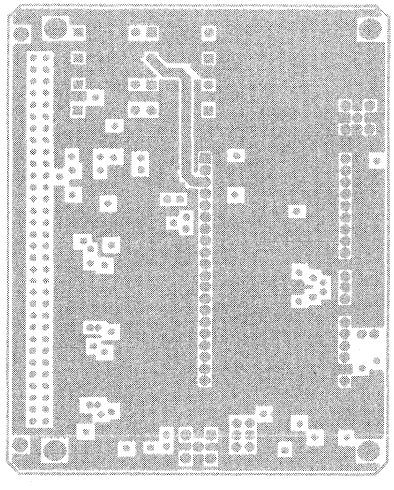
Layer 1 - Top Metal



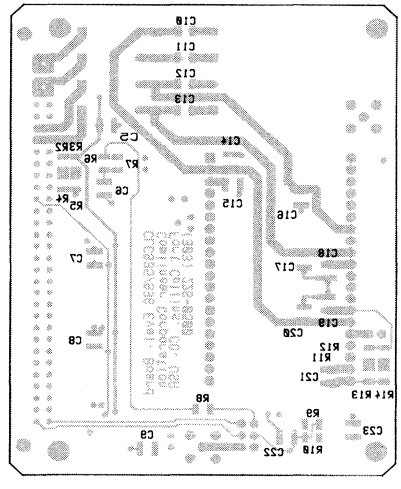
Layer 2 - Ground Plane



Layer 3 - Power Plane



Layer 4 - Bottom Metal



Description

An evaluation board is available for the CLC940, P/N 730011. The board is user-configurable for either TTL or ECL operation (see Figure 4).

On the board near pin 1 of the CLC940 are four points labeled "A," "H," "B," and "T" (see Figures 4 and 5). Jumpers are connected between these points to provide the CLC940 with the bias voltages needed for single-ended ECL and TTL. Points "H" and "T" go to the "hold" and "track" inputs, respectively. Point "A" goes to the "digital input," and "B" goes to the TTL/ECL bias network.

The connection scheme for TTL requires that the bias network provide +1.4V at point "B." The +15V supply is used and the diodes are inserted so as to be forward biased (see Figures 3 and 4). Jumpers are used to connect "A" to "H" and "B" to "T."

Single-ended ECL is connected similarly, however the bias network should be configured to provide −1.4V at point "B." The −15V supply is used and the diodes are inserted so as to be forward biased (see Figures 2 and 4). Jumpers are used to connect "A" to "H" and "B" to "T."

For differential ECL, signals can be sent directly to points "H" and "T," the "hold" and "track" inputs respectively. The bias circuit and jumper connections should be omitted (see Figures 1 and 4).

The resistor at the digital input, R_D, is omitted for TTL and ECL, but is otherwise used to set the (digital) input impedance. The resistor at the analog input, R_{in}, is selected for the desired input impedance. The output resistor, R_{out}, is selected for the desired output impedance and for optimum capacitive-load performance (see the R_{out} vs. Load Capacitance plot on the plot page of the data sheet).

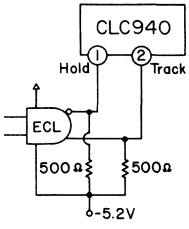


Figure 1: Differential ECL control

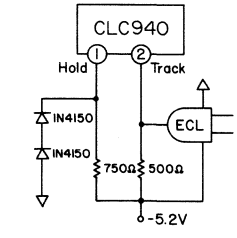


Figure 2: Single-ended ECL control

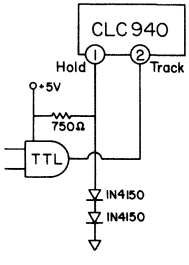
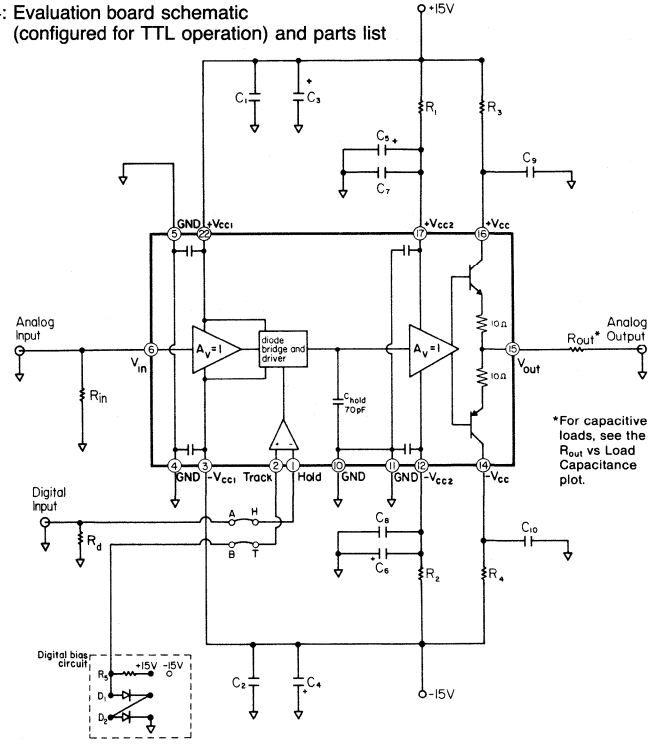


Figure 3: TTL control

Figure 4: Evaluation board schematic (configured for TTL operation) and parts list



For TTL, use the bias circuit shown. Omit R_d.

For single-ended ECL, reverse the direction of the diodes and connect R_s to −15V instead of +15V. Omit R_d.

For differential ECL, **omit** the jumper connections "A" to "H" and "B" to "T." Omit bias circuit. Make connections directly to "H"and "T."

14

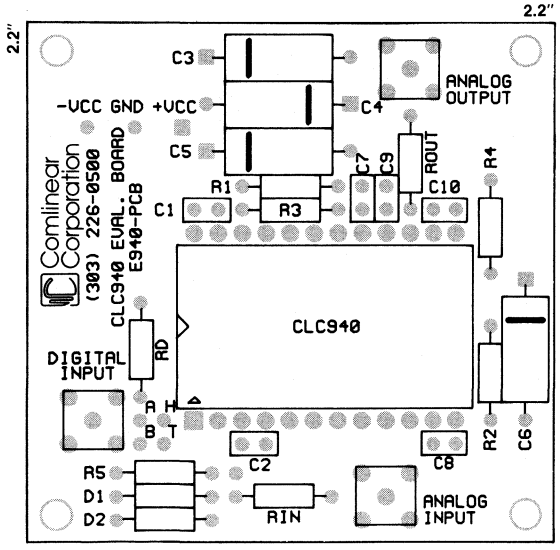


Figure 5: Component placement guide

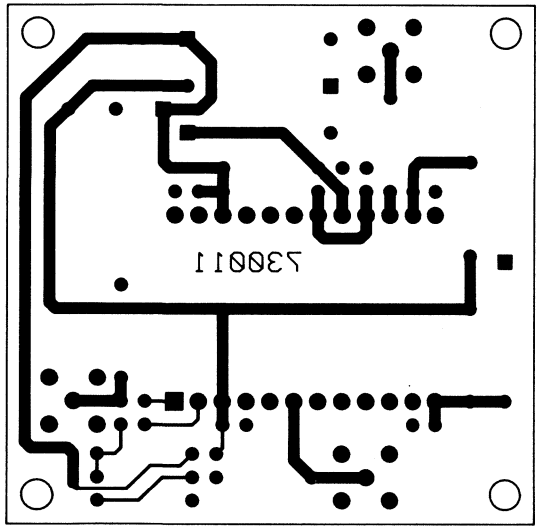


Figure 6: Solder side (bottom) as viewed from component side (top)

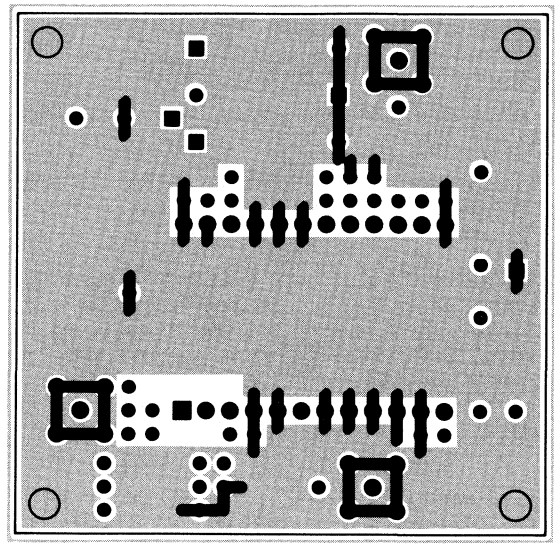


Figure 7: Component side (top) showing extensive ground plane

Parts List

Resistors:

R_1	200Ω	R_3	33Ω	R_5	2.6kΩ	R_{out}	*	*selected for desired input/
R_2	200Ω	R_4	33Ω	R_{in}	*	R_d	*	output impedance

Capacitors: (35V, +80% | −20%)

C_1	0.01μF ceramic radial lead	C_6	2.2μF (Sprague 150D series)
C_2	0.01μF ceramic radial lead	C_7	0.01μF ceramic radial lead
C_3	6.8μF (Sprague 150D series)	C_8	0.01μF ceramic radial lead
C_4	6.8μF (Sprague 150D series)	C_9	0.01μF ceramic radial lead
C_5	2.2μF (Sprague 150D series)	C_{10}	0.01μF ceramic radial lead

Diodes:

D_1	1N4150
D_2	1N4150

Hardware: (optional)
SMA connectors Amphenol 901-144 (straight)
or Amphenol 901-143 (angled)
"Socket" Cambion flush mount connector jacks 450-2598-01-06-00

CLC942 Evaluation Board Part Number 730017

Description

The CLC942 is a 12-Bit accurate, fast sampling, wideband track-and-hold amplifier which offers ultra-fast switching performance plus an unprecedented array of supporting specifications.

The CLC942 evaluation board (Comlinear part number 730017) is designed to support simple, effective evaluation of the CLC942 track-and-hold.

The board is user-configurable for TTL or ECL operation. The track/hold input may also be configured for a nominal input threshold of zero volts.

Power Supplies

The CLC942 uses +15V, +5V, and −5.2V supplies. If desired, −5V can be substituted for the −5.2 supply without degrading performance.

Inputs and Outputs

SMA connections are used to connect the track/hold input (SMA1), signal input (SMA2) and output (SMA3).

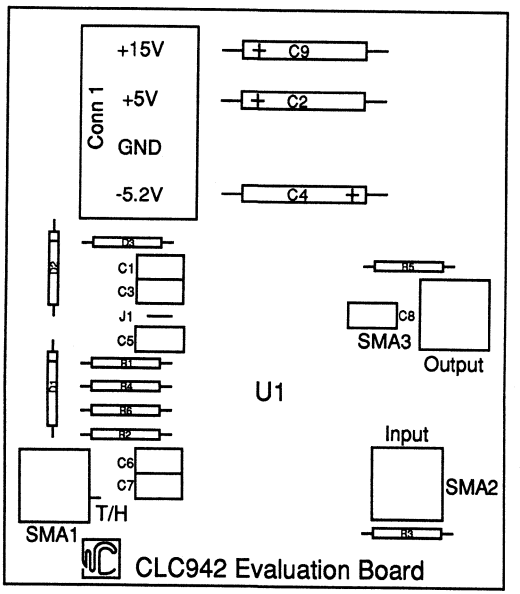
Track/Hold Input

The track/hold input may be set up for nominal TTL and ECL thresholds. In addition, it may be set up for a zero volt threshold. (See schematic for details.)

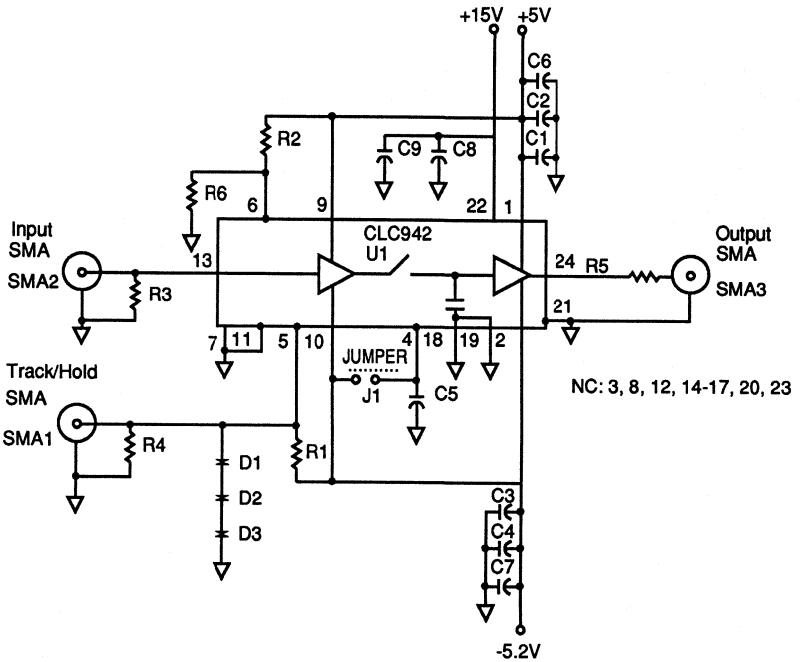
In order to maintain best signal to noise, the phase noise (or jitter) of the track/hold input must be kept as low as possible. Crystal oscillators or low phase noise synthesizers such as the HP8662 or Fluke T6160B are suitable.

Parts List

C1, C3 C5-C8	0.1 μF ceramic radial lead
C2, C4, C9	6.8 μF tantalum, Sprague 150D series or equivalent
D1-D3	1N4148
J1	Jumper wire (optional)
R1	50, 1/8W metal film
R2	3.9k, 1/8W metal film
R3	50, 1/8W metal film
R4	50, 1/8W metal film
R5	50, 1/8W metal film
R6	1.5k, 1/8W metal film (optional)
SMA1-SMA3	SMA connector, female Amphenol 901-144 or equivalent
U1	CLC942 track-and-hold
730017	Printed Circuit Board
socket	24 pieces Cambion 450-2598-01-06-00 or equivalent



Component Placement Guide



Configuration:

Threshold	J1	R1	R2	R4	D1-D3	R6
1. ECL	Short	130 Ohms	X	82 Ohms	Open	Short
2. TTL	Open	Open	3.9K	Open	Include	1.5K
3. Gnd Ref'd	Open	Open	X	50 Ohms	Open	Short

X-Not Critical

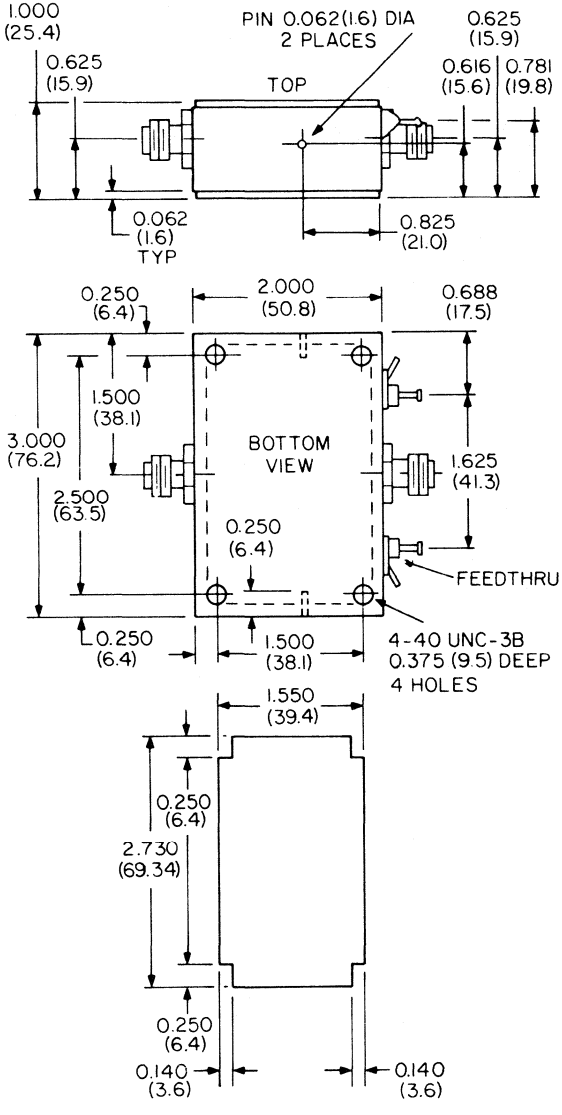
PRODUCT ACCESSORIES Section Two

The following product accessories, for use in conjunction with Comlinear products, are available by contacting the applicable company listed.

Adams-Russell, Modpak Division M/A-COM
80 Cambridge Street
Burlington, Massachusetts 01803-0964

Phone: (617) 273-3330
FAX: (617) 273-1921

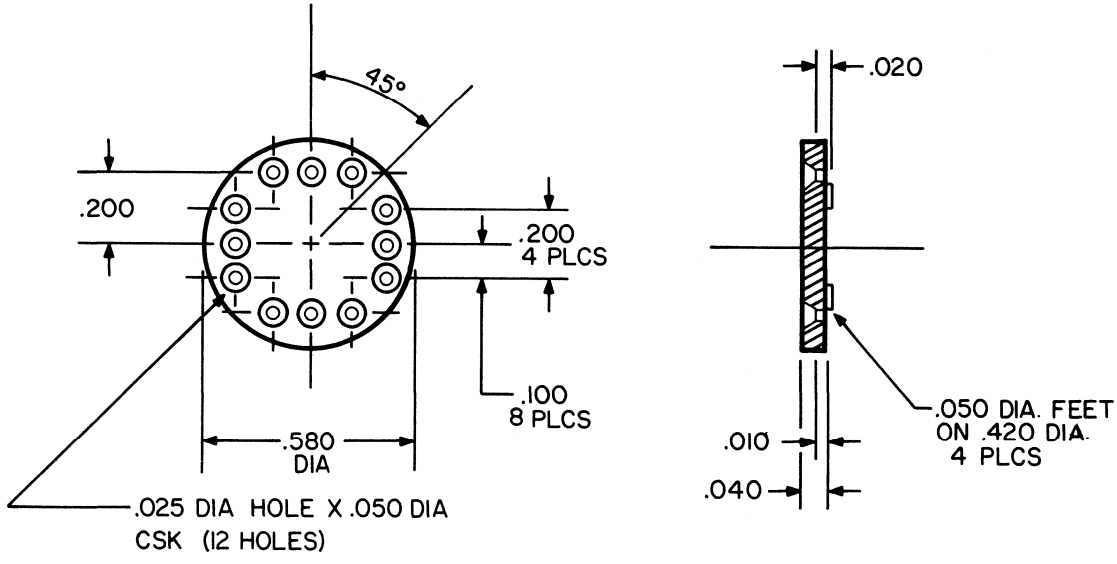
PART DESCRIPTION: Evaluation PC/board cases for use with the following PC evaluation boards: CLC104, CLC103, CLC203, CLC2XX, CLC300
Part Number: 7042



14

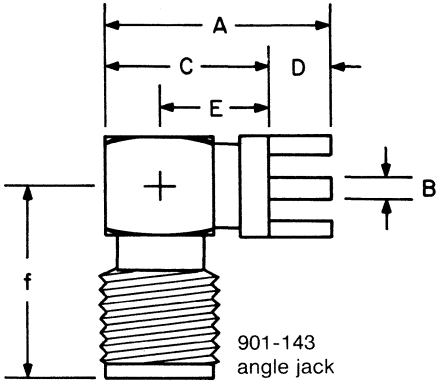
AFE
Accessories For Electronics, Inc.
800 Merrick Road
Baldwin, New York 11510
Phone: (516) 546-1751
FAX: (516) 867-1922

PART DESCRIPTION: TO-8 Non-Conductive Spacer
Part Number: 965-593N



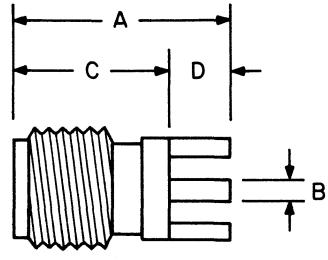
Amphenol Corporation
RF/Microwave Operations
One Kennedy Avenue
Danbury, Connecticut 06810
Phone: (203) 743-9272
FAX: (203) 796-2032

PART DESCRIPTION: SMA Receptacles – Printed circuit mount for use with the following PC evaluation boards: CLC110, 8-pin monolithic amplifiers, CLC500, CLC925, CLC940.
Part Number: 901-143



901-143
angle jack

PART DESCRIPTION: SMA Receptacles – Printed circuit mount for use with the following PC evaluation boards: CLC110, 8-pin monolithic amplifiers, CLC500, CLC925, CLC940.
Part Number: 901-144

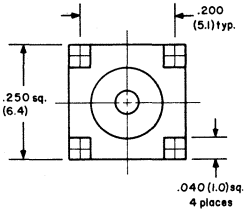


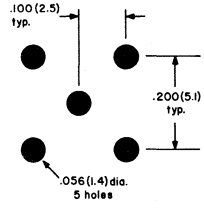
901-144
straight jack

Terminal	Dimensions, inches (millimeters)						Mfg. Hole	Notes	Amphenol Number
	a	b	c	d	e	f			
Blunt Post .156" (4.0) long	.531(13.5)	.050(1.3)	.375(9.6)	.156(4.0)	.250(6.4)	.460(11.7)	T	Angle Jack BeCu Body Brass Legs	901-143

Terminal	Dimensions, inches (millimeters)						Mfg. Hole	Notes	Amphenol Number
	a	b	c	d	e	f			
Blunt Post .156" (4.0) long	.531(13.5)	.050(1.3)	.375(9.6)	.156(4.0)	—	—	T	Straight Jack BeCu Body and Legs	901-144

Mounting Details



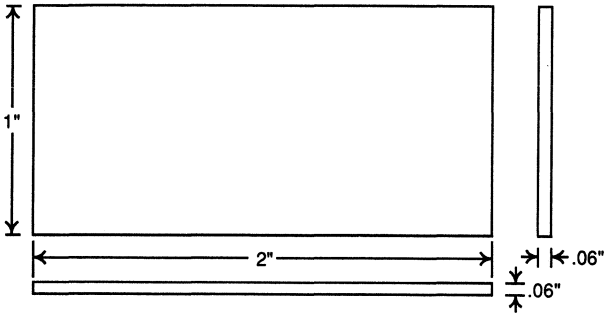


Bergquist
5300 Edina Industrial Boulevard
Minneapolis, Minnesota 55435-3791

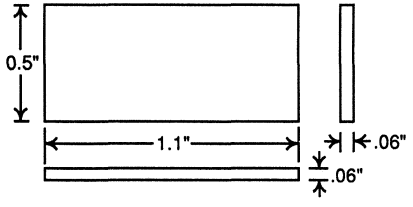
Phone: 1-800-347-4572
FAX: (612) 835-4156

PART DESCRIPTION: Several thermally conductive pads for use between several hybrid product packages and a top surface ground plane to enhance heat conduction to the external environment.

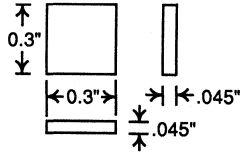
These are all SIL-PAD 200 material with adhesive on one side. Part numbers are Comlinear part numbers at Bergquist.



Part Number: 550007
Used for 40-pin, 1.1" wide ceramic DIP package (e.g. CLC922, 925, 926, 935, 936). Thermal impedance 2.6°C - in^2/W (typical).



Part Number: 550006
Used for 24-pin , .6" wide ceramic DIP package (e.g. CLC560, 561, 942).
Thermal impedance 2.6°C - in^2/W (typical).

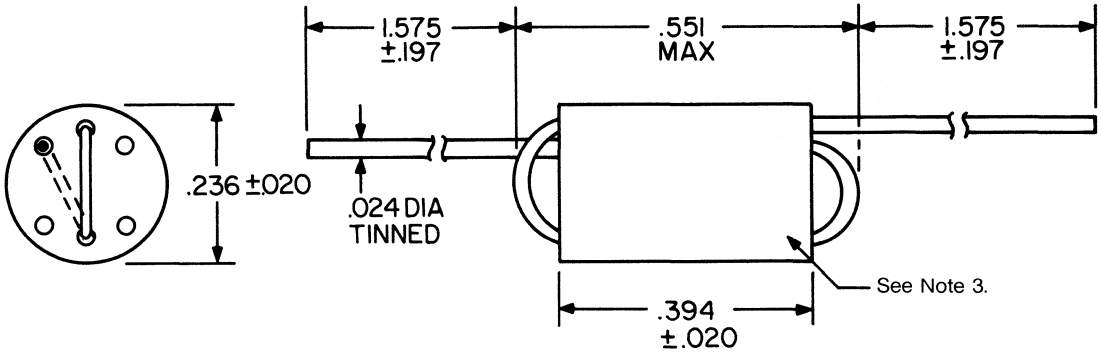


Part Number: 550009
Used for 12-pin, TO-8 package (e.g. CLC231, 205, 206, 207, etc.)
Thermal impedance 2.0°C - in^2/W (typical).

Phillips Components
5083 Kings Highway
Saugerties, New York 12477

Phone: (914) 246-2811
FAX: (914) 246-0486

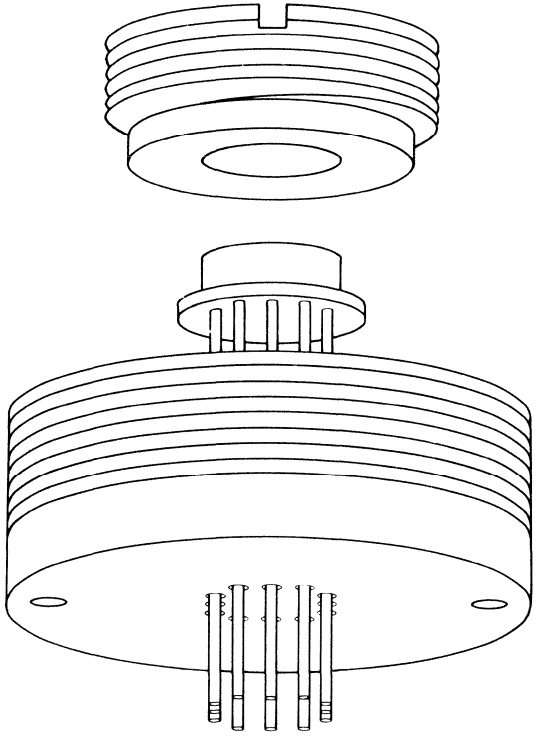
PART DESCRIPTION: Wideband ferrite coil for improved power supply isolation (optional) on the following PC evaluation boards: CLC110, CLC925.
Part Number: VK-200-19



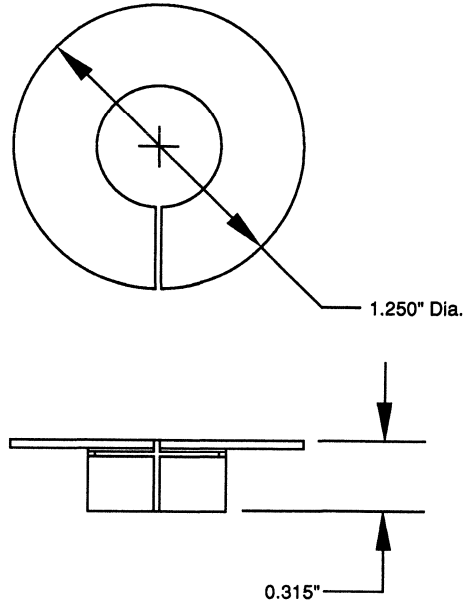
Notes:
1. Windings 1 × 1.5 turns
2. Z Min. (kΩ - - - - .35 @ Freq = 250MHz
3. The ferrite part will be partially covered with a light green color tint.
4. Bare spots on the .024 tinned dia shall be allowed.

Thermalloy, Inc.
P.O. Box 810839
2021 West Valley View Lane
Dallas, Texas 75381-0839
Phone: (214) 243-4321
FAX: (214) 241-4656

PART DESCRIPTION: TO-8 heat sinks
Part Number: 2240B



Part Number: 2268B



Ordering Guide/Return and Warranty Information

Contents

ORDER PLACEMENT

Orders may be placed and information obtained from either your area representative or distributor, via telephone, facsimile and mail, or by contacting Comlinear directly.

If it is determined that a "special" product is required, such as SCD (Specification Control Drawing) products, custom products or specially tested products, we recommend that you call your area representative or the Comlinear Sales Support Group.

In order to provide maximum service and satisfaction, products should be ordered in their country of end use.

Customers requiring formal paperwork such as pro forma invoices or quotations can receive immediate assistance from your area representative or distributor.

When placing your order, please provide as a minimum, the purchase order number, model number, and ship-to and bill-to addresses.

TERMS OF SALE

All shipments are FOB, Fort Collins,Colorado. Comlinear's standard terms are NET 30 days inside the U.S.A. Terms for customers outside the U.S.A. are irrevocable letters of credit or cash in advance unless other terms have been arranged. Detailed standard terms and conditions of sale are available upon request.

TECHNICAL ASSISTANCE

Comlinear is dedicated to providing innovative solutions to high-speed signal processing challenges. To support this effort, Comlinear maintains a staff of research-and-development-level applications engineers, to provide both technical and design assistance. Their experience, laboratory, and computer simulation resources uniquely qualify them to assist you.

SALES SUPPORT

Comlinear's solution to your signal processing needs continues with fast local support of your ordering and product availability needs. Comlinear maintains a network of highly qualified representatives and distributors, covering the United States, Canada, Europe, and Asia. For further information, Comlinear's in-house Sales Support staff is available to assist you. A complete listing of representatives and distributors is located in Section 16 of this databook.

RETURN AND WARRANTY INFORMATION

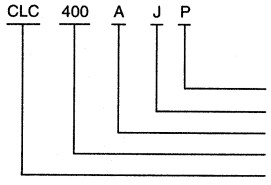
If for any reason, a product must be returned to Comlinear, a Return Material Authorization (RMA) should be used. This can be obtained by contacting your area representative, distributor, or Comlinear. The product should then be shipped prepaid to the Fort Collins, Colorado, facility for evaluation or repair. It is requested that a description of the problem and the specific application be included in the return.

All Comlinear Corporation products are warranted against defects in workmanship and materials under normal use for a period of one year from the date of manufacture. Comlinear shall have the option after evaluation to either replace or repair the defective product. This warranty does not apply to any products which have been subject to misuse (including ESD damage), neglect, accident or modification, or that have been soldered or altered during assembly, and are not capable of being tested by Comlinear under normal test conditions.

For additional warranty information, please refer to Comlinear's Standard Terms and Conditions of Sale (available upon request).

PART NUMBERING SYSTEM

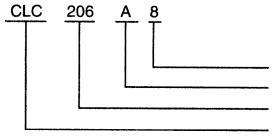
MONOLITHIC PRODUCTS:



PACKAGE
B - CERDIP
C - Die
D - Sidebrazed ceramic DIP
E - Small outline (SO)[1]
L - Leadless chip carrier
P - Plastic DIP

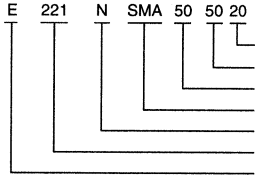
SCREENING LEVEL[2]
C - Commercial
I - Industrial
J - Industrial
L - Industrial (Die)
M - Military Hi-Rel
S - Level S
8 - MIL-STD-883, Level B

HYBRID PRODUCTS:

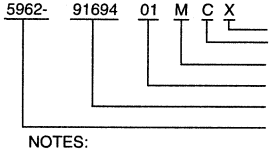


SCREENING LEVEL[2]
I - Industrial
K - Industrial Hi-Rel
M - Military Hi-Rel
S - "Comlinear" S level
8 - MIL-STD-883, Level H

MODULAR AND ENCASED PRODUCTS:



DESC SMD PRODUCTS:



LEAD FINISH
A - Hot solder dip
C - Gold electroplate
X - Any of the above

NOTES:
1. Tape and reel packaging available; order by putting" – TR" at end of part number.
2. See Section 2, Quality and Reliability, for detail process flows.
3. DESC SMD devices are marked with the SMD number ONLY; no Comlinear number.

Sales Offices/ Distributors

Contents

UNITED STATES SALES REPRESENTATIVES

ALABAMA
Beacon Electronics
Huntsville, Alabama
(205) 881-5031
FAX (205) 883-9516

ALASKA
Comlinear Corporation
Fort Collins, Colorado
(800) 776-0500
FAX (303) 226-0564

ARIZONA
Cain Technology
Tempe, Arizona
(602) 966-4322
FAX (602) 968-5132

ARKANSAS
The Thorson Company
Dallas, Texas
(214) 233-5744
FAX (214) 702-0993

CALIFORNIA
(Northern)
Cain White & Co.
Los Altos, California
(415) 948-6533
FAX (415) 948-0115

(Southern)
Cain Technology
Van Nuys, California
(818) 904-9392
FAX (818) 904-0805

COLORADO
Front Range Microwave
Englewood, Colorado
(303) 791-4405
FAX (303) 791-4406

CONNECTICUT
R.J. Sickles Associates
Lexington, Massachusetts
(617) 862-5100
FAX (617) 863-0684

DELAWARE
Beacon North
Sterling, Virginia
(800) 877-3747
FAX (703) 435-7115

FLORIDA
(Central, Eastern & Southern)
Beacon Electronics
Longwood, Florida
(407) 332-1940
FAX (407) 332-1786

(Panhandle)
Beacon Electronics
Huntsville, Alabama
(205) 881-5031
FAX (205) 883-9516

(Western)
Beacon Electronics
Clearwater, Florida
(813) 796-2378
FAX (813) 796-0075

GEORGIA
Beacon Electronics
Atlanta, Georgia
(404) 256-9640
FAX (404) 256-1398

HAWAII
Comlinear Corporation
Fort Collins, Colorado
(800) 776-0500
FAX (303) 226-0564

IDAHO
Cain Sweet & Co.
Bellevue, Washington
(206) 462-2118
FAX (206) 451-9418

ILLINOIS
(Northern)
Dytec Central
Arlington Heights, Illinois
(708) 394-3380
FAX (708) 394-0270

INDIANA
Dytec Central
Indianapolis, Indiana
(317) 578-0474
FAX (317) 578-0476

IOWA
(Eastern)
Dytec Central
Arlington Heights, Illinois
(708) 394-3380
FAX (708) 394-0270

(Rest of Iowa)
Ohms Technology
Edina, Minnesota
(612) 932-2920
FAX (612) 932-2918

KANSAS

KENTUCKY
Dytec Central
Indianapolis, Indiana
(317) 578-0474
FAX (317) 578-0476

LOUISIANA
The Thorson Company
Dallas, Texas
(214) 233-5744
FAX (214) 702-0993

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R.J. Sickles Associates
Lexington, Massachusetts
(617) 862-5100
FAX (617) 863-0684

MARYLAND
Beacon North
Sterling, Virginia
(800) 877-3747
FAX (703) 435-7115

MASSACHUSETTS
R.J. Sickles Associates
Lexington, Massachusetts
(617) 862-5100
FAX (617) 863-0684

MICHIGAN
Dytec Central
Arlington Heights, Illinois
(708) 394-3380
FAX (708) 394-0270

MINNESOTA
Ohms Technology
Edina, Minnesota
(612) 932-2920
FAX (612) 932-2918

MISSISSIPPI
Beacon Electronics
Huntsville, Alabama
(205) 881-5031
FAX (205) 883-9516

UNITED STATES SALES REPRESENTATIVES

MISSOURI

MONTANA
Front Range Microwave
Englewood, Colorado
(303) 791-4405
FAX (303) 791-4406

NEBRASKA

NEVADA
(Southern & Las Vegas)
Cain Technology
Tempe, Arizona
(602) 966-4322
FAX (602) 968-5132

(Northern)
Cain White & Co.
Los Altos, California
(415) 948-6533
FAX (415) 948-0115

NEW HAMPSHIRE
R.J. Sickles Associates
Lexington, Massachusetts
(617) 862-5100
FAX (617) 863-0684

NEW JERSEY
(Northern)
U.S. Technical Marketing
Kings Park, New York
(516) 724-4250
FAX (516) 724-1542

(Southern)
Beacon North
Sterling, Virginia
(800) 877-3747
FAX (703) 435-7115

NEW MEXICO
Nelco TWO Company
Albuquerque, New Mexico
(505) 293-1399
FAX (505) 293-1011

NEW YORK
(Metropolitan & Long Island)
U.S. Technical Marketing
Kings Park, New York
(516) 724-4250
FAX (516) 724-1542

(Upstate)
Robtron
Skaneateles, New York
(315) 685-5731
FAX (315) 685-3717

NORTH CAROLINA
Beacon Electronics
Raleigh, North Carolina
(919) 787-0330
FAX (919) 781-8431

NORTH DAKOTA
Ohms Technology
Edina, Minnesota
(612) 932-2920
FAX (612) 932-2918

OHIO
Cain-Forlaw Co., Inc.
Worthington, Ohio
(614) 436-3004
FAX (614) 436-3097

OKLAHOMA
The Thorson Company
Dallas, Texas
(214) 233-5744
FAX (214) 702-0993

OREGON
Cain Sweet & Co.
Bellevue, Washington
(206) 462-2118
FAX (206) 451-9418

PENNSYLVANIA
(Eastern)
Beacon North
Sterling, Virginia
(800) 877-3747
FAX (703) 435-7115

(Western)
Cain-Forlaw Co., Inc.
Worthington, Ohio
(614) 436-3004
FAX (614) 436-3097

PUERTO RICO
Comlinear Corporation
Fort Collins, Colorado
(800) 776-0500
FAX (303) 226-0564

RHODE ISLAND
R.J. Sickles Assoicates
Lexington, Massachusetts
(617) 862-5100
FAX (617) 863-0684

SOUTH CAROLINA
Beacon Electronics
Atlanta, Georgia
(404) 256-9640
FAX (404) 256-1398

SOUTH DAKOTA
Ohms Technology
Edina, Minnesota
(612) 932-2920
FAX (612) 932-2918

TENNESSEE
(Central & Western)
Beacon Electronics
Huntsville, Alabama
(205) 881-5031
FAX (205) 883-9516

(Eastern)
Beacon Electronics
Knoxville, Tennessee
(615) 691-0062
FAX (615) 691-3586

TEXAS
(El Paso)
Nelco TWO Company
Albuquerque, New Mexico
(505) 293-1399
FAX (505) 293-1011

(Rest of Texas)
The Thorson Company
Dallas, Texas
(214) 233-5744
FAX (214) 702-0993

UTAH
Front Range Microwave
Englewood, Colorado
(303) 791-4405
FAX (303) 791-4406

VERMONT
R.J. Sickles Associates
Lexington, Massachusetts
(617) 862-5100
FAX (617) 863-0684

VIRGINIA
Beacon North
Sterling, Virginia
(800) 877-3747
FAX (703) 435-7115

WASHINGTON
Cain Sweet & Co.
Bellevue, Washington
(206) 462-2118
FAX (206) 451-9418

UNITED STATES SALES REPRESENTATIVES

WASHINGTON, D.C.
Beacon North
Sterling, Virginia
(800) 877-3747
FAX (703) 435-7115

WEST VIRGINIA
Beacon North
Sterling, Virginia
(800) 877-3747
FAX (703) 435-7115

WISCONSIN
(Western)
Ohms Technology
Edina, Minnesota
(612) 932-2920
FAX (612) 932-2918

(Eastern)
Dytec Central
Arlington Heights, Illinois
(708) 394-3380
FAX (708) 394-0270

WYOMING
Front Range Microwave
Englewood, Colorado
(303) 791-4405
FAX (303) 791-4406

INTERNATIONAL SALES REPRESENTATIVES

EUROPE

AUSTRIA
Transtech Hochfrequenztechnik
GmbH & Co. KG
Munich, Germany
(011) 49-89-843017
FAX (011) 49-89-8417568

BELGIUM
Tekelec Belgium NV/SA
Halle
(011) 32-2-3601288
FAX (011) 32-2-3603807

CZECHOSLOVAKIA
Transtech Praha spol. s.r.o.
Prague
(011) 42-2-806-753
FAX (011) 42-2-809-874

DENMARK
Exatec A/S
Copenhagen
(011) 45-31-19-10-22
FAX (011) 45-31-19-31-20

FRANCE
Micro Puissance
Les Ulis, Cedex
(011) 33-1-69071211
FAX (011) 33-1-69076712

GERMANY
Transtech Hochfrequenztechnik
GmbH & Co. KG
Heilbronn
(011) 49-7131-593-0
FAX (011) 49-7131-593-193

NETHERLANDS
Tekelec Airtronic B.V.
Zoetermeer
(011) 31-7-9310100
FAX (011) 31-7-9417504

IRELAND
Joseph Electronics, Ltd.
Birmingham, England
(011) 4421-643-6999
FAX (011) 4421-643-2011

ISRAEL
Elul Technologies, Ltd.
Tel-Aviv
(011) 972-3-6970707
FAX (011) 972-3-6950484

ITALY
Microelit S.P.A.
Milano
(011) 39-2-4817900
FAX (011) 39-2-4813594

PORTUGAL
Anatronic, S.A.
Madrid, Spain
(011) 34-1-542-4455
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